

# DATA SHEET

**74LV00**

Quad 2-input NAND gate

Product specification  
Supersedes data of 1998 Apr 13  
IC24 Data Handbook

1998 Apr 20

# Quad 2-input NAND gate

# 74LV00

## FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Output capability: standard
- $I_{CC}$  category: SSI

## DESCRIPTION

The 74LV00 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT00.

The 74LV00 provides the 2-input NAND function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay nA, nB to nY	$C_L = 15$ pF; $V_{CC} = 3.3$ V	7	ns
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per gate	See Notes 1 and 2	22	pF

### NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = \text{GND to } V_{CC}$ .

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
14-Pin Plastic DIL	$-40^{\circ}\text{C to } +125^{\circ}\text{C}$	74LV00 N	74LV00 N	SOT27-1
14-Pin Plastic SO	$-40^{\circ}\text{C to } +125^{\circ}\text{C}$	74LV00 D	74LV00 D	SOT108-1
14-Pin Plastic SSOP Type II	$-40^{\circ}\text{C to } +125^{\circ}\text{C}$	74LV00 DB	74LV00 DB	SOT337-1
14-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C to } +125^{\circ}\text{C}$	74LV00 PW	74LV00PW DH	SOT402-1

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 9, 12	1A – 4A	Data inputs
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	$V_{CC}$	Positive supply voltage

## FUNCTION TABLE

INPUTS		OUTPUTS
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

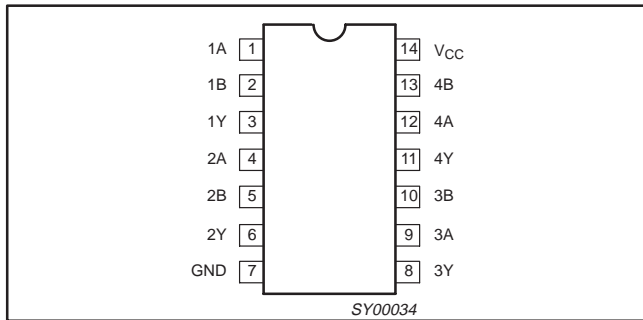
### NOTES:

- H = HIGH voltage level  
L = LOW voltage level

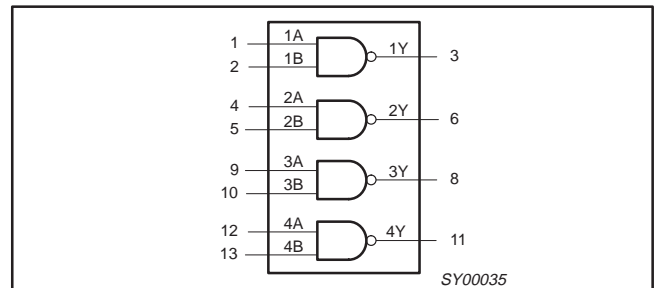
# Quad 2-input NAND gate

74LV00

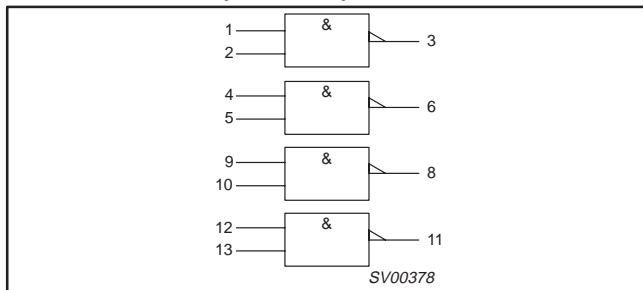
## PIN CONFIGURATION



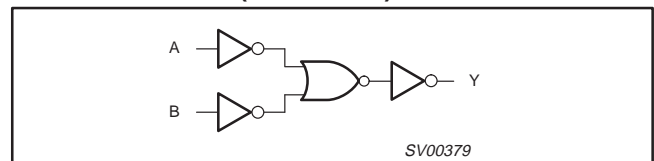
## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM (ONE GATE)



## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note 1	1.0	3.3	5.5	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$ $V_{CC} = 3.6V$ to $5.5V$	– – – –	– – – –	500 200 100 50	ns/V

**NOTE:**

1. The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 5.5V$ .

## Quad 2-input NAND gate

74LV00

**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$ , $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with – standard outputs		50	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2V$	0.9			0.9		V
		$V_{CC} = 2.0V$	1.4			1.4		
		$V_{CC} = 2.7$ to $3.6V$	2.0			2.0		
		$V_{CC} = 4.5$ to $5.5V$	$0.7 \cdot V_{CC}$			$0.7 \cdot V_{CC}$		
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2V$			0.3		0.3	V
		$V_{CC} = 2.0V$			0.6		0.6	
		$V_{CC} = 2.7$ to $3.6V$			0.8		0.8	
		$V_{CC} = 4.5$ to $5.5V$			$0.3 \cdot V_{CC}$		$0.3 \cdot V_{CC}$	
$V_{OH}$	HIGH level output voltage; all outputs	$V_{CC} = 1.2V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	2.8	3.0		2.8		
		$V_{CC} = 4.5V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	4.3	4.5		4.3		
$V_{OH}$	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 6mA$	2.40	2.82		2.20		V
		$V_{CC} = 4.5V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 12mA$	3.60	4.20		3.50		
$V_{OL}$	LOW level output voltage; all outputs	$V_{CC} = 1.2V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0				V
		$V_{CC} = 2.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 2.7V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 4.5V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
$V_{OL}$	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 6mA$		0.25	0.40		0.50	V
		$V_{CC} = 4.5V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 12mA$		0.35	0.55		0.65	

# Quad 2-input NAND gate

74LV00

## DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$I_I$	Input leakage current	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND			1.0		1.0	$\mu A$
$I_{CC}$	Quiescent supply current; SSI	$V_{CC} = 5.5V; V_I = V_{CC}$ or GND; $I_O = 0$			20.0		40	$\mu A$
$\Delta I_{CC}$	Additional quiescent supply current	$V_{CC} = 2.7V$ to 3.6V; $V_I = V_{CC} - 0.6V$			500		850	$\mu A$

**NOTE:**

1. All typical values are measured at  $T_{amb} = 25^\circ C$ .

## AC CHARACTERISTICS

$GND = 0V; t_r = t_f \leq 2.5ns; C_L = 50pF; R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				$V_{CC}(V)$	MIN	TYP <sup>1</sup>	MAX	MIN	
$t_{PHL/PLH}$	Propagation delay nA, nB to nY	Figures 1, 2	1.2		45				ns
			2.0		15	26		31	
			2.7		11	18		23	
			3.0 to 3.6		9 <sup>2</sup>	15		18	
			4.5 to 5.5		6.5 <sup>3</sup>	11		14	

**NOTES:**

1. Unless otherwise stated, all typical values are measured at  $T_{amb} = 25^\circ C$ .
2. Typical values are measured at  $V_{CC} = 3.3 V$ .
3. Typical values are measured at  $V_{CC} = 5.0 V$ .

## AC WAVEFORMS

$V_M = 1.5 V$  at  $V_{CC} \geq 2.7 V$  and  $\leq 3.6 V$ ;  
 $V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7 V$  and  $\geq 4.5 V$ ;  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

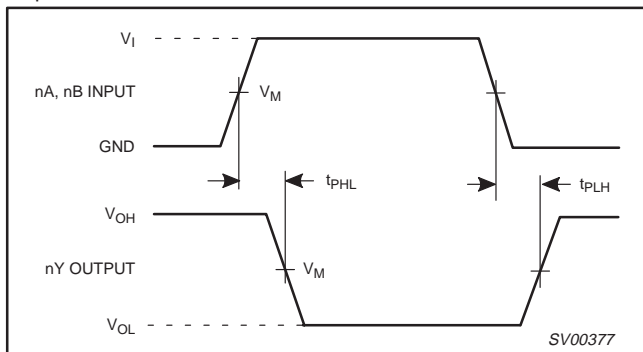


Figure 1. Input (nA, nB) to output (nY) propagation delays.

## TEST CIRCUIT

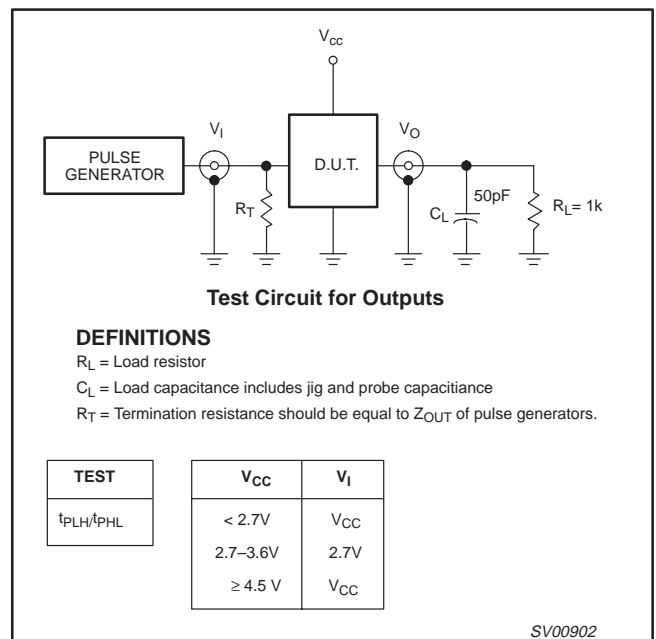


Figure 2. Load circuitry for switching times.

# Quad 2-input NAND gate

## 74LV00

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

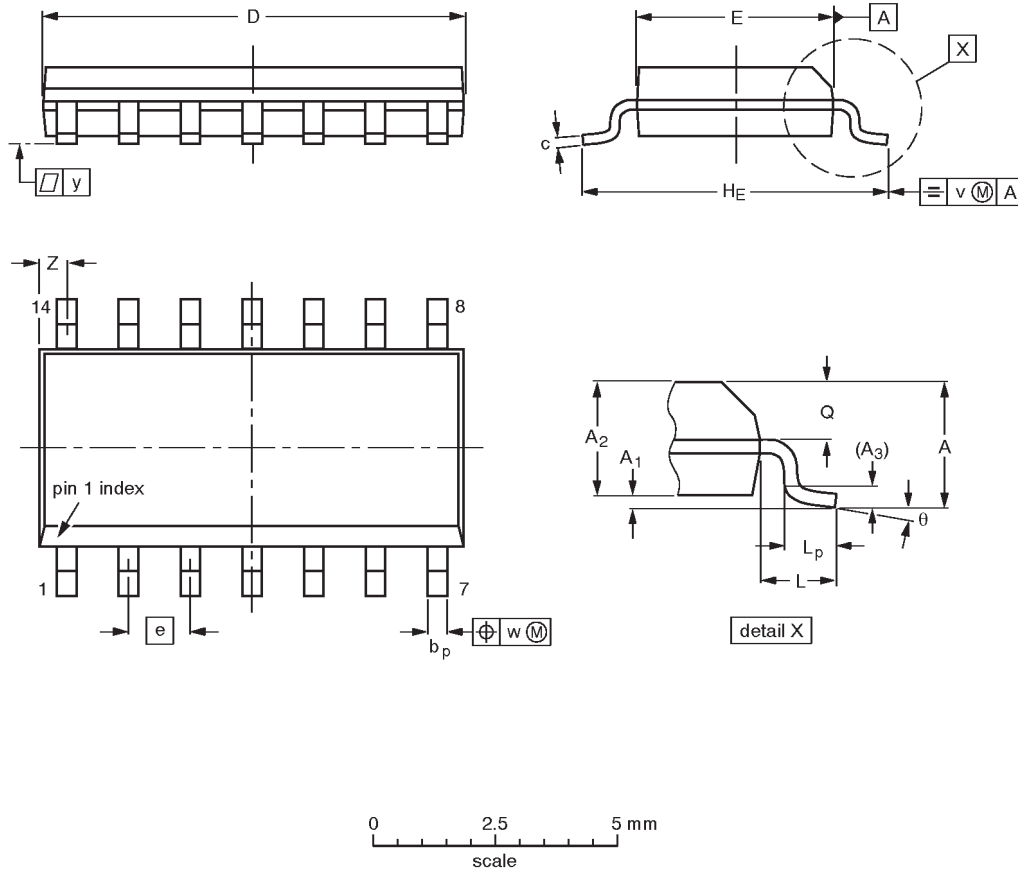
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11

# Quad 2-input NAND gate

# 74LV00

**SO14: plastic small outline package; 14 leads; body width 3.9 mm**

**SOT108-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				91-08-13 95-01-23

# Quad 2-input NAND gate

# 74LV00

**SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm**

**SOT337-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				<del>95-02-04</del> 96-01-18

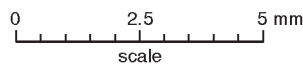
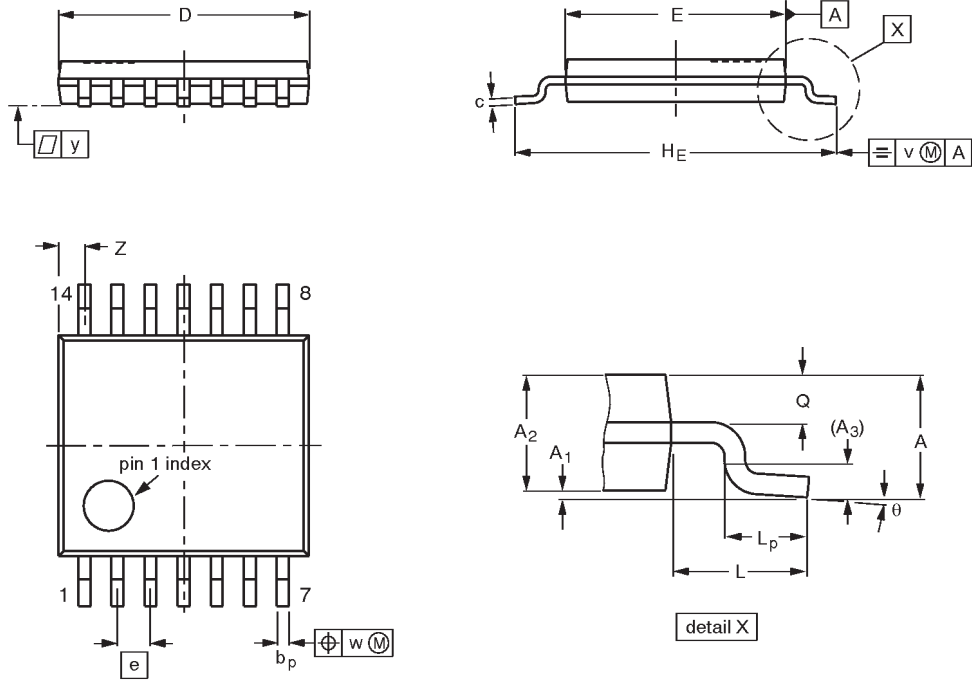


# Quad 2-input NAND gate

# 74LV00

**TSSOP14:** plastic thin shrink small outline package; 14 leads; body width 4.4 mm

**SOT402-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-94-07-12- 95-04-04

## Quad 2-input NAND gate

74LV00

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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