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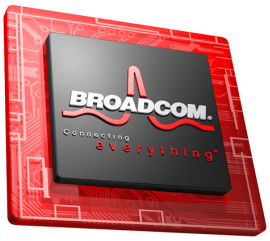
BCM8128
PRODUCT Brief



MULTI-RATE 10-GBPS SONET/SDH/10GE/FEC MUX

FEATURES

- 10-Gigabit MSA (Multi-Source Agreement) compliant
- Fully integrated Clock Multiplication Unit (CMU) supports multiple rates: OC-192, 10GE, 10GFC and its FEC rates
- 16:1 multiplexer with LVDS data input
- Configurable divide by 16 or 32 clock modes
- Configurable LVDS input clock-to-data bus timing skew control
- On-chip 16 x 10 FIFO eliminates system timing issues
- Serial data polarity invert
- Bit order reversal
- Low Jitter 10 Gigabit Output Clock for retiming lased Tx clock output
- Lock detect
- Core power supply: 1.8V
- I/O power supply: CML at 1.8V, LVDS and CMOS at 1.8V or 3.3V
- Power consumption: 450 mW
- Standard CMOS fabrication process
- 127-pin BGA package

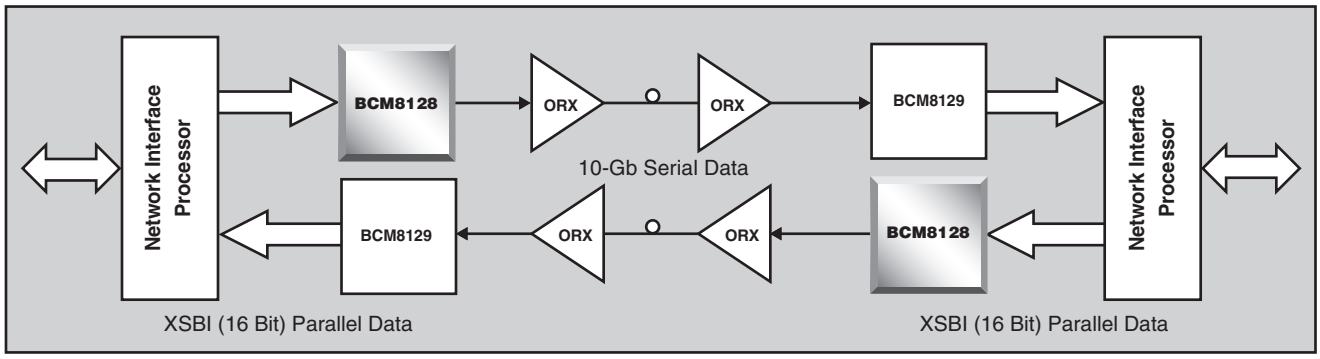
SUMMARY OF BENEFITS

- Compliant with Optical Internetworking Forum (OIF), Telcordia, ITU-T, ANSI, and IEEE 802.3ae industry standards.
- Reduces design cycle and time to market.
- High level of integration allows for higher port density solutions.
- Uses the most effective silicon economy of scale for CMOS-based devices.
- Low-power consumption eliminates the need for external cooling sources.

APPLICATIONS

- OC-192/STM-64/10GE transmission equipment
- SONET/SDH optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbones
- SONET test equipment
- Terabit routers
- Edge routers

BCM8128 Functional Block Diagram



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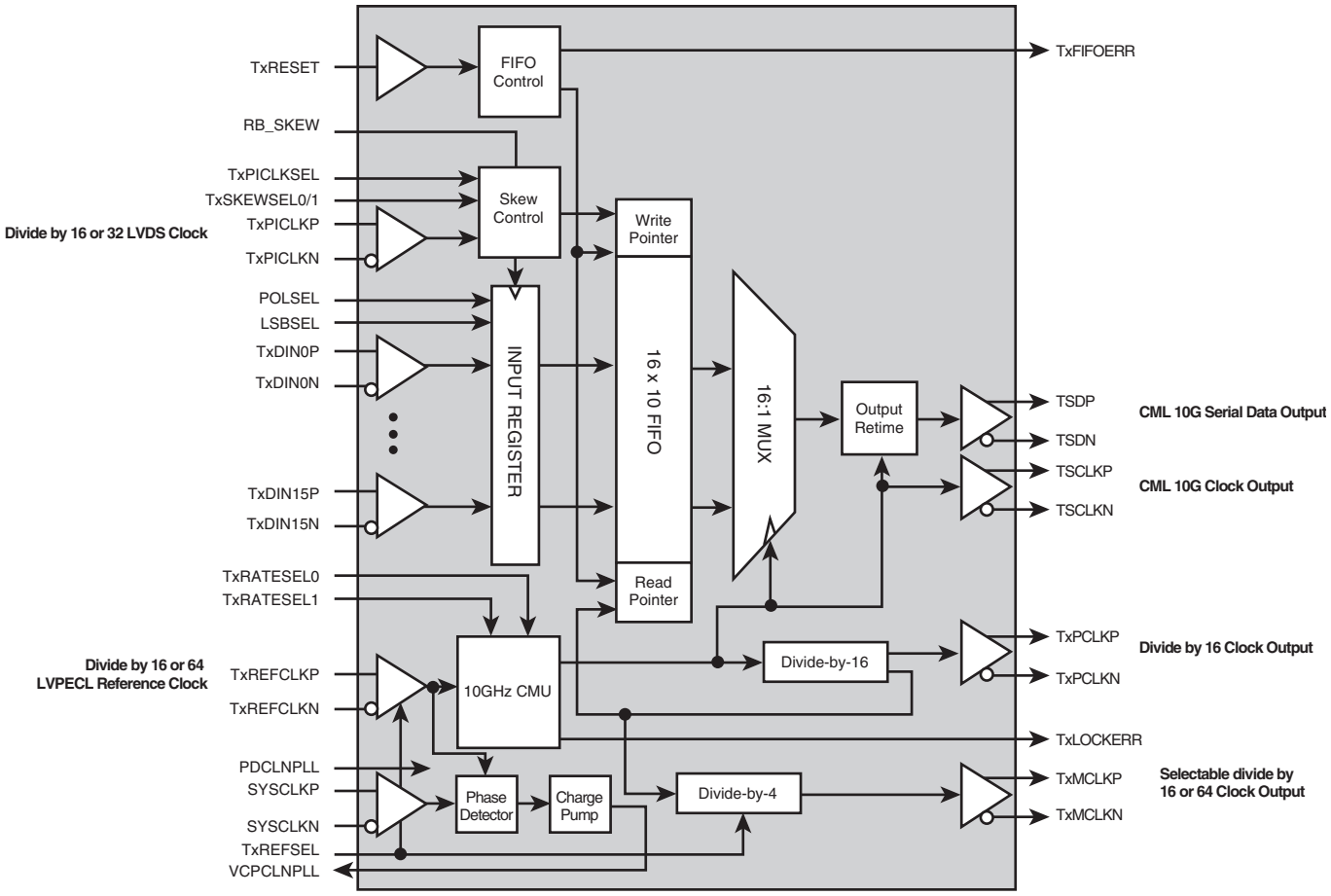
OVERVIEW



The **BCM8128** is a fully integrated MSA-compliant quad-rate SONET/SDH/10GE transmitter operating at OC-192 (9.953 Gbps), 10GE (10.3125 Gbps), 10GFC (10.513 Gbps), and FEC (Forward Error Correction) data rates (10.664/10.709, 11.096, or 11.31 Gbps) with serializer and Clock Multiplication Unit (CMU). The low-jitter LVDS interface and onboard low-jitter PLL exceed Optical Internetworking Forum (OIF), IEEE 802.3ae, Telcordia, ANSI, and ITU-T jitter standards.

The **BCM8128** reference clock input frequency is user-selectable to the line rate divided by either 16 or 64. The two reference clock outputs can be squelched under user control.

The **BCM8128** provides skew control between the LVDS transmit parallel input clock and data to accommodate difficult timing variances. A 10-word FIFO decouples the parallel input timing domain from the serial output timing domain.

The **BCM8128** provides a CML serial output clock to retime the data at the optical interface.

The **BCM8128** can be powered with a single 1.8V supply or dual 1.8/3.3V supply without any special power supply sequencing requirements.

The **BCM8128** comes in a 11 x 11 mm, 127-pin BGA package.

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BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

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Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com