



P-Channel Enhancement-Mode Vertical DMOS Power FETs

Objective
T-37-25

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package	
			TO-220	TO-92
-100V	0.8Ω	-5A	IRF9522	R9522
-60V	0.8Ω	-5A	IRF9523	R9523

Features

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

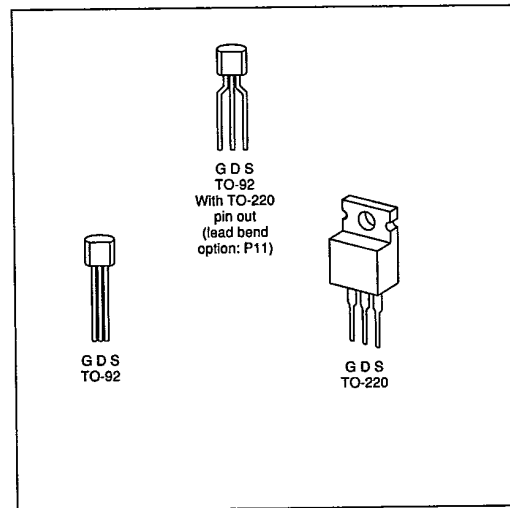
- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Package Options



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JC} $^\circ\text{C/W}$	θ_{JA} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
IRF9522 IRF9523	-5.0A	-20.0A	40W	80	3.12	-5.0A	-20.0A
R9522 R9523	-0.55A	-7.0A	1W	125	170	-0.55A	-7.0A

* I_D (continuous) is limited by max rated T_J .

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Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRF9522	-100			V	$V_{GS} = 0V, I_D = -250\mu A$
		R9522					
		IRF9523	-60				
$V_{GS(th)}$	Gate Threshold Voltage		-2.0		-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
I_{GSS}	Gate Body Leakage				-500	nA	$V_{GS} = \pm 20V, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current				-250	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$ $V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_C = 125^\circ\text{C}$
					-1000		
$I_{D(ON)}$	ON-State Drain Current		-5.0			A	$V_{DS} > I_{D(ON)} \times R_{DS(ON)}$ Max Rating $V_{GS} = -10V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance				0.8	Ω	$V_{GS} = -10V, I_D = -3.5A$
G_{FS}	Forward Transconductance		0.9			S	$V_{DS} > I_{D(ON)} \times R_{DS(ON)}$ Max $I_D = -3.5A$
C_{ISS}	Input Capacitance				450	pF	$V_{GS} = 0, V_{DS} = -25V$ $f = 1.0 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance				350		
C_{RSS}	Reverse Transfer Capacitance				100		
$t_{d(ON)}$	Turn-ON Delay Time				50	ns	$V_{DD} = 0.5BV_{DSS}$ $I_D = -3.5A$ $R_G = 50\Omega$
t_r	Rise Time				100		
$t_{d(OFF)}$	Turn-OFF Delay Time				100		
t_f	Fall Time				100		
V_{SD}	Diode Forward Voltage Drop				-6.0		
t_{rr}	Reverse Recovery Time			230		ns	$T_J = 150^\circ\text{C}, I_F = -6.0A,$ $dI_{F/dt} = 100A/\mu S$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: $300\mu s$ pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

