INTEGRATED CIRCUITS

DATA SHEET

74AHC541; 74AHCT541
Octal buffer/line driver; 3-state

Product specification
Supersedes data of 1998 Sep 21
File under Integrated Circuits, IC06

1999 Nov 24

Philips
Semiconductors

PHILIPS

FEATURES

- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V
  CDM EIA/JESD22-C101 exceeds 1000 V
- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V_{CC}
- For AHC only: operates with CMOS input levels
- For AHCT only: operates with TTL input levels
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74AHC/AHCT541 is a high-speed Si-gate CMOS device.

The 74AHC/AHCT541 are octal non-inverting buffer/line drivers with 3-state bus compatible outputs.

The 3-state outputs are controlled by the output enable inputs $\overline{OE}_0$ and $\overline{OE}_1$.

A HIGH on $\overline{OE}_n$ causes the outputs to assume a high-impedance OFF-state.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC	AHCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	C_L = 15 pF; V_{CC} = 5 V	3.5	3.5	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND	3	3	pF
C_O	output capacitance		4.0	4.0	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	10	12	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT			OUTPUT
$\overline{OE}_0$	$\overline{OE}_1$	A_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don't care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

OUTSIDE NORTH AMERICA	NORTH AMERICA	PACKAGES			
		PINS	PACKAGE	MATERIAL	CODE
74AHC541D	74AHC541D	20	SO	plastic	SOT163-1
74AHC541PW	74AHC541PW DH	20	TSSOP	plastic	SOT360-1
74AHCT541D	74AHCT541D	20	SO	plastic	SOT163-1
74AHCT541PW	7AHCT541PW DH	20	TSSOP	plastic	SOT360-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}_0$	output enable input
2, 3, 4, 5, 6, 7, 8 and 9	A_0 to A_7	data inputs
10	GND	ground (0 V)
11, 12, 13, 14, 15, 16, 17 and 18	Y_7 to Y_0	data inputs/outputs
19	$\overline{OE}_1$	output enable input
20	V_{CC}	DC supply voltage

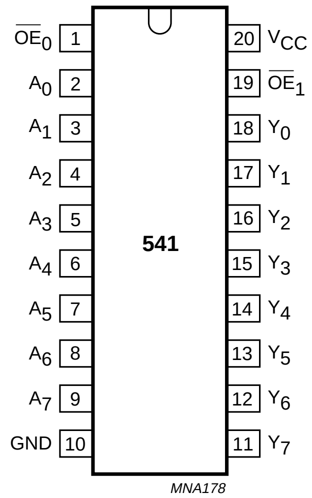


Fig.1 Pin configuration.

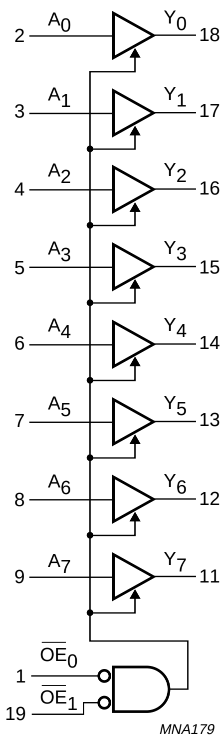


Fig.2 Logic symbol.

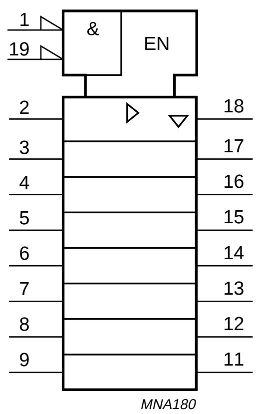


Fig.3 IEEE/IEC logic symbol.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC			74AHCT			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	+25	+125	–40	+25	+125	°C
t_r,t_f (Δt/Δf)	input rise and fall times	V_{CC} = 3.3 ±0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 ±0.5 V	–	–	20	–	–	20	

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	DC input diode current	V_I < –0.5 V; note 1	–	–20	mA
I_{OK}	DC output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	DC output source or sink current	–0.5 V < V_O < V_{CC} + 0.5 V	–	±25	mA
I_{CC}	DC V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range: –40 to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO-package: above 70 °C the value of P_D derates linearly with 8 mW/K.
   For TSSOP-package: above 60 °C the value of P_D derates linearly with 5.5 mW/K.

DC CHARACTERISTICS

Family 74AHC

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	
			5.5	3.85	–	–	3.85	–	3.85	–	
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	
			5.5	–	–	1.65	–	1.65	–	1.65	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -50$ µA	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	
			4.5	4.4	4.5	–	4.4	–	4.4	–	
		$V_I = V_{IH}$ or V_{IL}; $I_O = -4.0$ mA	3.0	2.58	–	–	2.48	–	2.40	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ µA	2.0	–	0	0.1	–	0.1	–	0.1	V
			3.0	–	0	0.1	–	0.1	–	0.1	
			4.5	–	0	0.1	–	0.1	–	0.1	
		$V_I = V_{IH}$ or V_{IL}; $I_O = 4.0$ mA	3.0	–	–	0.36	–	0.44	–	0.55	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	
I_I	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	0.1	–	1.0	–	2.0	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	µA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

Family 74AHCT

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		OTHER	V_{CC} (V)	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	2.0	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = -50$ µA	4.5	4.4	4.5	–	4.4	–	4.4	–	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = -8.0$ mA	4.5	3.94	–	–	3.8	–	3.70	–	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; $I_O = 50$ µA	4.5	–	0	0.1	–	0.1	–	0.1	V
		$V_I = V_{IH}$ or V_{IL}; $I_O = 8.0$ mA	4.5	–	–	0.36	–	0.44	–	0.55	V
I_I	input leakage current	$V_I = V_{IH}$ or V_{IL}	5.5	–	–	0.1	–	1.0	–	2.0	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; $I_O = 0$	5.5	–	–	±0.25	–	±2.5	–	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	5.5	–	–	4.0	–	40	–	80	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V other inputs at V_{CC} or GND; $I_O = 0$	4.5 to 5.5	–	–	1.35	–	1.5	–	1.5	mA
C_I	input capacitance		–	–	3	10	–	10	–	10	pF

AC CHARACTERISTICS

Type 74AHC541

Ground = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 3.0 to 3.6 V; note 1											
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	see Figs 4 and 6	15 pF	–	5.0	7.0	1.0	8.5	1.0	9.0	ns
t_{PZL}/t_{PZH}	propagation delay $\overline{OE}_n$ to Y_n	see Figs 5 and 6		–	5.5	10.5	1.0	11.0	1.0	13.5	ns
t_{PLZ}/t_{PHZ}	propagation delay $\overline{OE}_n$ to Y_n			–	6.0	11.0	1.0	12.0	1.0	14.0	ns
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	see Figs 4 and 6	50 pF	–	7.0	10.5	1.0	12.0	1.0	13.5	ns
t_{PZL}/t_{PZH}	propagation delay $\overline{OE}_n$ to Y_n	see Figs 5 and 6		–	7.5	14.0	1.0	16.0	1.0	17.5	ns
t_{PLZ}/t_{PHZ}	propagation delay $\overline{OE}_n$ to Y_n			–	9.5	15.4	1.0	17.5	1.0	19.5	ns
V_{CC} = 4.5 to 5.5 V; note 2											
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	see Figs 4 and 6	15 pF	–	3.5	5.0	1.0	6.0	1.0	6.5	ns
t_{PZL}/t_{PZH}	propagation delay $\overline{OE}_n$ to Y_n	see Figs 5 and 6		–	3.5	7.2	1.0	8.5	1.0	9.0	ns
t_{PLZ}/t_{PHZ}	propagation delay $\overline{OE}_n$ to Y_n			–	4.5	7.5	1.0	8.0	1.0	9.5	ns
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	see Figs 4 and 6	50 pF	–	5.0	7.0	1.0	8.0	1.0	9.0	ns
t_{PZL}/t_{PZH}	propagation delay $\overline{OE}_n$ to Y_n	see Figs 5 and 6		–	5.0	9.2	1.0	10.5	1.0	11.5	ns
t_{PLZ}/t_{PHZ}	propagation delay $\overline{OE}_n$ to Y_n			–	6.5	8.8	1.0	10.0	1.0	11.0	ns

Notes

1. Typical values at V_{CC} = 3.3 V.
2. Typical values at V_{CC} = 5.0 V.

Type 74AHCT541

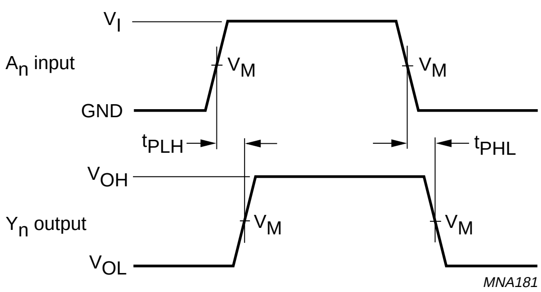
Ground = 0 V; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)							UNIT
		WAVEFORMS	C_L	25			−40 to +85		−40 to +125		
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{CC} = 4.5 to 5.5 V; note 1											
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	see Figs 4 and 6	15 pF	–	3.5	5.5	1.0	6.5	1.0	7.0	ns
t_{PZL}/t_{PZH}	propagation delay $\overline{OE}_n$ to Y_n	see Figs 5 and 6		–	4.0	7.0	1.0	8.0	1.0	9.0	ns
t_{PLZ}/t_{PHZ}	propagation delay $\overline{OE}_n$ to Y_n			–	5.0	7.0	1.0	8.0	1.0	9.0	ns
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	see Figs 4 and 6	50 pF	–	5.0	8.5	1.0	9.5	1.0	11.0	ns
t_{PZL}/t_{PZH}	propagation delay $\overline{OE}_n$ to Y_n	see Figs 5 and 6		–	5.5	10.0	1.0	12.0	1.0	12.5	ns
t_{PLZ}/t_{PHZ}	propagation delay $\overline{OE}_n$ to Y_n			–	7.0	10.0	1.0	12.0	1.0	12.5	ns

Note

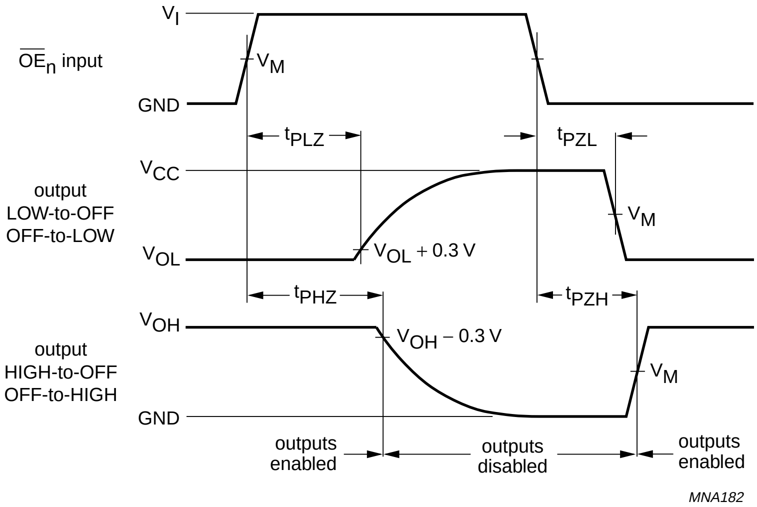
1. Typical values at V_{CC} = 5.0 V.

AC WAVEFORMS



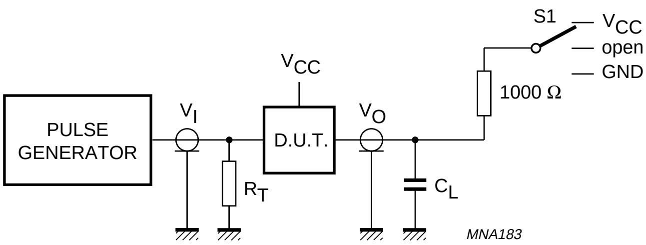
FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.4 The input (A_n) to output (Y_n) propagation delays.



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	50% V_{CC}	50% V_{CC}
AHCT	GND to 3.0 V	1.5 V	50% V_{CC}

Fig.5 The 3-state output enable and disable times.



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit.

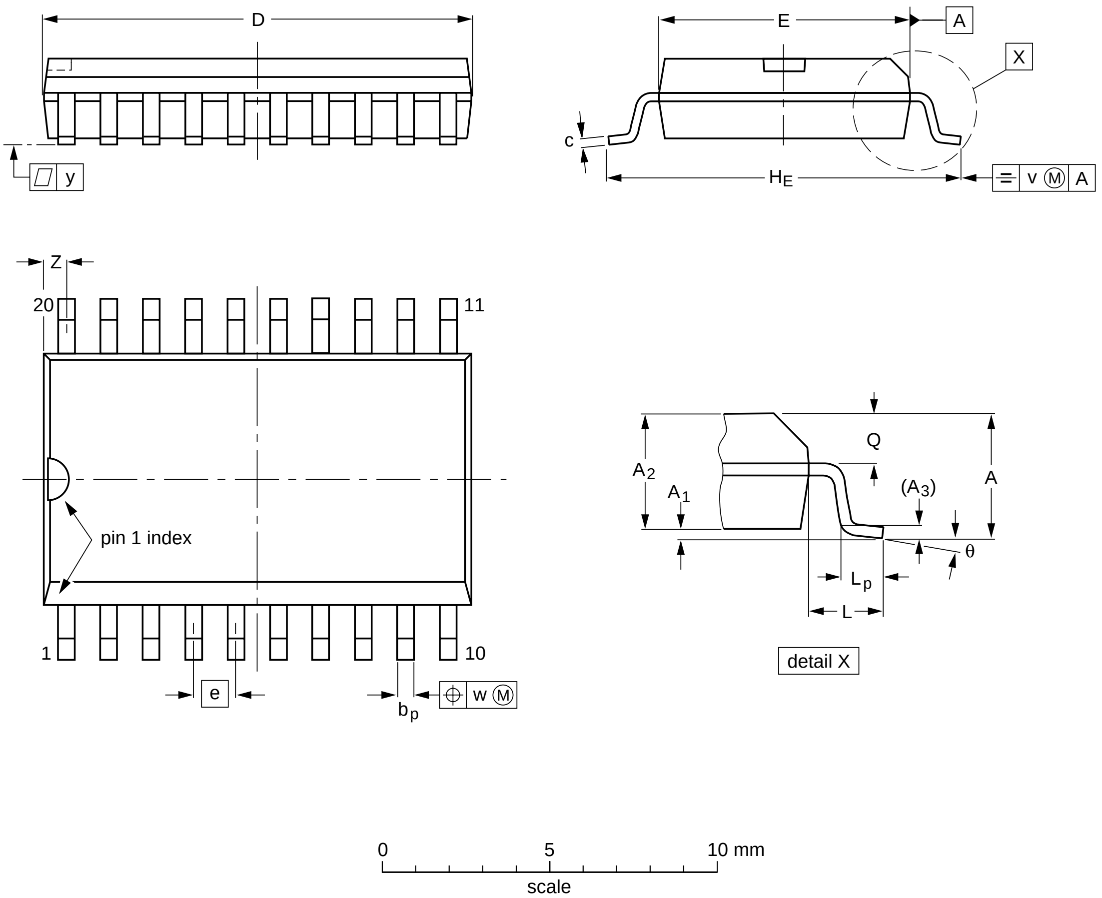
C_L = load capacitance including jig and probe capacitance (See Chapter “AC characteristics”).

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.6 Load circuitry for switching times.

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

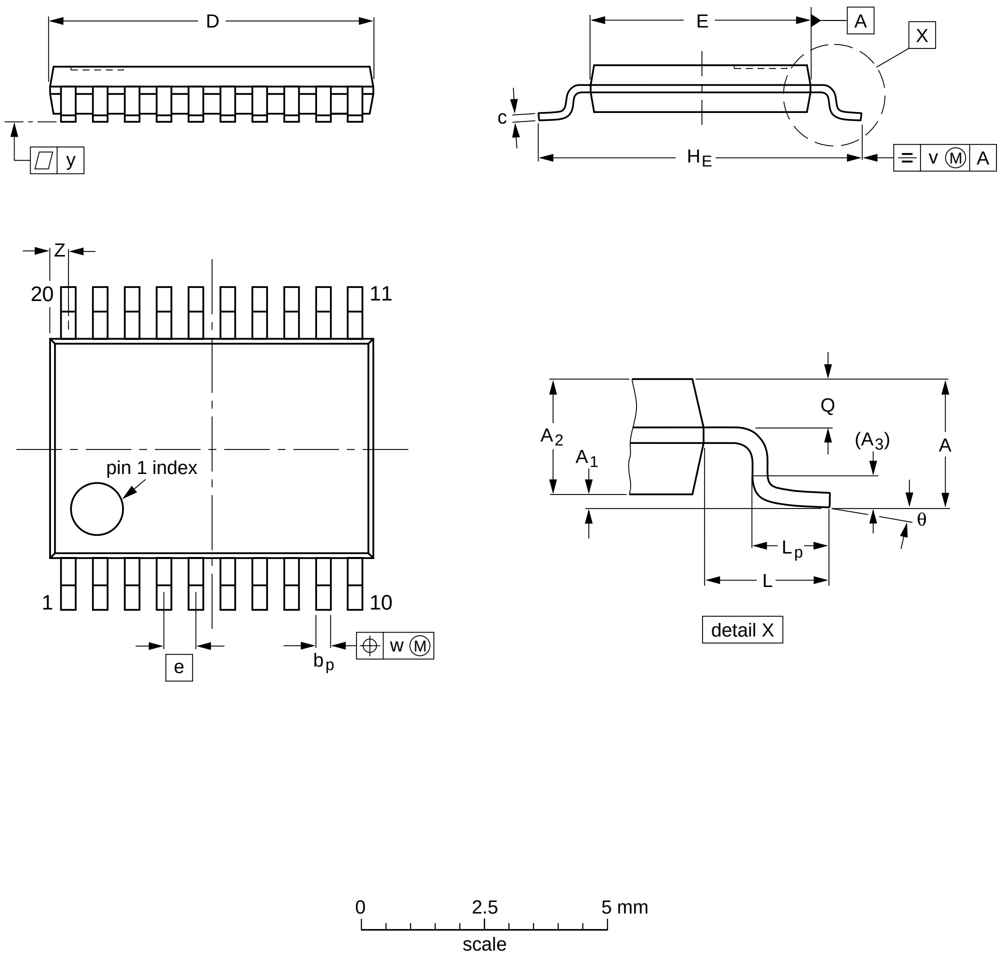
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(2)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				~~93-06-16~~ 95-02-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Printed in The Netherlands 245002/02/pp16 Date of release: 1999 Nov 24 Document order number: 9397 750 06301