❑ MN102L36K / L360C

Type	**MN102L36K [ES (Engineering Sample) available] / L360C**
ROM (×8-Bit / ×16-Bit)	256 K / External
RAM (×8-Bit / ×16-Bit)	10 K / 5 K
Minimum Instruction Execution Time	**100 ns (at 4.5 V to 5.5 V, 20 MHz)** **200 ns (at 2.7 V to 3.6 V, 10 MHz)**

Interrupts

• RESET • Watchdog • Timer Counter 0 to 5 • Fixed-Length Serial ch 0,1 Transmission
• Fixed-Length Serial Ch 0,1 Reception • Timer Counter 6 to 7 • Timer Counter 6 to 7 Compare Capture A
• Timer Counter 6 to 7 Compare Capture B • ACT Transfer Finish • External 0 to 7 • Serial ch 0,1 Transmission
• Serial ch 0,1 Reception • NMI Pin • A/D Conversion Finish

Timer Counter

Timer Counter 0: 8-Bit × 1 (Timer Output, Event Count)
Clock Source . 1/1, 1/128 of System Clock, 1/4 of Low Speed Clock, External Clock
Interrupt Source . . .Timer Counter 0 Underflow

Timer Counter 1: 8-Bit × 1 (Timer Output, Even Count, A/D Conversion Start)
Clock Source System Clock, 1/4 of Low Speed Clock, External Clock, Timer Counter 0 Output
Interrupt Source Timer Counter 1 Underflow

Timer Counter 2 to 3: 8-Bit × 1 (Timer Output, Event Count, UART Baud Rate Generation)
Clock Source System Clock, External Clock, Timer Counter 0 Output, Timer Counter 1, 2 Output
Interrupt Source Timer Counter 2, 3 Underflow

Timer Counter 4,5: 8-Bit × 1 (Timer Output, Event Count)
Clock Source . 1/4 of Low Speed Clock, External Clock, Timer Counter 0 Output, Timer Counter 3, 4 Output
Interrupt Source . .Timer Counter 4, 5 Underflow

Timer Counter 6, 7: 16-Bit × 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encoder Input)
Clock Source . System Clock, External Clock, Timer Counter 4, 5 Output
Interrupt Source Coincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture, Underflow of Timer Counter 6, 7

(Connectable) Timer Counter 0 to 5

Serial Interface

Serial 0: 7, 8-Bit × 1 (Common use with UART, Transfer Direction of MSB/LSB Selectable)
Clock Source 1/16 of Timer Counter 2, 1/16 of Timer Counter 3, External Clock, 1/2 of Timer Counter 2
I^2C Mode (Master Transmission/Reception is Possible in The Single Master System)

Serial 1: 7, 8-Bit × 1 (Common use with UART, Transfer Direction of MSB/LSB Selectable)
Clock Source .. 1/16 of Timer Counter 2, 1/16 of Timer Counter 3, External Clock, 1/2 of Timer Counter 3)
I^2C Mode (Master Transmission/Reception is Possible in The Single Master System)

Fixed-Length serial 0: 8-Bit × 1
Clock Source External Clock
Sending Direction LSB

Fixed-Length serial 1: 8-Bit × 1
Clock Source . . .External Clock
Sending Direction .. . .LSB

I/O Pins	**I/O**	**104** **83**	• Common use 16 (by 8-Bits), 8 (by 4-Bits), 80 (by-bit) (MN102L36K) • Common use 8 (by 4-Bits), 75 (by-bit) (MN102L360C)
A/D Inputs			8-Bit × 8ch (with S/H)
D/A Inputs			8-Bit × 2ch
PWM			16-Bit × 2ch
Notes			Burst ROM interface support, ATC (support between serial 0 ch and built-in RAM)
Package			LQFP128-P-1818C

Electrical Characteristics

A/D Converter Characteristics (at VDD = 5 V)

Parameter	Symbol	Condition		Limit min	Limit typ	Limit max	Unit
A/D Conversion Relative Error		VDD = 5 V, VSS = 0 V	ch0 to 7			±3	LSB
A/D Conversion Time				48			µs
Analog Input Voltage	VIA			VSS		VDD	V

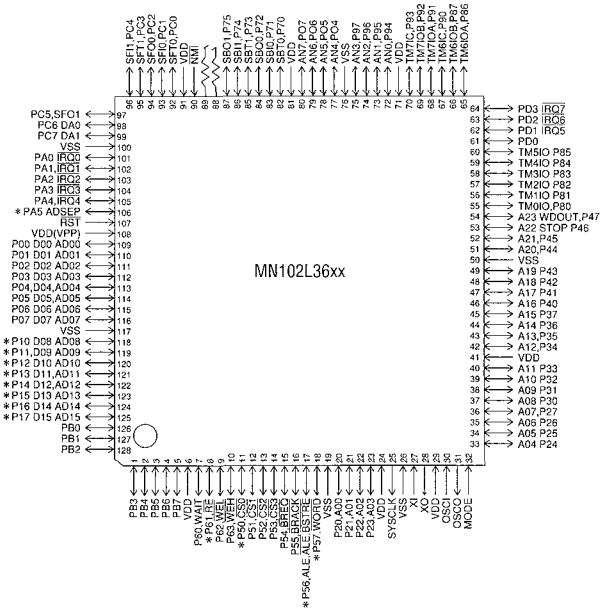
(Ta = 25 °C, VDD = 5.0 V, VSS = 0 V)

A/D Converter Characteristics (at VDD = 3 V)

Parameter	Symbol	Condition		Limit min	Limit typ	Limit max	Unit
A/D Conversion Relative Error		VDD = 3 V, VSS = 0 V	ch0 to 7			±3	LSB
A/D Conversion Time				96			µs
Analog Input Voltage	VIA			VSS		VDD	V

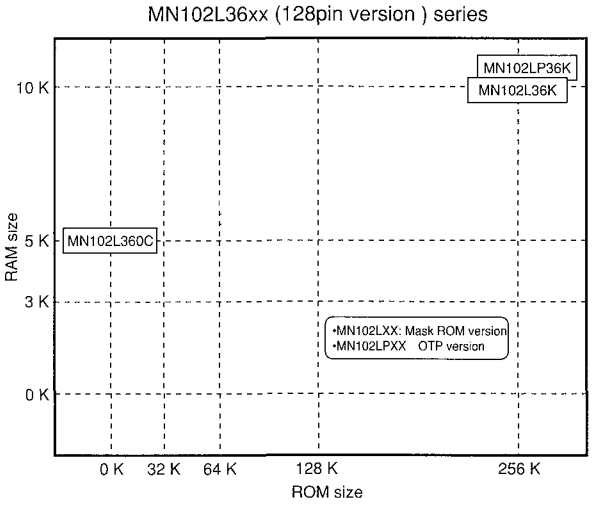
(Ta = 25 °C, VDD = 3.0 V, VSS = 0 V)

Pin Assignment



LQFP128-P-1818C

* Port unusable in MN102L360C



See the next page for support tool.

Support Tool

In-Circuit Emulator	PX-ICE102L00 + PX-PRB102L36	
EPROM built-in Type	**Type**	MN102LP36K [ES (Engineering Sample) available] / LP36Z
	ROM (× 8-Bit / × 16-Bit)	256 K / 128 K
	RAM (× 8-Bit / × 16-Bit)	10 K / 10 K
	Minimum Instruction Execution Time	100 µs (at 4.5 V to 5 5 V, 20 MHz) 200 µs (at 2.7 V to 3 6 V, 10 MHz)
	Package	LQFP128-P-1818C