ISSUE 10 May 1995

Features

- ST-BUS™ compatible
- Transmit/Receive filters & PCM Codec in one I.C
- Meets AT&T D3/D4 and CCITT G711 and G712
- μ-Law: MT8960/62/64/67
- A-Law: MT8961/63/65/67
- Low power consumption:
  Op.: 30 mW typ.
  Stby.: 2.5 mW typ.
- Digital Coding Options:
  MT8964/65/66/67 CCITT Code
  MT8960/61/62/63 Alternative Code
- Digitally controlled gain adjust of both filters
- Analog and digital loopback
- Filters and codec independently user accessible for testing
- Powerdown mode available
- 2.048 MHz master clock input
- Up to six uncommitted control outputs
- ±5V ±5% power supply

Ordering Information

MT8964/65AC	18 Pin Ceramic DIP
MT8960/61/64/65AE	18 Pin Plastic DIP
MT8962/63AE	20 Pin Plastic DIP
MT8962/63/66/67AS	20 Pin SOIC

0°C to+70°C

Description

Manufactured in ISO^2-CMOS, these integrated filter/codecs are designed to meet the demanding performance needs of the digital telecommunications industry, e.g., PABX, Central Office, Digital telephones.

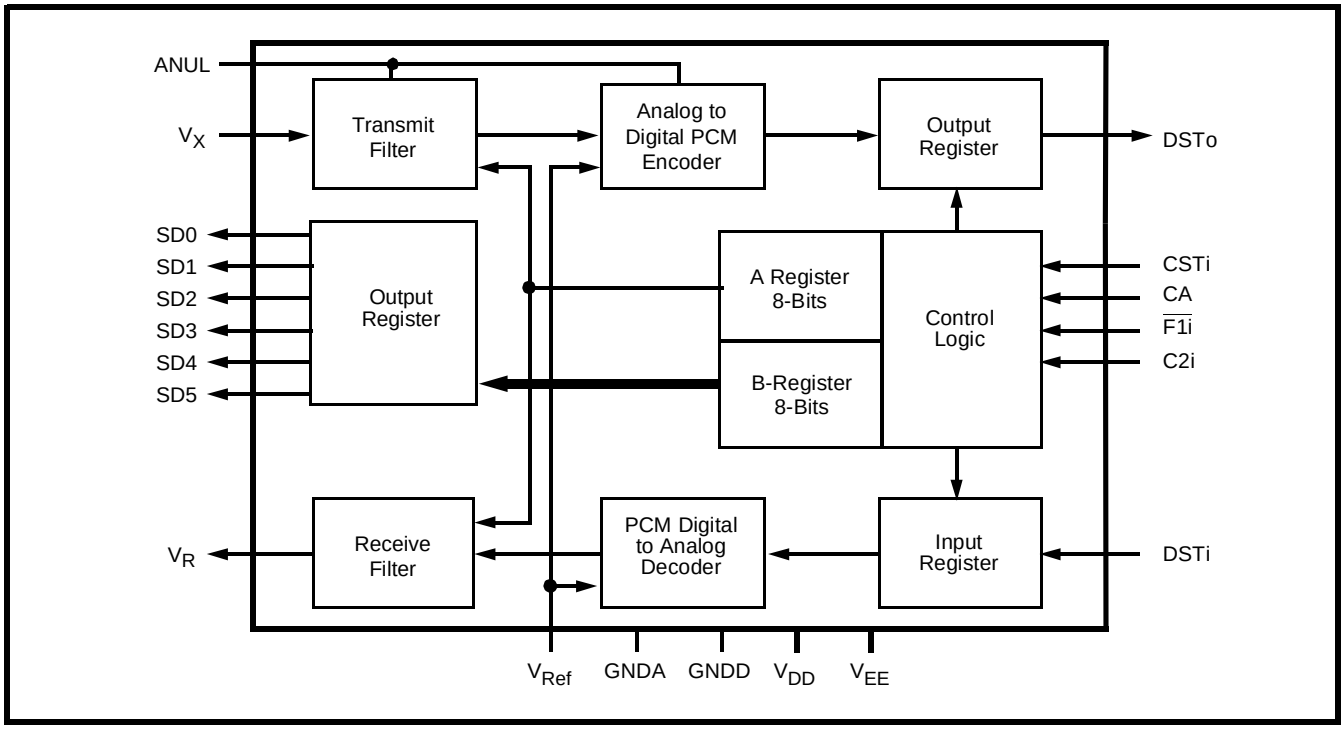


Figure 1 - Functional Block Diagram

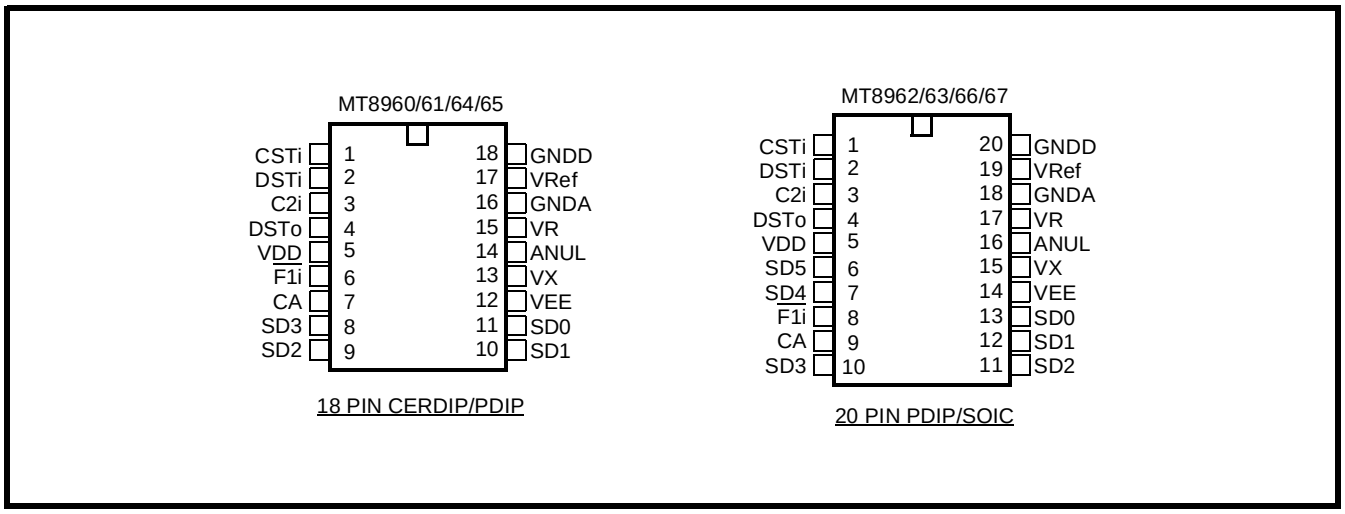


Figure 2 - Pin Connections

Pin Description

Pin Name	Description
CSTi	**Control ST-BUS In** is a TTL-compatible digital input used to control the function of the filter/codec. Three modes of operation may be effected by applying to this input a logic high (V_{DD}), logic low (GNDD), or an 8-bit serial word, depending on the logic states of CA and $\overline{F1i}$. Functions controlled are: powerdown, filter gain adjust, loopback, chip testing, SD outputs.
DSTi	**Data ST-BUS In** accepts the incoming 8-bit PCM word. Input is TTL-compatible.
C2i	**Clock Input** is a TTL-compatible 2.048 MHz clock.
DSTo	**Data ST-BUS Out** is a three-state digital output driving the PCM bus with the outgoing 8-bit PCM word.
V_{DD}	**Positive power Supply** (+5V).
$\overline{F1i}$	**Synchronization Input** is an active low digital input enabling (in conjunction with CA) the PCM input, PCM output and digital control input. It is internally sampled on every positive edge of the clock, C2i, and provides frame and channel synchronization.
CA	**Control Address** is a three-level digital input which enables PCM input and output and determines into which control register (A or B) the serial data, presented to CSTi, is stored.
SD3	**System Drive Output** is an open drain output of an N-channel transistor which has its source tied to GNDA. Inactive state is open circuit.
SD4-5	**System Drive Outputs** are open drain outputs of N-channel transistors which have their source tied to GNDD. Inactive state is open circuit.
SD0-2	**System Drive Outputs** are “Totempole“ CMOS outputs switching between GNDD and V_{DD}. Inactive state is logic low.
V_{EE}	**Negative power supply** (-5V).
V_X	**Voice Transmit** is the analog input to the transmit filter.
ANUL	**Auto Null** is used to integrate an internal auto-null signal. A 0.1µF capacitor must be connected between this pin and GNDA.
V_R	**Voice Receive** is the analog output of the receive filter.
GNDA	**Analog ground** (0V).
V_{Ref}	**Voltage Reference** input to D to A converter.
GNDD	**Digital ground** (0V).

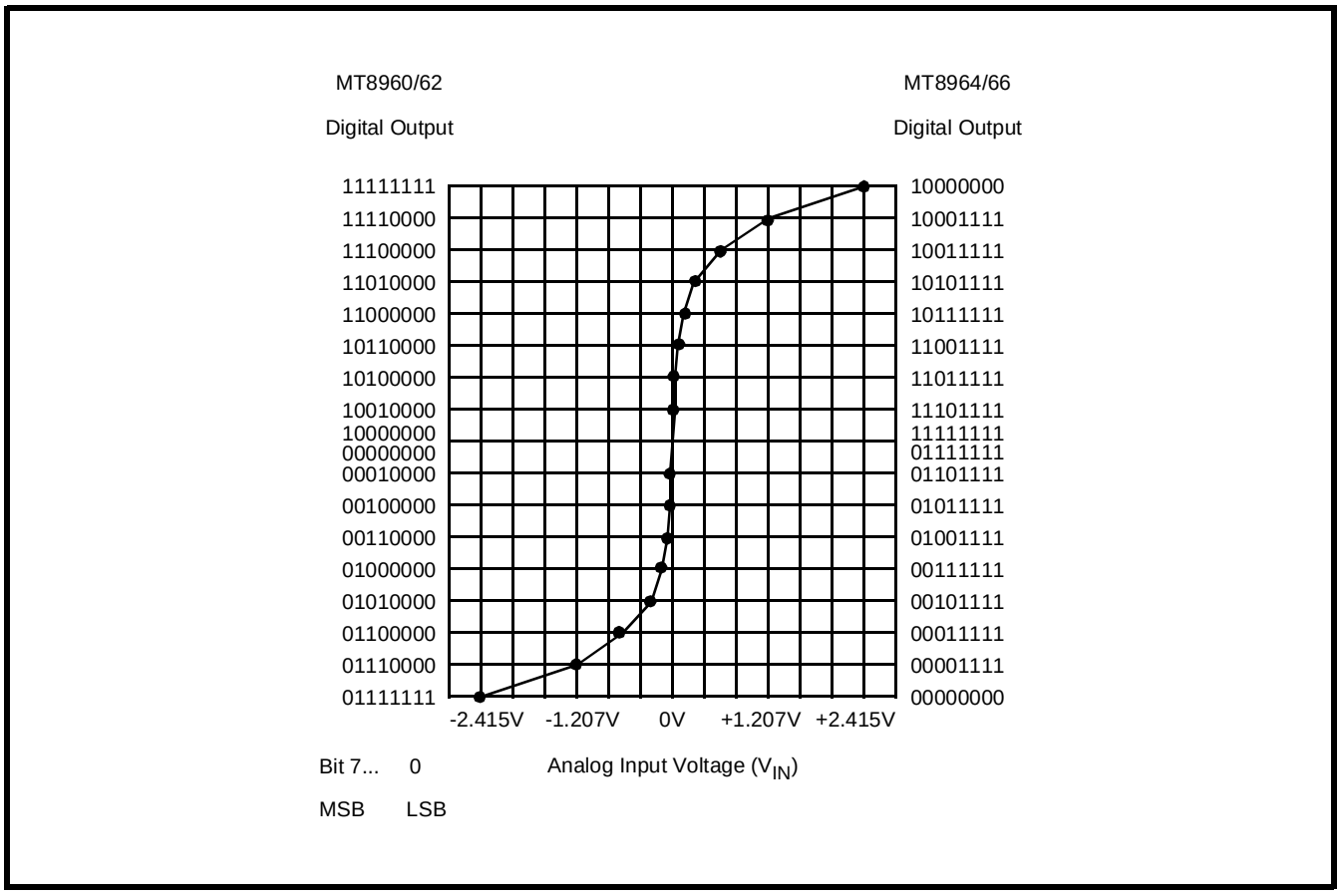


Figure 3 - μ-Law Encoder Transfer Characteristic

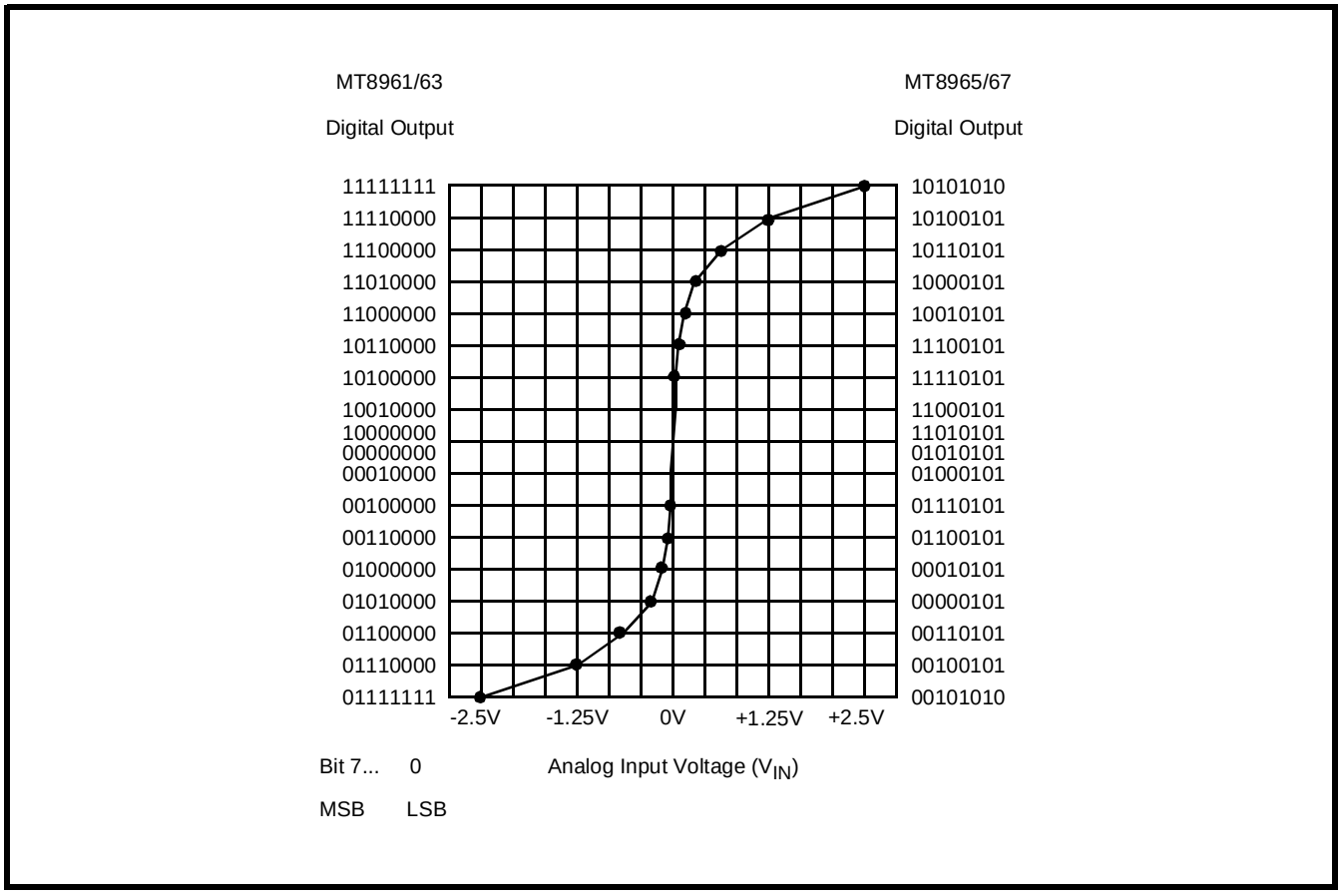


Figure 4 - A-Law Encoder Transfer Characteristic

Functional Description

Figure 1 shows the functional block diagram of the MT8960-67. These devices provide the conversion interface between the voiceband analog signals of a telephone subscriber loop and the digital signals required in a digital PCM (pulse code modulation) switching system. Analog (voiceband) signals in the transmit path enter the chip at V_X, are sampled at 8kHz, and the samples quantized and assigned 8-bit digital values defined by logarithmic PCM encoding laws. Analog signals in the receive path leave the chip at V_R after reconstruction from digital 8-bit words.

Separate switched capacitor filter sections are used for bandlimiting prior to digital encoding in the transmit path and after digital decoding in the receive path. All filter clocks are derived from the 2.048 MHz master clock input, C2i. Chip size is minimized by the use of common circuitry performing the A to D and D to A conversion. A successive approximation technique is used with capacitor arrays to define the 16 steps and 8 chords in the signal conversion process. Eight-bit PCM encoded digital data enters and leaves the chip serially on DSTi and DSTo pins, respectively.

Transmit Path

Analog signals at the input (Vx) are firstly bandlimited to 508 kHz by an RC lowpass filter section. This performs the necessary anti-aliasing for the following first-order sampled data lowpass pre-filter which is clocked at 512 kHz. This further bandlimits the signal to 124 kHz before a fifth-order elliptic lowpass filter, clocked at 128 kHz, provides the 3.4 kHz bandwidth required by the encoder section. A 50/60 Hz third-order highpass notch filter clocked at 8 kHz completes the transmit filter path. Accumulated DC offset is cancelled in this last section by a switched-capacitor auto-zero loop which integrates the sign bit of the encoded PCM word, fed back from the codec and injects this voltage level into the non-inverting input of the comparator. An integrating capacitor (of value between 0.1 and 1 µF) must be externally connected from this point (ANUL) to the Analog Ground (GNDA).

The absolute gain of the transmit filter (nominally 0 dB at 1 kHz) can be adjusted from 0 dB to 7 dB in 1 dB steps by means of three binary controlled gain pads.

The resulting bandpass characteristics with the limits shown in Figure 10 meet the CCITT and AT&T recommended specifications. Typical atttenuations are 30 dB for 0-60 Hz and 35 dB for 4.6 kHz and above.

The filter output signal is an 8 kHz staircase waveform which is fed into the codec capacitor array, or alternatively, into an external capacitive load of 250 pF when the chip is in the test mode. The digital encoder generates an eight-bit digital word representation of the 8 kHz sampled analog signal. The first bit of serial data stream is bit 7 (MSB) and represents the sign of the analog signal. Bits 4-6 represent the chord which contains the analog sample value. Bits 0-3 represent the step value of the analog sample within the selected chord. The MT8960-63 provide a sign plus magnitude PCM output code format. The MT8964/66 PCM output code conforms to the AT &T D3 specification, i.e., true sign bit and inverted magnitude bits. The MT8965/67 PCM output code conforms to the CCITT specifications with alternate digit inversion (even bits inverted). See Figs. 3 and 4 for the digital output code corresponding to the analog voltage, V_{IN}, at V_X input.

The eight-bit digital word is output at DSTo at a nominal rate of 2.048 MHz, via the output buffer as the first 8-bits of the 125 µs sampling frame.

Receive Path

An eight-bit PCM encoded digital word is received on DSTi input once during the 125 µs period and is loaded into the input register. A charge proportional to the received PCM word appears on the capacitor array and an 8 kHz sample and hold circuit integrates this charge and holds it for the rest of the sampling period.

The receive (D/A) filter provides interpolation filtering on the 8 kHz sample and hold signal from the codec. The filter consists of a 3.4 kHz lowpass fifth-order elliptic section clocked at 128 kHz and performs bandlimiting and smoothing of the 8 kHz "staircase" waveform. In addition, sinx/x gain correction is applied to the signal to compensate for the attenuation of higher frequencies caused by the capacitive sample and hold circuit. The absolute gain of the receive filter can be adjusted from 0 dB to -7 dB in 1 dB steps by means of three binary controlled gain pads. The resulting lowpass characteristics, with the limits shown in Figure 11, meet the CCITT and AT & T recommended specifications.

Typical attenuation at 4.6 kHz and above is 30 dB. The filter is followed by a buffer amplifier which will drive 5V peak/peak into a 10k ohm load, suitable for driving electronic 2-4 wire circuits.

V_{Ref}

An external voltage must be supplied to the V_{Ref} pin which provides the reference voltage for the digital encoding and decoding of the analog signal. For V_{Ref} = 2.5V, the digital encode decision value for overload (maximum analog signal detect level) is equal to an analog input V_{IN} = 2.415V (µ-Law version) or 2.5V (A-Law version) and is equivalent to a signal level of 3.17 dBm0 or 3.14 dBm0 respectively, at the codec.

The analog output voltage from the decoder at V_R is defined as:

µ-Law:

$$V_{Ref} \times \left[\left(\frac{-0.5}{128}\right)+\left(\frac{2^C}{128}\right)\left(\frac{16.5+S}{33}\right)\right] \pm V_{OFFSET}$$

A-Law:

$$V_{Ref} \times \left[\left(\frac{2^{C+1}}{128}\right)\left(\frac{0.5+S}{32}\right)\right] \pm V_{OFFSET} C=0$$

$$V_{Ref} \times \left[\left(\frac{2^C}{128}\right)\left(\frac{16.5+S}{32}\right)\right] \pm V_{OFFSET} C\neq 0$$

where C = chord number (0-7)

S = step number (0-15)

V_{Ref} is a high impedance input with a varying capacitive load of up to 40 pF.

The recommended reference voltage for the MT8960 series of codecs is 2.5V ±0.5%. The output voltage from the reference source should have a maximum temperature coefficient of 100 ppm/C°. This voltage should have a total regulation tolerance of ±0.5% both for changes in the input voltage and output loading of the voltage reference source. A voltage reference circuit capable of meeting these specifications is shown in Figure 5. Analog Devices 'AD1403A voltage reference circuit is capable of driving a large number of codecs due to the high input impedance of the V_{Ref} input. Normal precautions should be taken in PCB layout design to minimize noise coupling to this pin. A 0.1 µF capacitor connected from V_{Ref} to ground and located as close as possible to the codec is recommended to minimize noise entering through V_{Ref}. This capacitor should have good high frequency characteristics.

Timing

The codec operates in a synchronous manner (see Figure 9a). The codec is activated on the first positive edge of C2i after $\overline{F1i}$ has gone low. The digital output at DSTo (which is a three-state output driver) will then change from a high impedance state to the sign bit of the encoded PCM word to be output. This will remain valid until the next positive edge, when the next most significant bit will be output.

On the first negative clock edge (after $\overline{F1i}$ signal has been internally synchronized and CA is at GNDD or V_{EE}) the logic signal present at DSTi will be clocked into the input shift register as the sign bit of the incoming PCM word.

The eight-bit word is thus input at DSTi on negative edges of C2i and output at DSTo on positive edges of C2i.

$\overline{F1i}$ must return to a high level after the eighth clock pulse causing DSTo to enter high impedance and preventing further input data to DSTi. $\overline{F1i}$ will continue to be sampled on every positive edge of C2i. (Note: $\overline{F1i}$ may subsequently be taken low during the same sampling frame to enable entry of serial data into CSTi. This occurs usually mid-frame, in conjunction with CA=V_{DD}, in order to enter an 8-bit control word into Register B. In this case, PCM input and output are inhibited by CA at V_{DD}.)

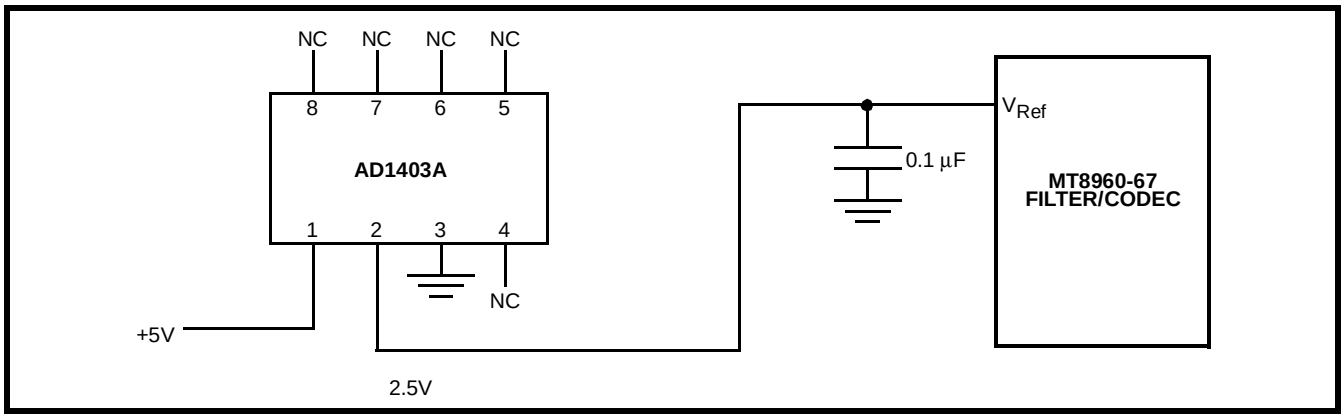


Figure 5 - Typical Voltage Reference Circuit

Internally the codec will then perform a decode cycle on the newly input PCM word. The sampled and held analog signal thus decoded will be updated 25 µs from the start of the cycle. After this the analog input from the filter is sampled for 18 µs, after which digital conversion takes place during the remaining 82 µs of the sampling cycle.

Since a single clock frequency of 2.048 MHz is required, all digital data is input and output at this rate. DSTo, therefore, assumes a high impedance state for all but 3.9 µs of the 125 µs frame. Similarly, DSTi input data is valid for only 3.9 µs.

Digital Control Functions

CSTi is a digital input (levels GNDD to V_{DD}) which is used to control the function of the filter/codec. It operates in three different modes depending on the logic levels applied to the Control Address input (CA) and chip enable input ($\overline{F1i}$) (see Table 1).

Mode 1

CA=-5V (V_{EE}); CSTi=0V (GNDD)

The filter/codec is in normal operation with nominal transmit and receive gain of 0dB. The SD outputs are in their active states and the test modes cannot be entered.

CA = -5V (V_{EE}); CSTi = +5V (V_{DD})

A state of powerdown is forced upon the chip whereby DSTo becomes high impedance, V_R is connected to GNDA and all analog sections have power removed.

Mode 2

CA= -5V (V_{EE}); CSTi receives an eight-bit control word

CSTi accepts a serial data stream synchronously with DSTi (i.e., it accepts an eight-bit serial word in a 3.9 µs timeslot, updated every 125 µs, and is specified identically to DSTi for timing considerations). This eight-bit control word is entered into Control Register A and enables programming of the following functions: transmit and receive gain, powerdown, loopback. Register B is reset to zero and the SD outputs assume their inactive state. Test modes cannot be entered.

Mode 3

CA=0V (GNDD); CSTi receives an eight-bit control word

As in Mode 2, the control word enters Register A and the aforementioned functions are controlled. In this mode, however, Register B is not reset, thus not affecting the states of the SD outputs.

CA=+5V (V_{DD}); CSTi receives an 8-bit control word

In this case the control word is transferred into Register B. Register A is unaffected. The input and output of PCM data is inhibited.

The contents of Register B controls the six uncommitted outputs SD0-SD5 (four outputs, SD0-SD3, on MT8960/61/64/65 versions of chip) and also provide entry into one of the three test modes of the chip.

MODE	CA	CSTi	FUNCTION
1 (Note 1)	V_{EE}	GNDD	Normal chip operation.
		V_{DD}	Powerdown.
2	V_{EE}	Serial Data	Eight-bit control word into Register A. Register B is reset.
3 (Note 2)	GNDD	Serial Data	Eight-bit control word into register A. Register B is unaffected.
	V_{DD}	Serial Data	Eight-bit control word into register A. Register B is unaffected.
Note 1:	When operating in Mode 1, there should be only one frame pulse ($\overline{F1i}$) per 125µs frame		
Note 2:	When operating in Mode 3, PCM input and output is inhibited by CA=V_{DD}.		

Table 1. Digital Control Modes

Note: For Modes 1 and 2, $\overline{F1i}$ must be at logic low for one period of 3.9 µs, in each 125 µs cycle, when PCM data is being input and output, and the control word at CSTi enters Register A. For Mode 3, $\overline{F1i}$ must be at a logic low for two periods of 3.9 µs, in each 125 µs cycle. In the first period, CA must be at GNDD or V_{EE}, and in the second period CA must be high (V_{DD}).

Control Registers A, B

The contents of these registers control the filter/codec functions as described in Tables 2 and 3.

Bit 7 of the registers is the MSB and is defined as the first bit of the serial data stream input (corresponding to the sign bit of the PCM word).

On initial power-up these registers are set to the powerdown condition for a maximum of 25 clock cycles. During this time it is impossible to change the data in these registers.

Chip Testing

By enabling Register B with valid data (eight-bit control word input to CSTi when $\overline{F1i}$=GNDD and CA= V_{CC}) the chip testing mode can be entered. Bits 6 and 7 (most sign bits) define states for testing the transmit filter, receive filter and the codec function. The input in each case is V_X input and the output in each case is V_R output. (See Table 3 for details.)

Loopback

Loopback of the filter/codec is controlled by the control word entered into Register A. Bits 6 and 7 (most sign bits) provide either a digital or analog loopback condition. Digital loopback is defined as follows:

- PCM input data at DSTi is latched into the PCM input register and the output of this register is connected to the input of the 3-state PCM output register.
- The digital input to the PCM digital-to-analog decoder is disconnected, forced to zero (0).
- The output of the PCM encoder is disabled and thus the encoded data is lost. The PCM output at DSTo is determined by the PCM input data.

Analog loopback is defined as follows:

- PCM input data is latched, decoded and filtered as normal but not output at V_R.
- Analog output buffer at V_R has its input shorted to GNDA and disconnected from the receive filter output.
- Analog input at V_X is disconnected from the transmit filter input.
- The receive filter output is connected to the transmit filter input. Thus the decode signal is fed back through the receive path and encoded in the normal way. The analog output buffer at V_R is not tested by this configuration.

In both cases of loopback, DSTi is the input and DSTo is the output.

BIT 2	BIT 1	BIT 0	TRANSMIT (A/D) FILTER GAIN (dB)
0	0	0	0
0	0	1	+ 1
0	1	0	+ 2
0	1	1	+ 3
1	0	0	+ 4
1	0	1	+ 5
1	1	0	+ 6
1	1	1	+ 7
BIT 5	**BIT 4**	**BIT 3**	**RECEIVE (D/A) FILTER GAIN (dB)**
0	0	0	0
0	0	1	- 1
0	1	0	- 2
0	1	1	- 3
1	0	0	- 4
1	0	1	- 5
1	1	0	- 6
1	1	1	- 7
BIT 7	**BIT 6**	**FUNCTION CONTROL**	
0	0	Normal operation	
0	1	Digital Loopback	
1	0	Analog Loopback	
1	1	Powerdown	

Table 2. Control States - Register A

Logic Control Outputs SD0-5

These outputs are directly controlled by the logic states of bits 0-5 in Register B. A logic low (GNDD) in Register B causes the SD outputs to assume an inactive state. A logic high (V_{DD}) in Register B causes the SD outputs to assume an active state (see Table 3). SD0-2 switch between GNDD and V_{DD} and may be used to control external logic or transistor circuitry, for example, that employed on the line card for performing such functions as relay drive for application of ringing to line, message waiting indication, etc.

SD3-5 are used primarily to drive external analog circuitry. Examples may include the switching in or out of gain sections or filter sections (eg., ring trip filter) (Figure 7).

MT8962/63/66/67 provides all six SD outputs.

MT8960/61/64/65 each packaged in an 18-pin DIP provide only four control outputs, SD0-3.

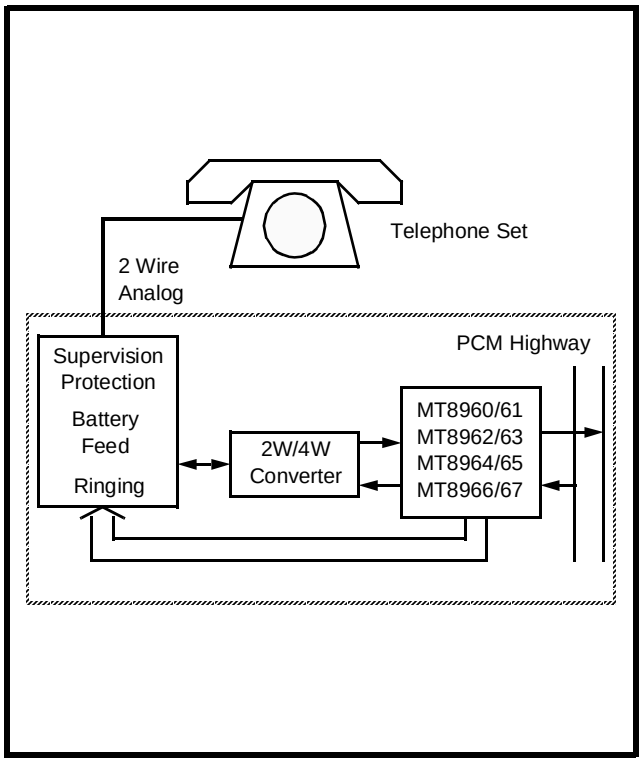


Figure 6 - Typical Line Termination

BITS 0-2		LOGIC CONTROL OUTPUTS SD_0-SD_2
0		Inactive state - logic low (GNDD).
1		Active state - logic high (V_{DD}).
BIT 3		**LOGIC CONTROL OUTPUT SD_3**
0		Inactive state - High Impedance.
1		Active state - GNDA.
BITS 4,5		**LOGIC CONTROL OUTPUTS SD_4, SD_5**
0		Inactive state - High Impedance.
1		Active state - GNDD.
BIT 7	**BIT 6**	**CHIP TESTING CONTROLS**
0	0	Normal operation.
0	1	Transmit filter testing, i.e.: Transmit filter input connected to V_X input Receive filter and Buffer disconnected from V_R
1	0	Receive filter testing, i.e.: Receive filter input connected to V_X input Receive filter input disconnected from codec
1	1	Codec testing i.e.: Codec analog input connected to V_X Codec analog input disconnected from transmit filter output Codec analog output connected to V_R V_R disconnected from receive filter output

Table 3. Control States - Register B

Powerdown

Powerdown of the chip is achieved in several ways:

Internal Control:

1) Initial Power-up. Initial application of V_{DD} and V_{EE} causes powerdown for a period of 25 clock cycles and during this period the chip will accept input only from C2i. The B-register is reset to zero forcing SD0-5 to be inactive. Bits 0-5 of Register A (gain adjust bits) are forced to zero and bits 6 and 7 of Register A become logic high thus reinforcing the powerdown.

2) Loss of C2i. Powerdown is entered 10 to 40 µs after C2i has assumed a continuous logic high (V_{DD}). In this condition the chip will be in the same state as in (1) above.

   Note: If C2i stops at a continuous logic low (GNDD), the digital data and status is indeterminate.

External Control:

1) Register A. Powerdown is controlled by bits 6 and 7 (when both at logic high) of Register A which in turn receives its control word input via CSTi, when $\overline{F1i}$ is low and CA input is either at V_{EE} or GNDD. Power is removed from the filters and analog sections of the chip. The analog ouput buffer at V_R will be connected to GNDA. DSTo becomes high impedance and the clocks to the majority of the logic are stopped. SD outputs are unaffected and may be updated as normal.

2) CSTi Input. With CA at V_{EE} and CSTi held at continuous logic high the chip assumes the same state as described in External Control (1) above.

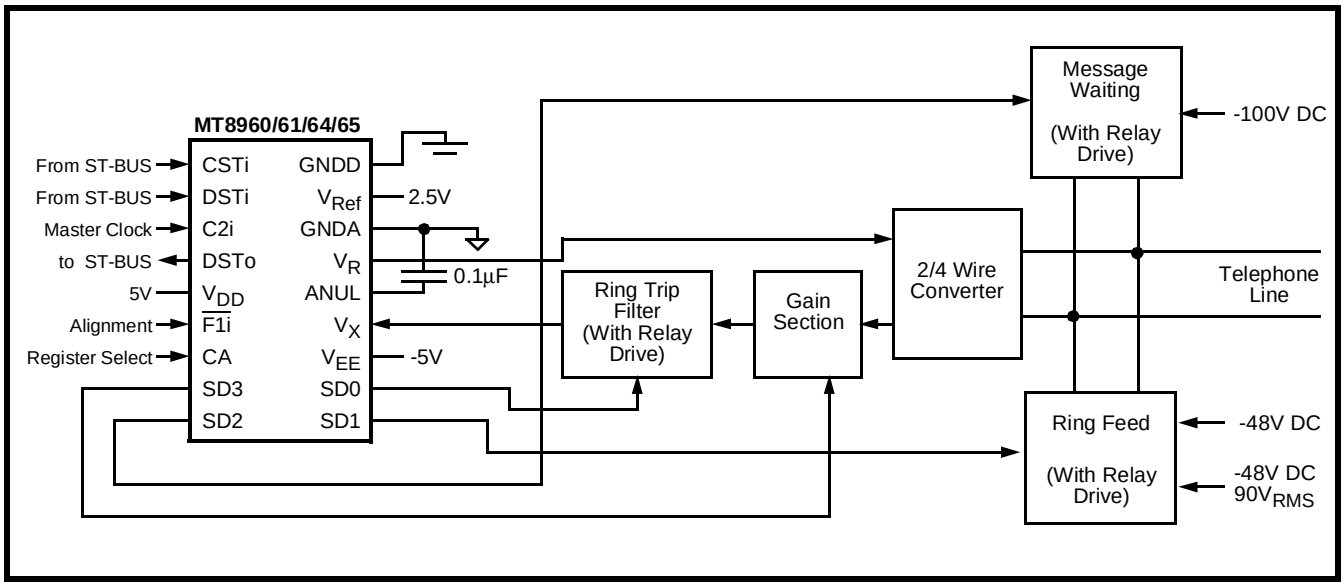


Figure 7 - Typical Use of the Special Drive Outputs

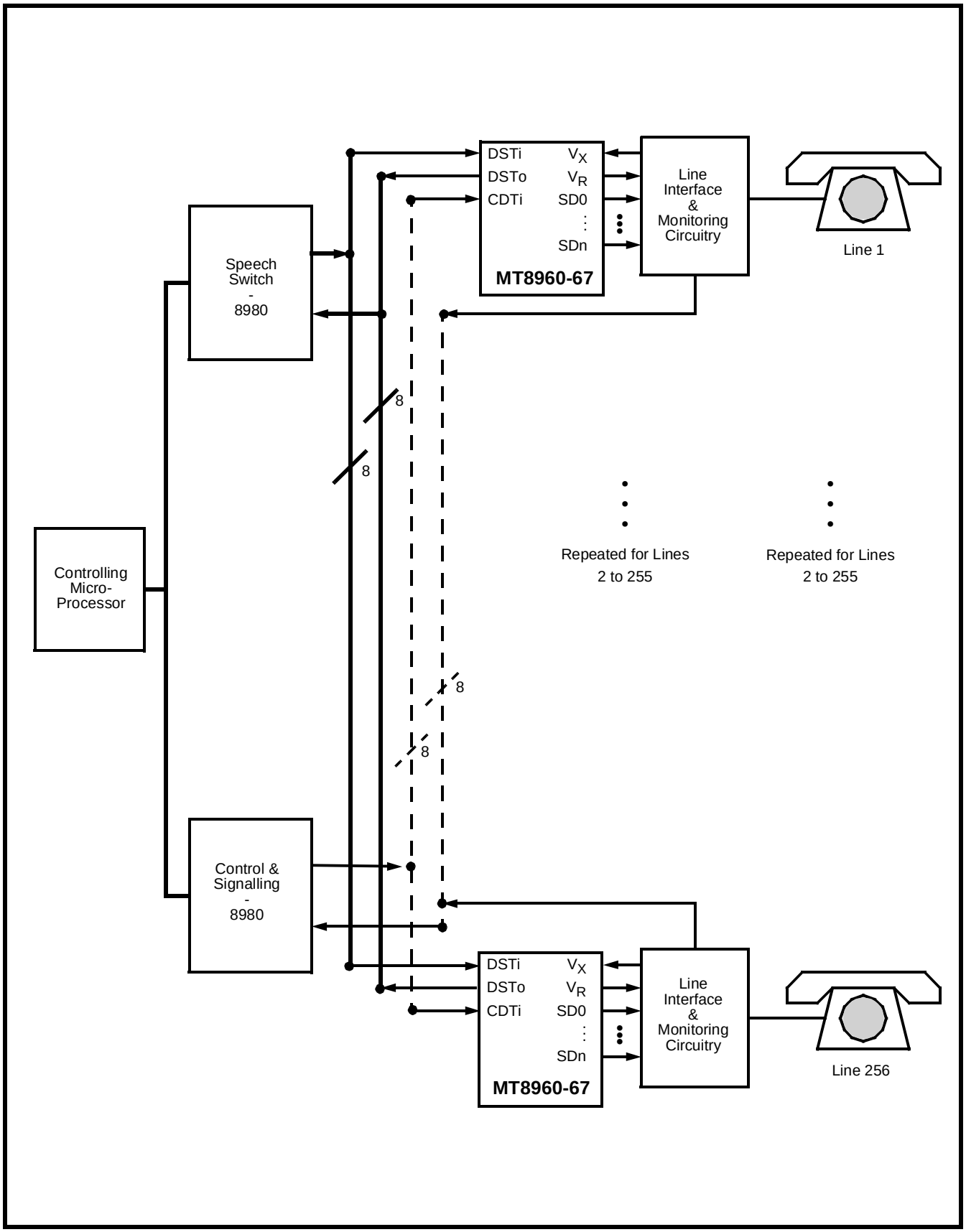


Figure 8 - Example Architecture of a Simple Digital Switching System Using the MT8960-67

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	DC Supply Voltages	V_{DD}-GNDD	-0.3	+6.0	V
		V_{EE}-GNDD	-6.0	+0.3	V
2	Reference Voltage	V_{Ref}	GNDA	V_{DD}	V
3	Analog Input	V_X	V_{EE}	V_{DD}	V
4	Digital Inputs	Except CA	GNDD-0.3	V_{DD}+0.3	V
		CA	V_{EE}-0.3	V_{DD}+0.3	V
5	Output Voltage	SD0-2	GNDD-0.3	V_{DD}+0.3	V
		SD3	V_{EE}-0.3	V_{DD}+0.3	V
		SD4-5	V_{EE}-0.3	V_{DD}+0.3	V
6	Current On Any Pin	I_I		20	mA
7	Storage Temperature	T_S	-55	+125	°C
8	Power Dissipation at 25°C (Derate 16 mW/°C above 75°C)	P_{Diss}		500	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to GNDD unless otherwise stated

		Characteristics	Sym	Min	Typ*	Max	Units	Comments
1		Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
			V_{EE}	-5.25	-5.0	-4.75	V	
			V_{Ref}		2.5		V	See Note 1
2		Voltage On Digital Ground	VGNDD	-0.1	0.0	+0.1	Vdc	Ref. to GNDA
				-0.4	0.0	+0.4	Vac	Ref. to GNDA 400ns max. duration in 125µs cycle
3		Operating Temperature	T_O	0		+70	°C	
4		Operating Current V_{DD} V_{EE}	I_{DD} I_{EE}		3.0 3.0	4.0 4.0	mA mA	All digital inputs at V_{DD} or GNDD (or V_{EE} for CA)
		V_{Ref}	I_{Ref}		2.0		µA	Mean current
5		Standby Current V_{DD} V_{EE}	I_{DDO} I_{EEO}		0.25 0.25	1.0 1.0	mA mA	All digital inputs at V_{DD} or GNDD (or V_{EE} for CA)

Note 1: Temperature coefficient of V_{Ref} should be better than 100 ppm/°C.

DC Electrical Characteristics - Voltages are with respect to GNDD unless otherwise stated.

T_A=0 to 70°C, V_{DD}=5V±5%, V_{EE}=-5V±5%, V_{Ref}=2.5V±0.5%, GNDA=GNDD=0V,Clock Frequency =2.048MHz. Outputs unloaded unless otherwise specified.

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1	DIGITAL	Input Current	Except CA	I_I			10.0	µA	V_{IN} = GNDD to V_{DD}
			CA	I_{IC}			10.0	µA	V_{IN} = V_{EE} to V_{DD}
2		Input Low Voltage	Except CA	V_{IL}	0.0		0.8	V	
			CA	V_{ILC}	V_{EE}		V_{EE}+1.2	V	
3		Input High Voltage	All Inputs	V_{IH}	2.4		5.0	V	
4		Input Intermediate Voltage	CA	V_{IIC}	0.0		0.8	V	
5		Output Leakage Current (Tristate)	DSTo SD3-5	I_{0Z}		±0.1	 10.0	µA µA	Output High Impedance

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics (cont'd)

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
6	DIGITAL	Output Low Voltage	DSTo	V_{OL}			0.4	V	I_{OUT} =1.6 mA
			SD0-2	V_{OL}			1.0	V	I_{OUT} =1 mA
7		Output High Voltage	DSTo	V_{OH}	4.0			V	I_{OUT} =-100µA
			SD0-2	V_{OH}	4.0			V	I_{OUT} =-1mA
8		Output Resistance	SD3-5	R_{OUT}		1.0	2.0	KΩ	V_{OUT} =+1V
9		Output Capacitance	DSTo	C_{OUT}		4.0		pF	Output High Impedance
10	ANALOG	Input Current	V_X	I_{IN}			10.0	µA	$V_{EE} \le V_{IN} \le V_{CC}$
11		Input Resistance	V_X	R_{IN}		10.0		MΩ	
12		Input Capacitance	V_X	C_{IN}		30.0		pF	f_{IN} = 0 - 4 kHz
13		Input Offset Voltage	V_X	V_{OSIN}		+1.0		mV	See Note 2
14		Output Resistance	V_R	R_{OUT}			100	Ω	
15		Output Offset Voltage	V_R	V_{OSOUT}			100	mV	Digital Input= +0

Note 2: V_{OSIN} specifies the DC component of the digitally encoded PCM word.

AC Electrical Characteristics - Voltages are with respect to GNDD unless otherwise stated.

T_A=0 to 70°C, V_{DD}=5V±5%, V_{EE}=-5V±5%, V_{Ref}=2.5V±0.5%, GNDA=GNDD=0V, Clock Frequency=2.048 MHz. Outputs unloaded unless otherwise specified.

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1	DIGITAL	Clock Frequency	C2i	f_C	2.046	2.048	2.05	MHz	See Note 3
2		Clock Rise Time	C2i	t_{CR}			50	ns	
3		Clock Fall Time	C2i	t_{CF}			50	ns	
4		Clock Duty Cycle	C2i		40	50	60	%	
5		Chip Enable Rise Time	$\overline{F1i}$	t_{ER}			100	ns	
6		Chip Enable Fall Time	$\overline{F1i}$	t_{EF}			100	ns	
7		Chip Enable Setup Time	$\overline{F1i}$	t_{ES}	50			ns	See Note 4
8		Chip Enable Hold Time	$\overline{F1i}$	t_{EH}	25			ns	See Note 4
9		Output Rise Time	DSTo	t_{OR}			100	ns	
10		Output Fall Time	DSTo	t_{OF}			100	ns	
11		Propagation Delay Clock to Output Enable	DSTo	t_{PZL} t_{PZH}			122 122	ns ns	R_L=10KΩ to V_{CC}
12		Propagation Delay Clock to Output	DSTo	t_{PLH} t_{PHL}			100 100	ns ns	C_L=100 pF
13		Input Rise Time	CSTi DSTi	t_{IR}			100 100	ns ns	
14		Input Fall Time	CSTi DSTi	t_{IF}			100 100	ns ns	
15		Input Setup Time	CSTi DSTi	t_{ISH} t_{ISL}	25 0			ns ns	
16		Input Hold Time	CSTi DSTi	t_{IH}	60 60			ns ns	

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics (cont'd)

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
17	DIGITAL	Propagation Delay SD Clock to SD Output	t_{PCS}			400	ns	C_L = 100 pF
18		SD Output Fall Time SD	t_{SF}			200	ns	C_L = 20 pF
19		SD Output Rise Time SD	t_{SR}			400	ns	
20		Digital Loopback Time DSTi to DSTo	t_{DL}			122	ns	

(See Figures 9a, 9b, 9c)

Note 3: The filter characteristics are totally dependent upon the accuracy of the clock frequency providing $\overline{F1i}$ is synchronized to C2i. The A/D and D/A functions are unaffected by changes in clock frequency.

Note 4: This gives a 75 ns period, 50 ns before and 25 ns after the 50% point of C2i rising edge, when change in $\overline{F1i}$ will give an undetermined state to to the internally synchronized enable signal.

AC Electrical Characteristics - Transmit (A/D) Path - Voltages are with respect to GNDD unless otherwise stated.

T_A=0 to 70°C, V_{DD}=5V±5%, V_{EE}=-5V±5%, V_{Ref}=2.5V±0.5%, GNDA=GNDD=0V, Clock Frequency = 2.048MHz, Filter Gain Setting = 0dB. Outputs unloaded unless otherwise specified.

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	ANALOG	Analog Input at V_X equivalent to the overload decision level at the codec	V_{IN}		4.829 5.000		V_{PP} V_{PP}	Level at codec: μ-Law: 3.17 dBm0 A-Law: 3.14 dBm0 See Note 6
2		Absolute Gain (0dB setting)	G_{AX}	-0.25		+0.25	dB	0 dBm0 @ 1004 Hz
3		Absolute Gain (+1dB to +7dB settings)		-0.35		+0.35	dB	from nominal, @ 1004 Hz
4		Gain Variation With Temp	G_{AXT}		0.01		dB	T_A=0°C to 70°C
		With Supplies	G_{AXS}		0.04		dB/V	
5		Gain Tracking (See Figure 12) CCITT G712 (Method 1)	GT_{X1}	-0.25 -0.25 -0.50		+0.25 +0.25 +0.50	dB dB dB	Sinusoidal Level: +3 to -20 dBm0 Noise Signal Level: -10 to -55 dBm0 -55 to -60 dBm0
		CCITT G712 (Method 2) AT&T	GT_{X2}	-0.25 -0.50 -1.50		+0.25 +0.50 +1.50	dB dB dB	Sinusoidal Level: +3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
6		Quantization Distortion (See Figure 13) CCITT G712 (Method 1)	D_{QX1}	28.00 35.60 33.90 29.30 14.20			dB dB dB dB dB	Noise Signal Level: -3 dBm0 -6 to -27 dBm0 -34 dBm0 -40 dBm0 -55 dBm0

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing.

Transmit (A/D) Path (cont'd)

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
	ANALOG	Quantization Distortion (cont'd) (See Figure 13)	CCITT G712 (Method 2) AT&T	D_{QX2}	 35.30 29.30 24.30			 dB dB dB	Sinusoidal Input Level: 0 to -30 dBm0 -40 dBm0 -45 dBm0
7		Idle Channel	C-message	N_{CX}			18	dBrnC0	μ-Law Only
		Noise	Psophometric	N_{PX}			-67	dBm0p	CCITT G712
8		Single Frequency Noise		N_{SFX}			-56	dBm0	CCITT G712
9		Harmonic Distortion (2nd or 3rd Harmonic)					-46	dB	Input Signal: 0 dBm0 @ 1.02 kHz
10		Envelope Delay		D_{AX}			270	μs	@ 1004 Hz
11		Envelope Delay Variation With Frequency	1000-2600 Hz 600-3000 Hz 400-3200 Hz	D_{DX}		60 150 250		μs μs μs	Input Signal: 400-3200 Hz Sinewave at 0 dBm0
12		Intermodulation Distortion	CCITT G712 50/60 Hz	IMD_{X1}			-55	dB	50/60 Hz @ -23 dBm0 and any signal within 300-3400 Hz at -9 dBm0
			CCITT G712 2 tone	IMD_{X2}			-41	dB	740 Hz and 1255 Hz @ -4 to -21 dBm0. Equal Input Levels
			AT&T	IMD_{X3}			-47	dB	2nd order products
			4 tone	IMD_{X4}			-49	dB	3rd order products
13		Gain Relative to Gain @ 1004 Hz (See Figure 10)	≤50 Hz 60 Hz 200 Hz 300-3000 Hz 3200 Hz 3300 Hz 3400 Hz 4000 Hz ≥4600 Hz	G_{RX}	 -1.8 -0.125 -0.275 -0.350 -0.80		-25 -30 0.00 0.125 0.125 0.030 -0.100 -14 -32	dB dB dB dB dB dB dB dB dB	0 dBm0 Input Signal Transmit Filter Response
14		Crosstalk D/A to A/D		CT_{RT}			-70	dB	0 dBm0 @ 1.02 kHz in D/A
15		Power Supply Rejection	V_{DD} V_{EE}	$PSSR_1$ $PSSR_2$	33 35			dB dB	Input 50 mV_{RMS} at 1.02 kHz
16		Overload Distortion (See Fig.15)							Input frequency=1.02kHz

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing.

Note 6: 0dBm0=1.185 V_{RMS} for the μ-Law codec.
0dBm0=1.231 V_{RMS} for the A-Law codec.

AC Electrical Characteristics - Receive (D/A) Path - Voltages are with respect to GNDD unless otherwise stated.

T_A=0 to 70°C, V_{DD}=5V±5%, V_{EE}=-5V±5%, V_{Ref}=2.5V±0.5%, GNDA=GNDD=0V, Clock Frequency = 2.048MHz,
Filter Gain Setting = 0dB. Outputs unloaded unless otherwise specified.

		Characteristics		Sym	Min	Typ*	Max	Units	Test Conditions
1	ANALOG	Analog output at V_R equivalent to the overload decision level at codec		V_{OUT}		4.829 5.000		V_{pp} V_{pp}	Level at codec: μ-Law: 3.17 dBm0 A-Law: 3.14 dBm0 R_L=10 KΩ See Note 7
2		Absolute Gain (0dB setting)		G_{AR}	-0.25		+0.25	dB	0 dBm0 @ 1004Hz
3		Absolute Attenuation (-1dB to -7dB settings)			-0.35		+0.35	dB	From nominal, @ 1004Hz
4		Gain Variation	With Temp.	G_{ART}		0.01		dB	T_A=0°C to 70°C
			With Supplies	G_{ARS}		0.04		dB/V	
5		Gain Tracking (See Figure 12)	CCITT G712 (Method 1)	GT_{R1}	-0.25 -0.25 -0.50		+0.25 +0.25 +0.50	dB dB dB	Sinusoidal Level: +3 to -10 dBm0 Noise Signal Level: -10 to -55 dBm0 -55 to -60 dBm0
			CCITT G712 (Method 2) AT & T	GT_{R2}	-0.25 -0.50 -1.50		+0.25 +0.50 +1.50	dB dB dB	Sinusoidal Level: +3 to -40 dBm0 -40 to -50 dBm0 -50 to -55 dBm0
6		Quantization Distortion (See Fig. 13)	CCITT G712 (Method 1)	D_{QR1}	28.00 35.60 33.90 29.30 14.30			dB dB dB dB dB	Noise Signal Level: -3 dBm0 -6 to -27 dBm0 -34 dBm0 -40 dBm0 -55 dBm0
			CCITT G712 (Method 2) AT & T	D_{QR2}	36.40 30.40 25.40			dB dB dB	Sinusoidal Input Level: 0 to -30 dBm0 -40 dBm0 -45 dBm0
7		Idle Channel	C-message	N_{CR}			12	dBrnC0	μ-Law Only
		Noise	Psophometric	N_{PR}			-75	dBm0p	CCITT G712
8		Single Frequency Noise		N_{SFR}			-56	dBm0	CCITT G712
9		Harmonic Distortion (2nd or 3rd Harmonic)					-46	dB	Input Signal 0 dBm0 at 1.02 kHz
10		Intermodulation Distortion	CCITT G712 2 tone	IMD_{R2}			-41	dB	
			AT & T	IMD_{R3}			-47	dB	2nd order products
			4 tone	IMD_{R4}			-49	dB	3rd order products

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing.

Receive (D/A) Path (cont'd)

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
11	ANALOG	Envelope Delay	D_{AR}			210	µs	@ 1004 Hz
12		Envelope Delay 1000-2600 Hz Variation with 600-3000 Hz Frequency 400-3200 Hz	D_{DR}		90 170 265		µs µs µs	Input Signal: 400 - 3200 Hz digital sinewave at 0 dBm0
13		Gain Relative to <200 Hz Gain @ 1004 Hz 200 Hz (See Figure 11) 300-3000 Hz 3300 Hz 3400 Hz 4000 Hz ≥4600 Hz	G_{RR}	 -0.5 -0.125 -0.350 -0.80		0.125 0.125 0.125 0.030 -0.100 -14.0 -28.0	dB dB dB dB dB dB dB	0 dBm0 Input Signal Receive Filter Response
14		Crosstalk A/D to D/A	CT_{TR}			-70	dB	0 dBm0 @ 1.02 kHz in A/D
15		Power Supply V_{DD} Rejection V_{EE}	$PSRR_3$ $PSRR_4$	33 35			dB dB	Input 50 mV_{RMS} at 1.02 kHz
16		Overload Distortion (See Fig. 15)						Input frequency=1.02 kHz

* Typical figures are at 25°C with nominal ±5V supplies. For design aid only: not guaranteed and not subject to production testing.
Note 7: 0dBm0=1.185 V_{RMS} for µ-Law codec and 0dBm0=1.231 V_{RMS} for A-Law codec.

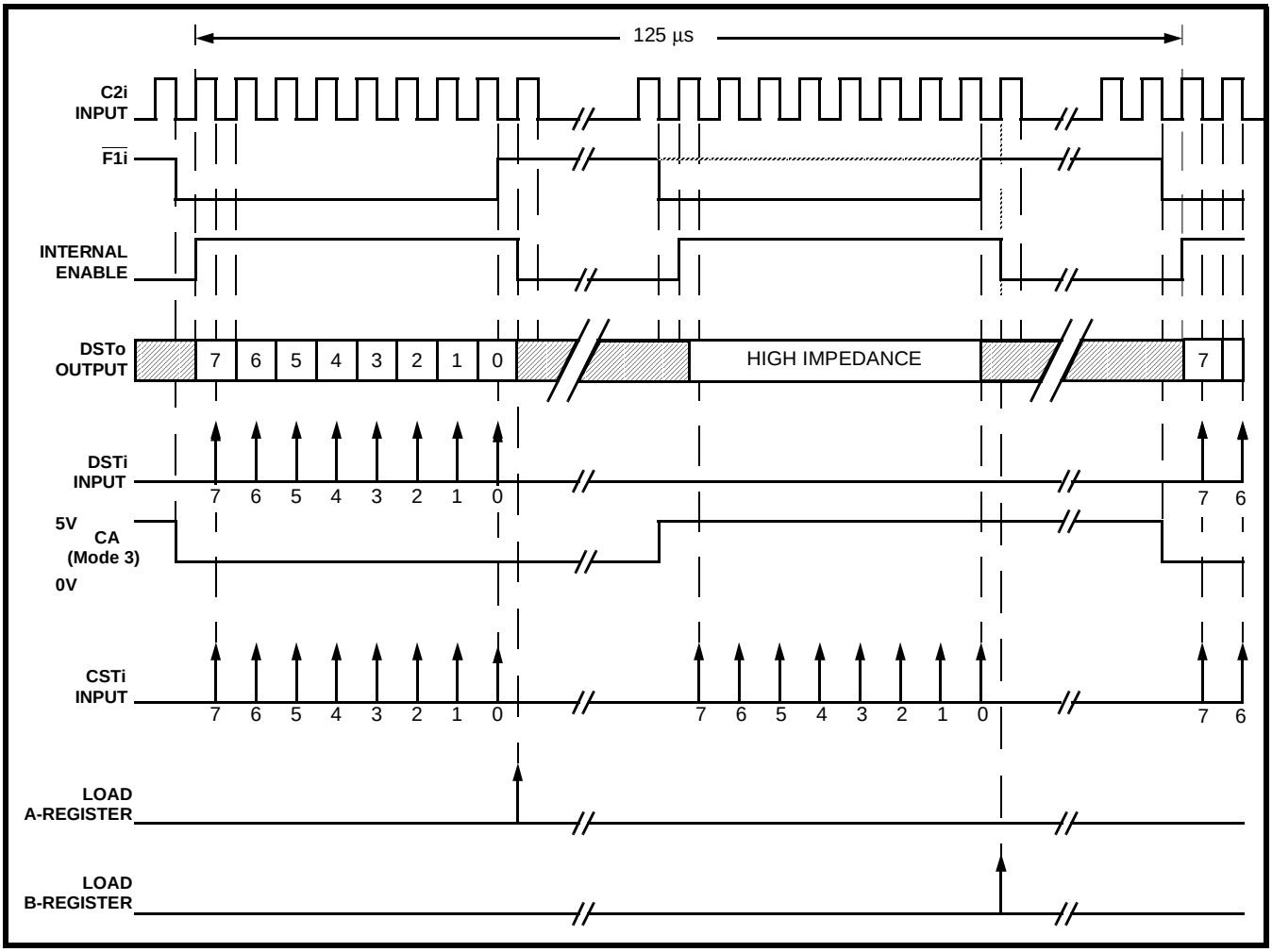


Figure 9a - Timing Diagram - 125µs Frame Period

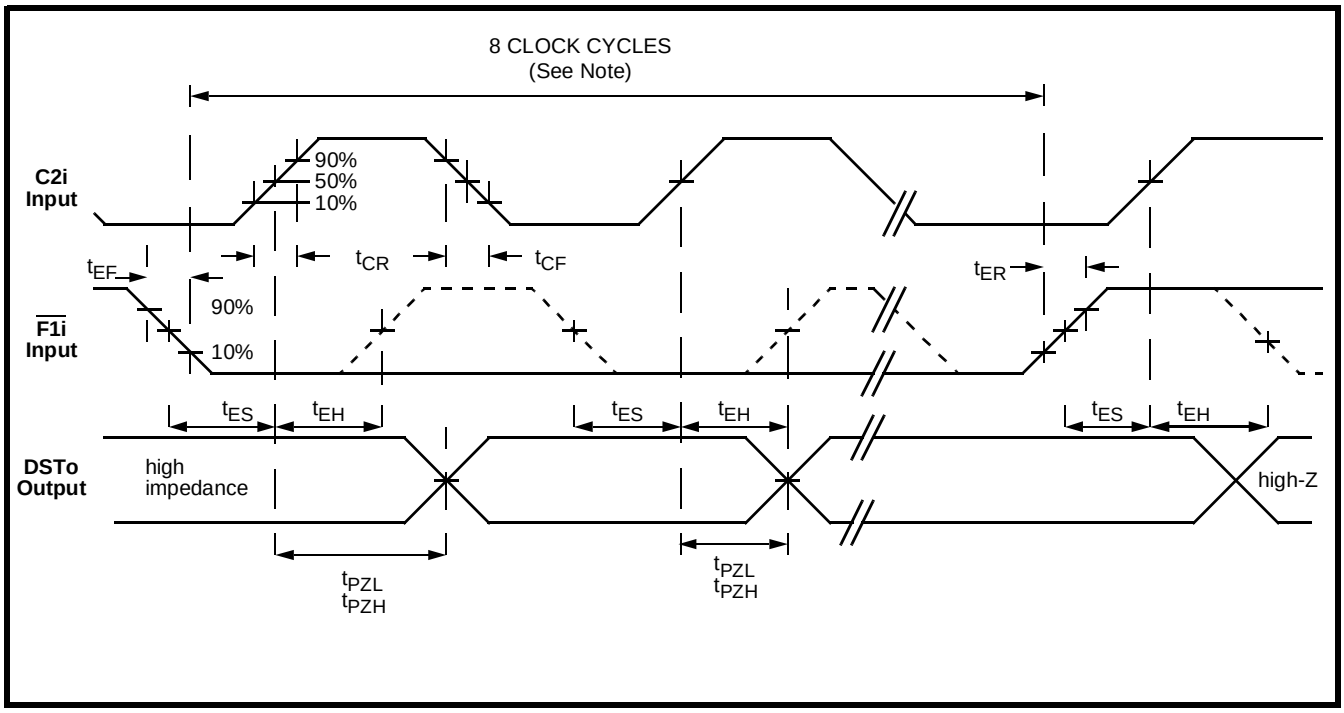


Figure 9b - Timing Diagram - Output Enable

Note: In typical applications, $\overline{F1i}$ will remain low for 8 cycles of C2i. However, the device will function normally as long as t_{ES} and t_{EH} are met at each positive edge of C2i.

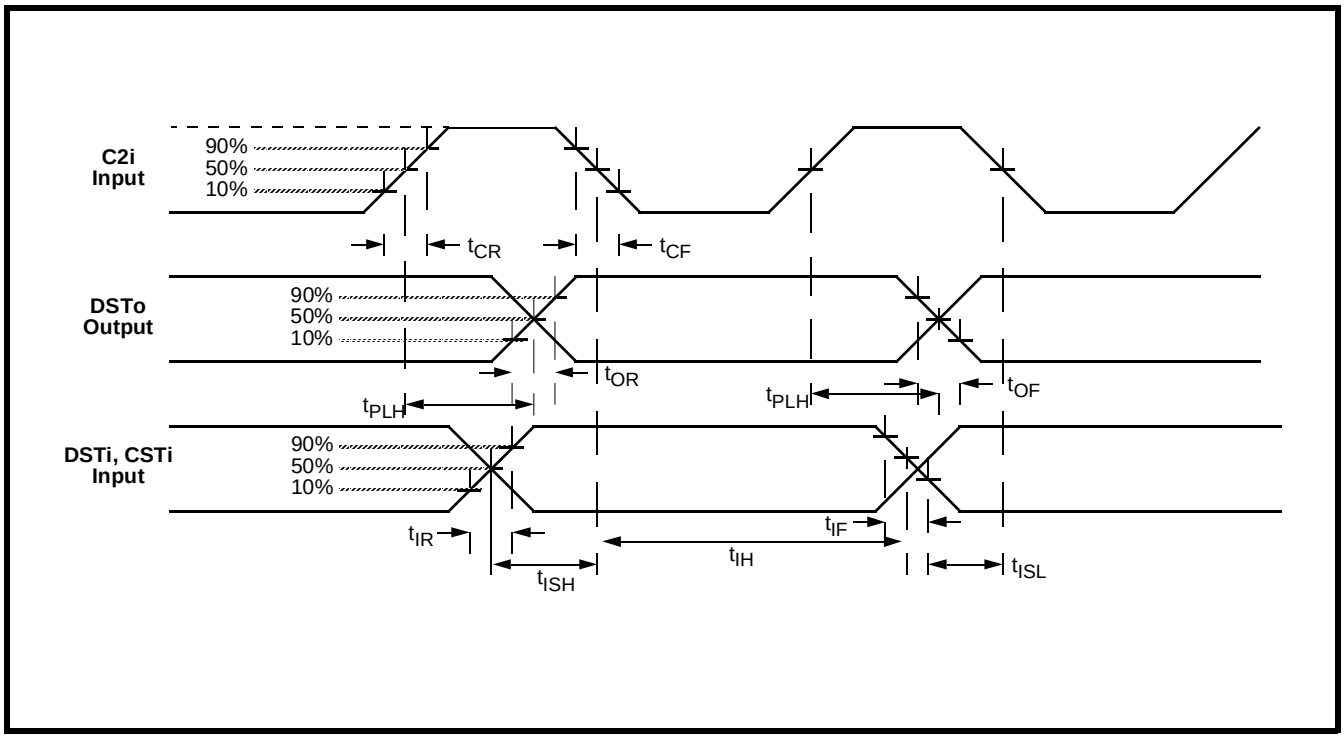


Figure 9c - Timing Diagram - Input/Output

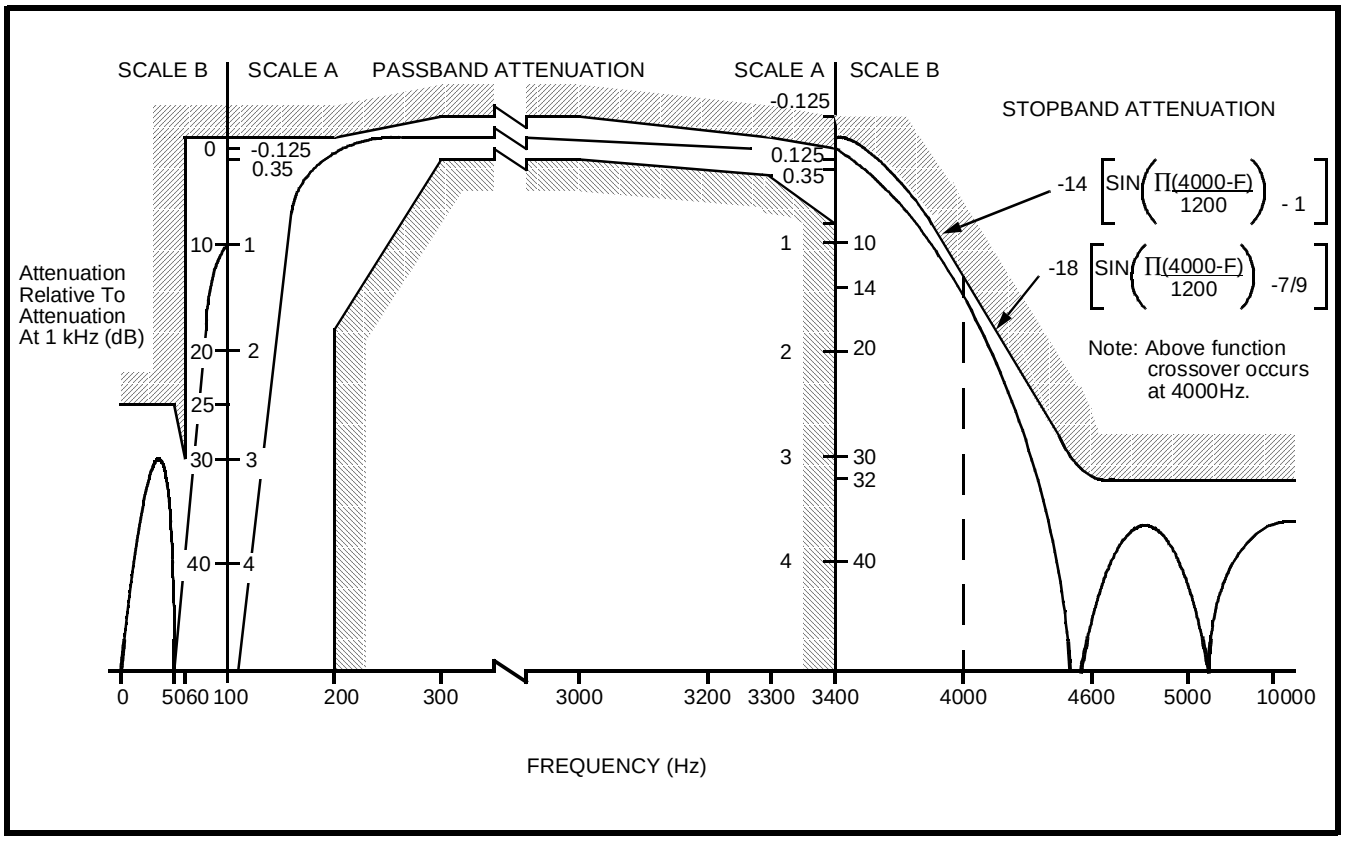


Figure 10 - Attenuation vs Frequency for Transmit (A/D) Filter

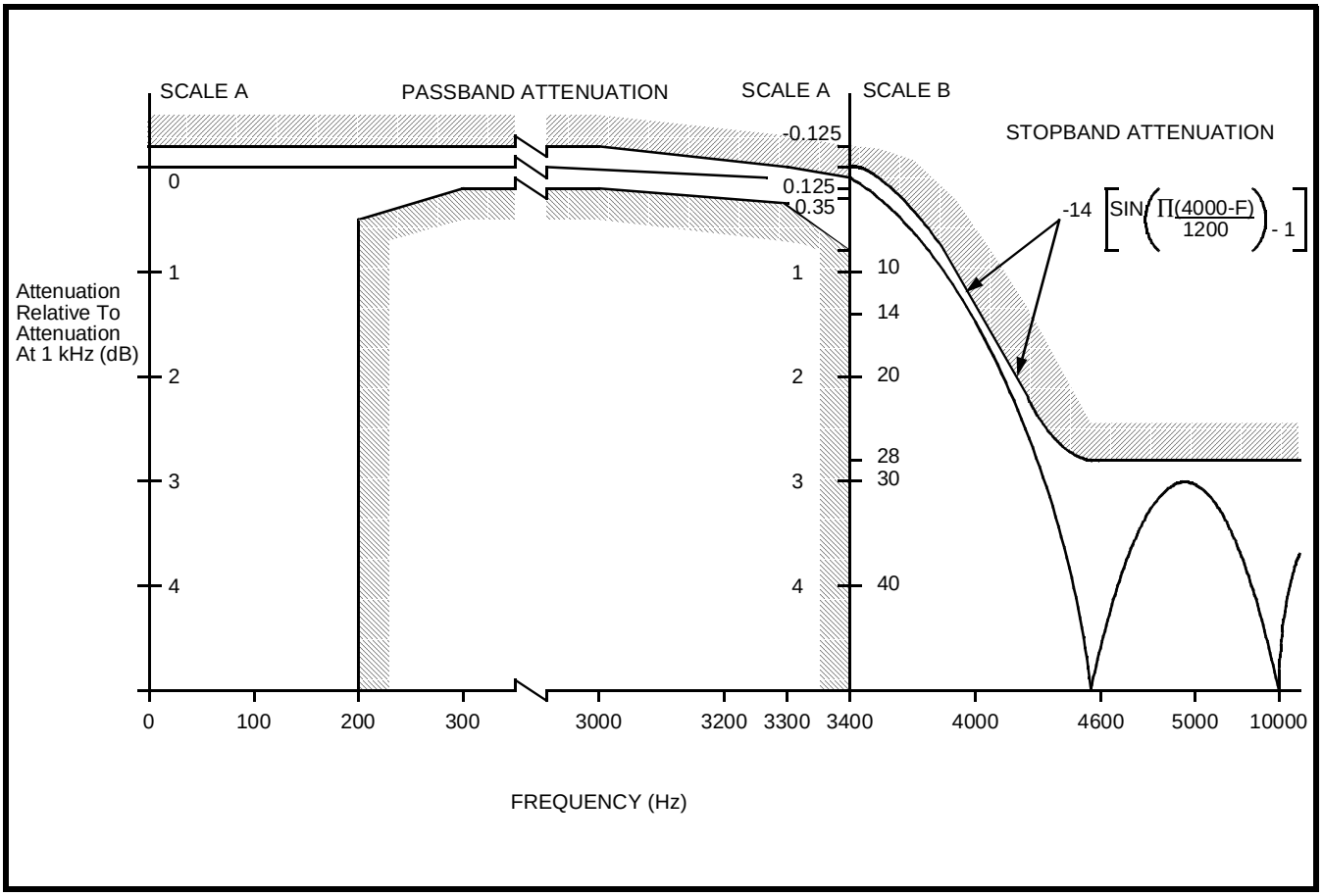


Figure 11 - Attenuation vs Frequency for Receive (D/A) Filter

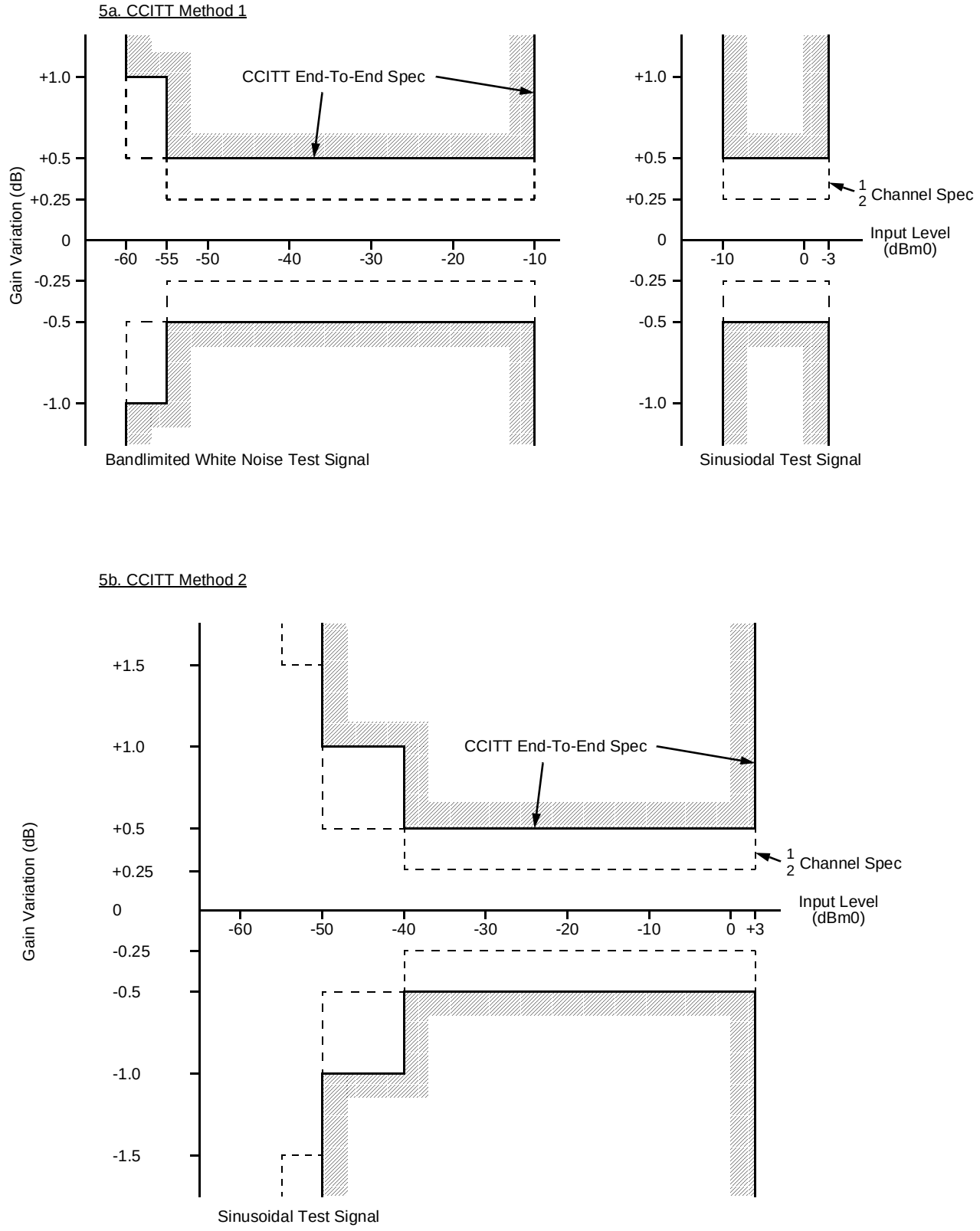


Figure 12 - Variation of Gain With Input Level

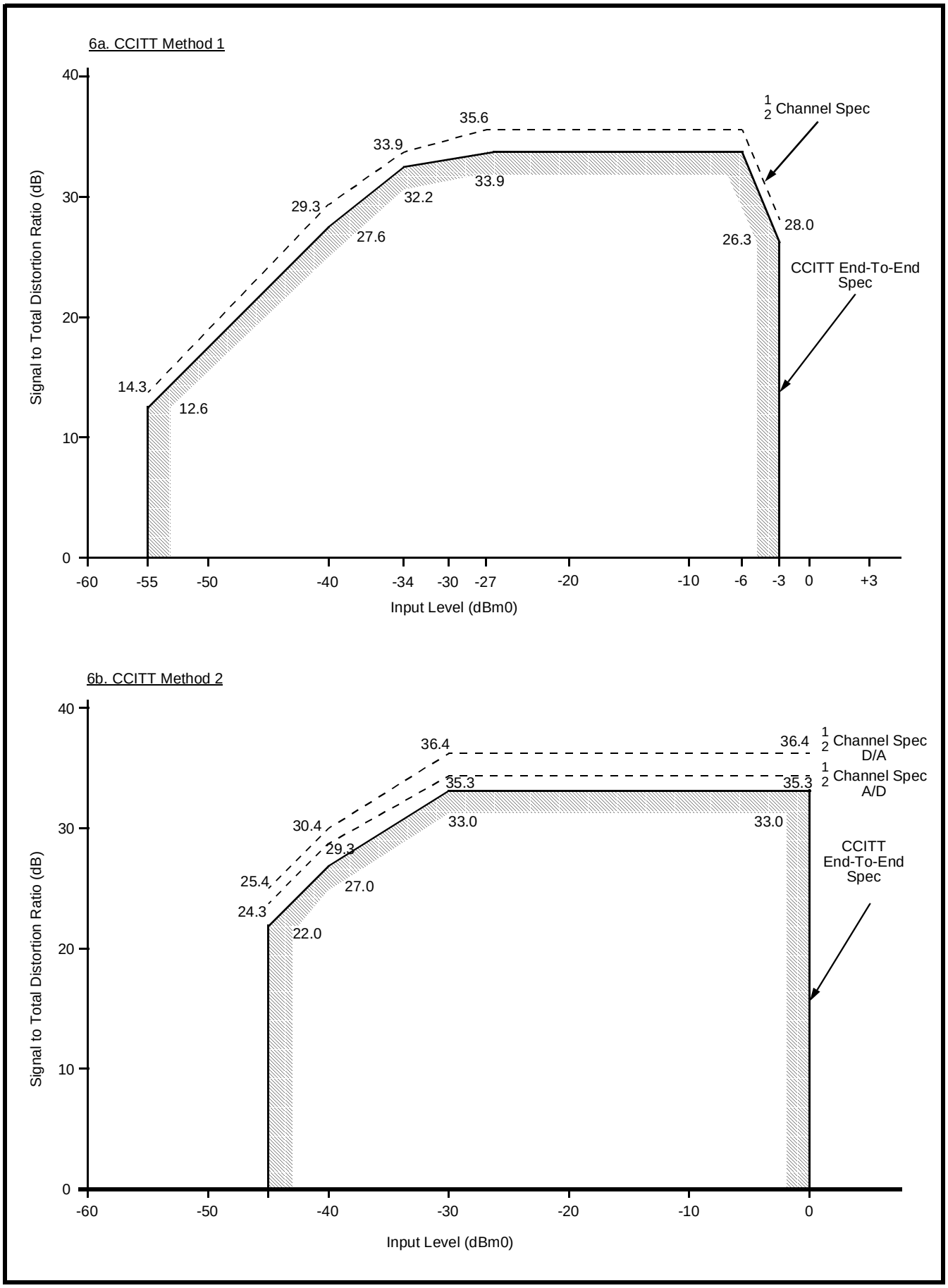


Figure 13 - Signal to Total Distortion Ratio vs Input Level

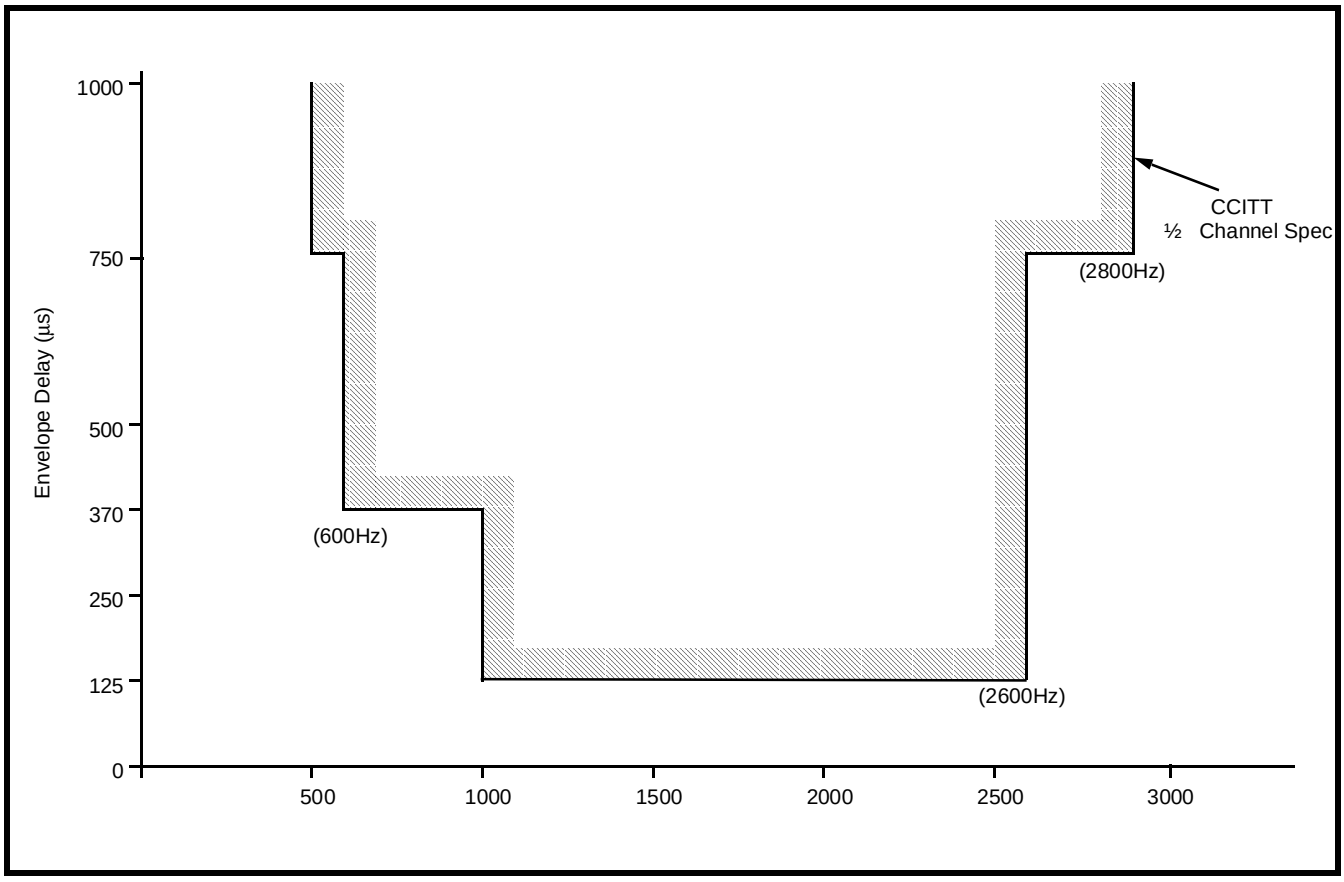
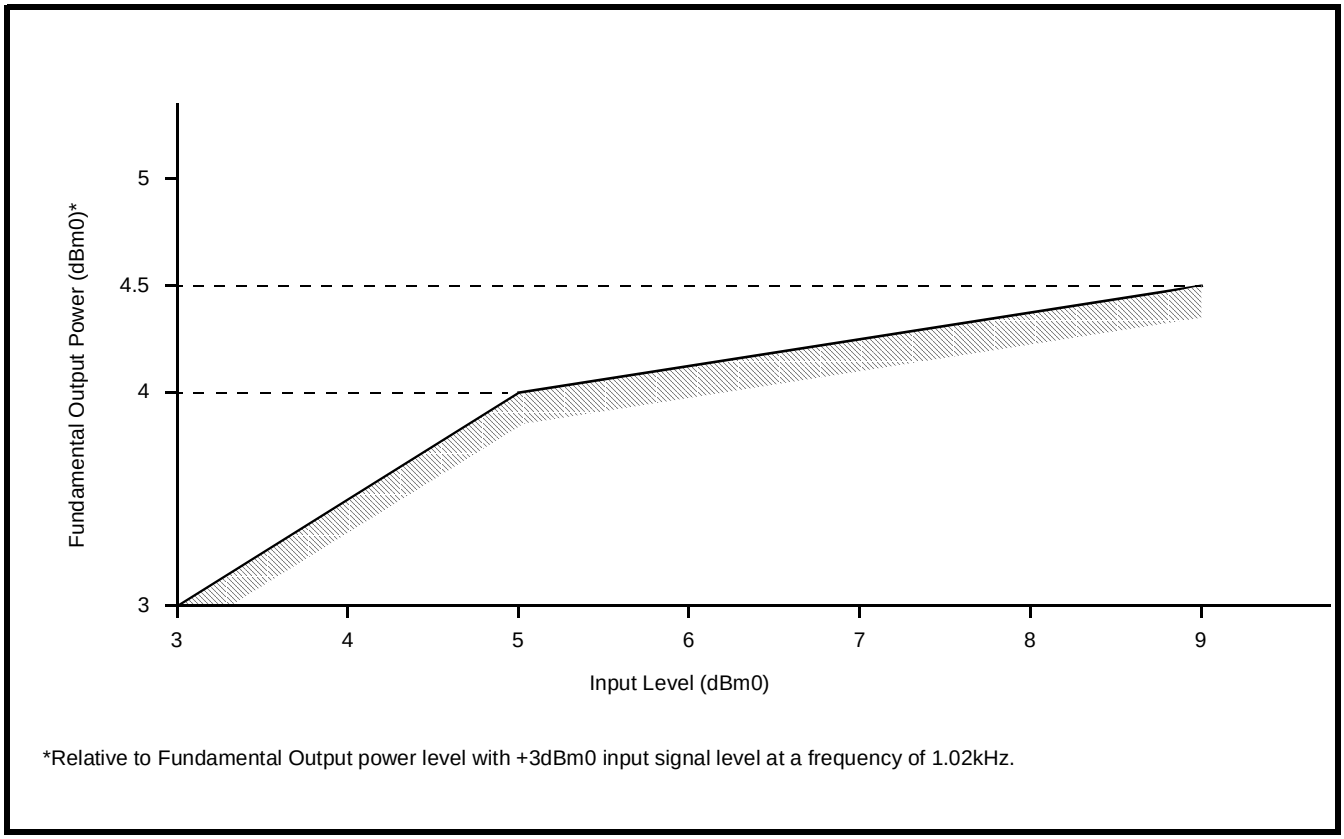


Figure 14 - Envelope Delay Variation Frequency



*Relative to Fundamental Output power level with +3dBm0 input signal level at a frequency of 1.02kHz.

Figure 15 - Overload Distortion (End-to-End)

NOTES: