

74LVTH16646

Low Voltage 16-Bit Transceiver/Register with 3-STATE Outputs

General Description

The LVTH16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition (see Functional Description).

The LVTH16646 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These transceivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH16646 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

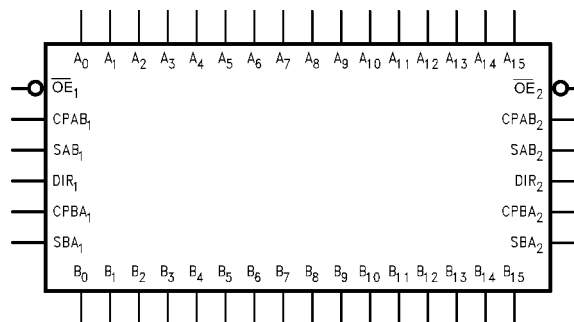
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 16646
- Latch-up performance exceeds 500 mA

Ordering Code:

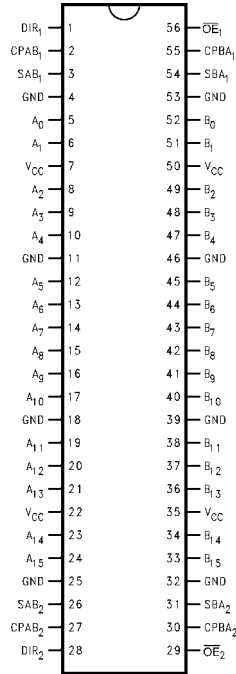
Order Number	Package Number	Package Description
74LVTH16646MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
74LVTH16646MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A ₀ -A ₁₅	Data Register A Inputs/3-STATE Outputs
B ₀ -B ₁₅	Data Register B Inputs/3-STATE Outputs
CPAB _n , CPBA _n	Clock Pulse Inputs
SAB _n , SBA _n	Select Inputs
$\overline{OE}_1, \overline{OE}_2$	Output Enable Inputs
DIR _n	Direction Control Inputs

Truth Table(Note 1)

Inputs						Data I/O		Output Operation Mode
\overline{OE}_1	DIR ₁	CPAB ₁	CPBA ₁	SAB ₁	SBA ₁	A ₀₋₇	B ₀₋₇	
H	X	H or L	H or L	X	X			Isolation
H	X	↘	X	X	X	Input	Input	Clock A _n Data into A Register Clock B _n Data Into B Register
L	H	X	X	L	X			A _n to B _n —Real Time (Transparent Mode)
L	H	↘	X	L	X	Input	Output	Clock A _n Data to A Register A Register to B _n (Stored Mode)
L	H	H or L	X	H	X			Clock A _n Data into A Register and Output to B _n
L	H	↘	X	H	X			Clock A _n Data into A Register and Output to B _n
L	L	X	X	X	L			B _n to A _n —Real Time (Transparent Mode)
L	L	X	↘	X	L	Output	Input	Clock B _n Data into B Register B Register to A _n (Stored Mode)
L	L	X	H or L	X	H			B Register to A _n (Stored Mode)
L	L	X	↘	X	H			Clock B _n into B Register and Output to A _n

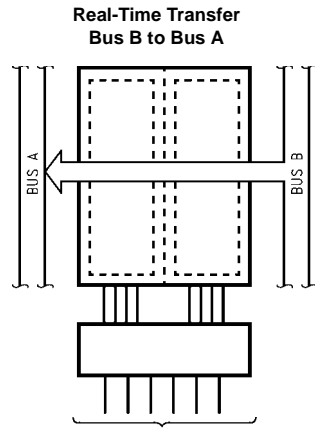
H = HIGH Voltage Level
 X = Immaterial
 L = LOW Voltage Level
 ↘ = LOW-to-HIGH Transition.

Note 1: The data output functions may be enabled or disabled by various signals at the \overline{OE} and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.

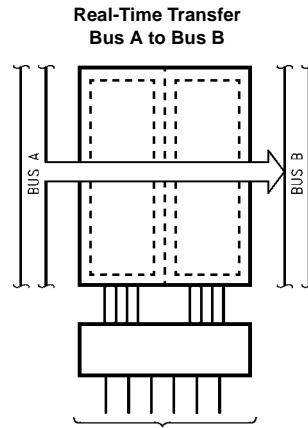
Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB_n , SBA_n) controls can multiplex stored and real-time. The examples shown below demonstrate the four fundamental bus-management functions that can be performed.

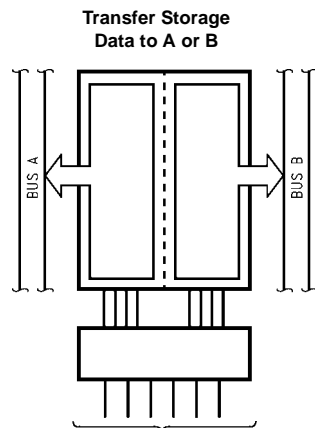
The direction control (DIR_n) determines which bus will receive data when \overline{OE}_n is LOW. In the isolation mode (\overline{OE}_n HIGH), A data may be stored in one register and/or B data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B, may be driven at a time.



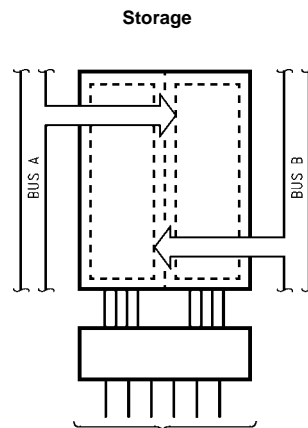
\overline{OE}	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L



\overline{OE}	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

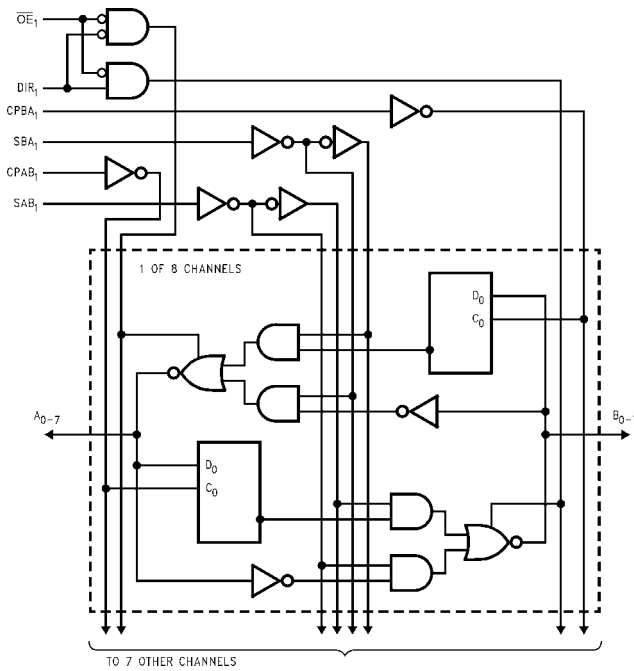
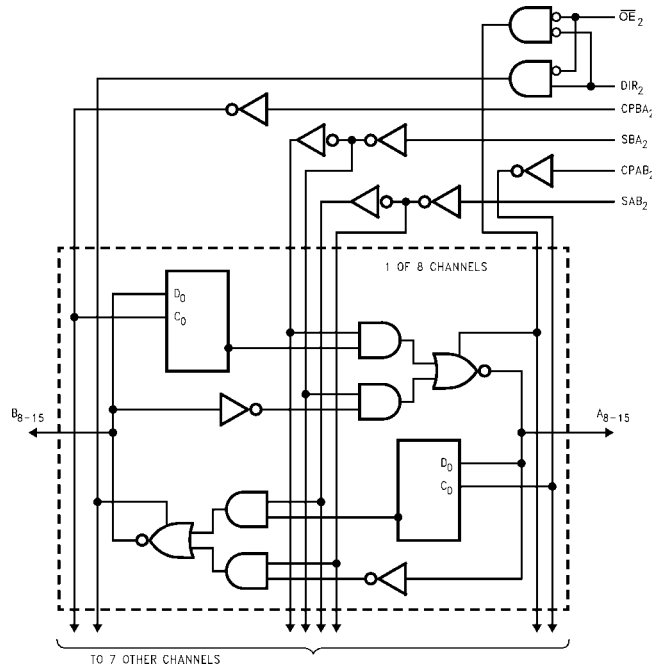


\overline{OE}	DIR	CPAB	CPBA	SAB	SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X



\overline{OE}	DIR	CPAB	CPBA	SAB	SBA
L	H	∩	X	L	X
L	L	X	∩	X	L
H	X	∩	X	X	X
H	X	X	∩	X	X

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings ^(Note 2)				
Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	-0.5 to +4.6		V
V _I	DC Input Voltage	-0.5 to +7.0		V
V _O	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 3)	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
I _O	DC Output Current	64	V _O > V _{CC} Output at HIGH State	mA
		128	V _O > V _{CC} Output at LOW State	
I _{CC}	DC Supply Current per Supply Pin	±64		mA
I _{GND}	DC Ground Current per Ground Pin	±128		mA
T _{STG}	Storage Temperature	-65 to +150		°C
Recommended Operating Conditions				
Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage	2.7	3.6	V
V _I	Input Voltage	0	5.5	V
I _{OH}	HIGH-Level Output Current		-32	mA
I _{OL}	LOW-Level Output Current		64	
T _A	Free-Air Operating Temperature	-40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V
<p>Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.</p> <p>Note 3: I_O Absolute Maximum Rating must be observed.</p>				

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions	
			Min	Max			
V _{IK}	Input Clamp Diode Voltage	2.7		-1.2	V	I _I = -18 mA	
V _{IH}	Input HIGH Voltage	2.7-3.6	2.0		V	V _O ≤ 0.1V or	
V _{IL}	Input LOW Voltage	2.7-3.6		0.8	V	V _O ≥ V _{CC} - 0.1V	
V _{OH}	Output HIGH Voltage	2.7-3.6	V _{CC} - 0.2		V	I _{OH} = -100 μA	
		2.7	2.4		V	I _{OH} = -8 mA	
		3.0	2.0		V	I _{OH} = -32 mA	
V _{OL}	Output LOW Voltage	2.7		0.2	V	I _{OL} = 100 μA	
		2.7		0.5	V	I _{OL} = 24 mA	
		3.0		0.4	V	I _{OL} = 16 mA	
		3.0		0.5	V	I _{OL} = 32 mA	
		3.0		0.55	V	I _{OL} = 64 mA	
I _{I(HOLD)}	Bushold Input Minimum Drive	3.0	75		μA	V _I = 0.8V	
			-75		μA	V _I = 2.0V	
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 4)	
			-500		μA	(Note 5)	
I _I	Input Current	3.6		10	μA	V _I = 5.5V	
			Control Pins		±1	μA	V _I = 0V or V _{CC}
			Data Pins		-5	μA	V _I = 0V
					1	μA	V _I = V _{CC}
I _{OFF}	Power Off Leakage Current	0		±100	μA	0V ≤ V _I or V _O ≤ 5.5V	
I _{PU/PO}	Power Up/Down 3-STATE Output Current	0-1.5V		±100	μA	V _O = 0.5V to 3.0V V _I = GND or V _{CC}	
I _{OZL}	3-STATE Output Leakage Current	3.6		-5	μA	V _O = 0.0V	
I _{OZH}	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.6V	
I _{OZH+}	3-STATE Output Leakage Current	3.6		10	μA	V _{CC} < V _O ≤ 5.5V	
I _{CCH}	Power Supply Current	3.6		0.19	mA	Outputs HIGH	
I _{CCL}	Power Supply Current	3.6		5	mA	Outputs LOW	
I _{CCZ}	Power Supply Current	3.6		0.19	mA	Outputs Disabled	
I _{CCZ+}	Power Supply Current	3.6		0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled	
ΔI _{CC}	Increase in Power Supply Current (Note 6)	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND	

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 8)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 8)

Note 7: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}, R_L = 500\Omega$				Units
		$V_{CC} = 3.3 \pm 0.3\text{V}$		$V_{CC} = 2.7\text{V}$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150		150		MHz
t_{PLH}	Propagation Delay	1.3	5.4	1.3	5.9	ns
t_{PHL}	CPAB or CPBA to A or B	1.3	5.2	1.3	5.8	
t_{PLH}	Propagation Delay	1.0	4.4	1.0	4.7	ns
t_{PHL}	Data to A or B	1.0	4.6	1.0	5.1	
t_{PLH}	Propagation Delay	1.0	4.6	1.0	5.4	ns
t_{PHL}	SBA or SAB to A or B	1.0	4.8	1.0	5.6	
t_{PZH}	Output Enable Time	1.0	4.7	1.0	5.4	ns
t_{PZL}	\overline{OE} to A or B	1.0	5.1	1.0	6.0	
t_{PHZ}	Output Disable Time	2.0	5.6	2.0	6.1	ns
t_{PLZ}	\overline{OE} to A or B	2.0	5.4	2.0	6.1	
t_{PZH}	Output Enable Time	1.0	4.9	1.0	5.4	ns
t_{PZL}	DIR to A or B	1.0	5.4	1.0	6.4	
t_{PHZ}	Output Disable Time	1.5	6.4	1.5	7.1	ns
t_{PLZ}	DIR to A or B	1.5	5.4	1.5	5.9	
t_W	Pulse Duration	CPAB or CPBA HIGH or LOW		3.3		ns
t_S	Setup Time	A or B before CPAB or CPBA, Data HIGH		1.2	1.5	ns
		A or B before CPAB or CPBA, Data LOW		2.0	2.8	
t_H	Hold Time	A or B after CPAB or CPBA, Data HIGH		0.5	0.0	ns
		A or B after CPAB or CPBA, Data LOW		0.5	0.5	
t_{OSHL}	Output to Output Skew (Note 9)		1.0		1.0	ns
t_{OSLH}			1.0		1.0	

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

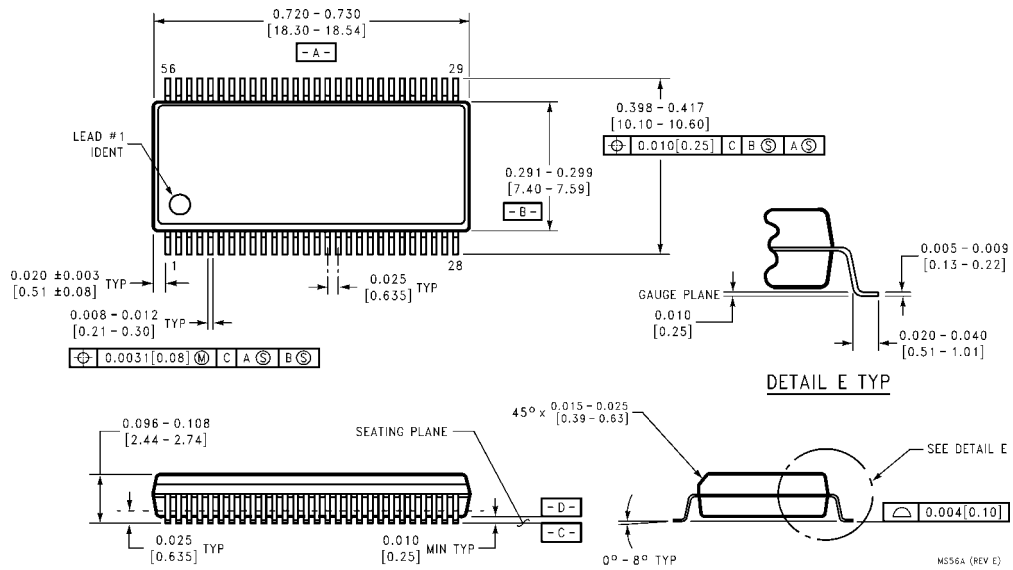
Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0\text{V or } V_{CC}$	4	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.0\text{V}, V_O = 0\text{V or } V_{CC}$	8	pF

Note 10: Capacitance is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883, Method 3012.

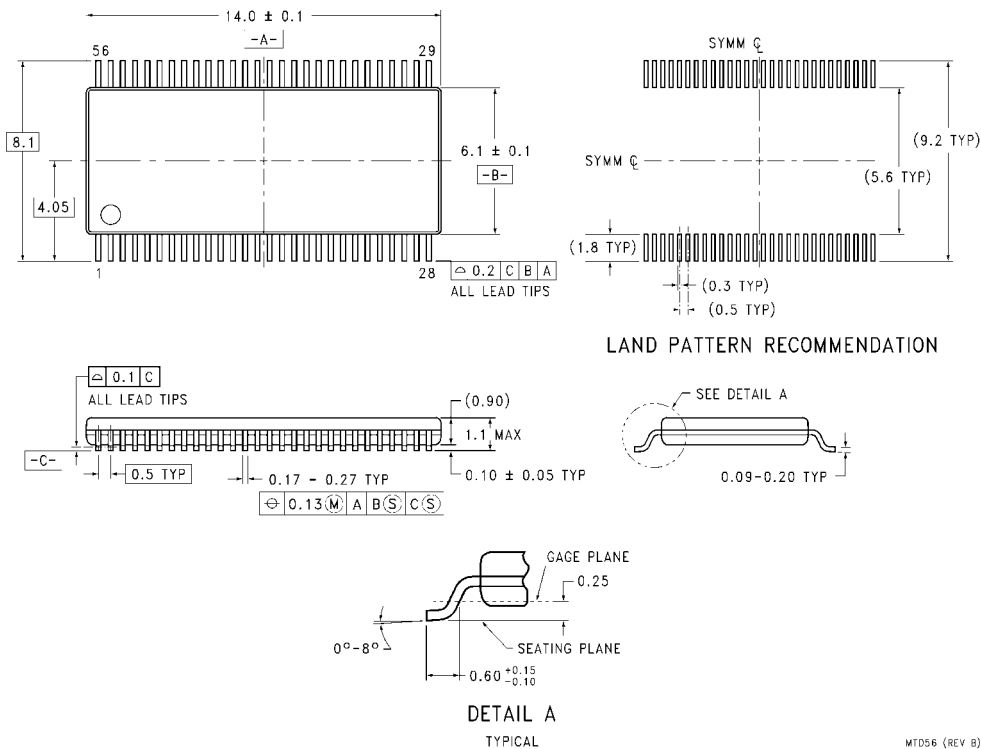
74LVTH16646

Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

MTD56 (REV B)

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