ANALOG DEVICES

16-/32- Channel, Serially Controlled 4 Ω 1.8 V to 5.5 V, ±2.5 V, Analog Multiplexers

Preliminary Technical Data   ADG725/ADG731

FEATURES
3-Wire SPI Serial Interface
1.8 V to 5.5 V Single Supply
±2.5 V Dual Supply Operation
4 Ω On Resistance
0.5 Ω On Resistance Flatness
7mm x 7mm 48 lead Chip Scale Package (CSP)
    or 48 lead TQFP package.
Rail to Rail Operation
Power On Reset
Fast Switching Times
Single 32 to 1 Channel Multiplexer
Dual/Differential 16 to 1 Channel Multiplexer
TTL/CMOS Compatible Inputs
For Functionally Equivalent devices with Parallel Interface
    See ADG726/ADG732

APPLICATIONS
Optical Applications
Data Acquisition Systems
Communication Systems
Relay replacement
Audio and Video Switching
Battery Powered Systems
Medical Instrumentation
Automatic Test Equipment

FUNCTIONAL BLOCK DIAGRAMS

GENERAL DESCRIPTION

The ADG725/ADG731 are monolithic CMOS 32 channel/dual 16 channel analog multiplexers with a serially controlled 3-wire interface. The ADG732 switches one of thirty-two inputs (S1-S32) to a common output, D. The ADG725 can be configured as a dual mux switching one of sixteen inputs to one output or a differential mux switching one of sixteen inputs to a differential output.
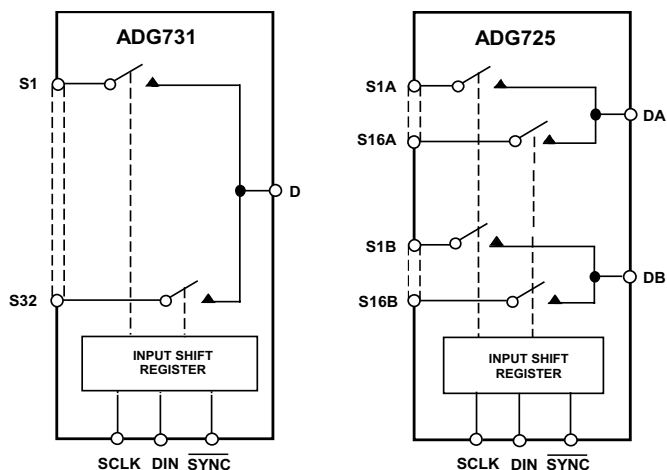
These mulitplexers utilize a 3-wire serial interface that is compatible with SPI™, QSPI™, MICROWIRE™ and some DSP interface standards. On power-up, the internal shift register contains all zeros and all switch are in the OFF state.

These multiplexers are designed on an enhanced submicron process that provides low power dissipation yet gives high switching speed, very low on resistance and leakage currents. They operate from single supply of 1.8V to 5.5V and ±2.5 V dual supply, making them ideally suited to a variety of applications. On resistance is in the region of a few Ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either Multiplexers or De-Multiplexers

and have an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels.

They are available in either 48 lead CSP or TQFP package.

PRODUCT HIGHLIGHTS
1. 3-Wire Serial Interface.
2. +1.8 V to +5.5 V Single or ±2.5 V Dual Supply operation. These parts are specified and guaranteed with +5 V ±10%, +3 V ±10% single supply and ±2.5 V ±10% dual supply rails.
3. On Resistance of 4 Ω.
4. Guaranteed Break-Before-Make Switching Action.
5. 7mm x 7mm 48 lead Chip Scale Package (CSP) or 48 lead TQFP package.

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ADG725/ADG731–SPECIFICATIONS[1] (V_{DD} = 5V ± 10%, V_{SS} = 0V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	4		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	5.5	6	Ω max	Test Circuit 1
On-Resistance Match Between		0.3	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
	±0.25	±0.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_D = 4.5 V/1 V, V_S = 1 V/4.5 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 3
ADG731	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_D = V_S = 1 V, or 4.5V;
ADG725	±0.5	±2.5	nA max	Test Circuit 4
ADG726	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	40		ns typ	R_L = 300 Ω, C_L = 35 pF, Test Circuit 5;
		60	ns max	V_{S1} = 3 V/0 V, V_{S32} = 0 V/3V
Break-Before-Make Time Delay, t_D	30		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 3 V, Test Circuit 6
Charge Injection	±5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF;
				Test Circuit 7
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz;
				Test Circuit 8
Channel to Channel Crosstalk	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz;
				Test Circuit 9
-3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	13		pF typ	f = 1 MHz
C_D (OFF)				
ADG725	180		pF typ	f = 1 MHz
ADG731	360		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	200		pF typ	f = 1 MHz
ADG731	400		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +5.5 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or +5.5 V
		20	µA max	

NOTES
[1]Temperature range is as follows: B Version: −40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

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SPECIFICATIONS[1] (V_{DD} = 3V ± 10%, V_{SS} = 0V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25ºC	B Version −40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On-Resistance (R_{ON})	7		Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA;
	11	12	Ω max	Test Circuit 1
On-Resistance Match Between		0.4	Ω typ	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		1	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)		3	Ω max	V_S = 0 V to V_{DD}, I_{DS} = 10 mA
LEAKAGE CURRENTS				V_{DD} = 3.3 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V;
	±0.25	±0.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_S = 1 V/3 V, V_D = 3 V/1 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 3
ADG731	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.05		nA typ	V_S = V_D = +1 V or +3 V;
ADG725	±0.5	±2.5	nA max	Test Circuit 4
ADG731	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	µA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	45		ns typ	R_L = 300 Ω, C_L = 35 pF Test Circuit 5
		75	ns max	V_{S1} = 2 V/0 V, V_{S32} = 0 V/2 V
Break-Before-Make Time Delay, t_D	30		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 2 V, Test Circuit 6
Charge Injection	±5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 7
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 8
Channel to Channel Crosstalk	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9
-3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	13		pF typ	f = 1 MHz
C_D (OFF)				
ADG725	180		pF typ	f = 1 MHz
ADG731	360		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	200		pF typ	f = 1 MHz
ADG731	400		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +3.3 V
I_{DD}	10		µA typ	Digital Inputs = 0 V or +3.3 V
		20	µA max	

NOTES

[1]Temperature ranges are as follows: B Version: −40°C to +85°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG725/ADG731–SPECIFICATIONS[1] Dual Supply

(V_{DD} = +2.5 V ±10%, V_{SS} = -2.5 V ±10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version −40°C to +85°C	Units	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On-Resistance (R_{ON})	4		Ω typ	$V_S = V_{SS}$ to V_{DD}, I_{DS} = 10 mA;
	5.5	6	Ω max	Test Circuit 1
On-Resistance Match Between		0.3	Ω typ	$V_S = V_{SS}$ to V_{DD}, I_{DS} = 10 mA
Channels (ΔR_{ON})		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.5		Ω typ	$V_S = V_{SS}$ to V_{DD}, I_{DS} = 10 mA
		1	Ω max	
LEAKAGE CURRENTS				V_{DD} = +2.75 V, V_{SS} = -2.75 V
Source OFF Leakage I_S (OFF)	±0.01		nA typ	V_S = +2.25 V/-1.25 V, V_D = -1.25 V/+2.25 V;
	±0.25	±0.5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.05		nA typ	V_S = +2.25 V/-1.25 V, V_D = -1.25 V/+2.25 V;
	±0.5	±2.5	nA max	Test Circuit 3
	±1	±5	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01		nA typ	$V_S = V_D$ = +2.25 V/-1.25 V, Test Circuit 4
	±0.5	±2.5	nA max	
	±1	±5	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		1.7	V min	
Input Low Voltage, V_{INL}		0.7	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		±0.1	μA max	
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
$t_{TRANSITION}$	40		ns typ	R_L = 300 Ω, C_L = 35 pF Test Circuit 5
		60	ns max	V_{S1} = 1.5 V/0 V, V_{S32} = 0 V/1.5 V
Break-Before-Make Time Delay, t_D	15		ns typ	R_L = 300 Ω, C_L = 35 pF;
		1	ns min	V_S = 1.5 V, Test Circuit 6
Charge Injection	±8		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test 7
Off Isolation	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz;
				Test Circuit 8
Channel to Channel Crosstalk	-60		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz;
				Test Circuit 9
-3 dB Bandwidth				
ADG725	34		MHz typ	R_L = 50 Ω, C_L = 5 pF, Test Circuit 10
ADG731	18		MHz typ	
C_S (OFF)	13		pF typ	
C_D (OFF)				
ADG725	180		pF typ	f = 1 MHz
ADG731	360		pF typ	f = 1 MHz
C_D, C_S (ON)				
ADG725	200		pF typ	f = 1 MHz
ADG731	400		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +2.75 V
I_{DD}	10		μA typ	Digital Inputs = 0 V or +2.75 V
		20	μA max	
I_{SS}	10		μA typ	V_{SS} = -2.75 V
		20	μA max	Digital Inputs = 0 V or +2.75 V

NOTES
[1]Temperature range is as follows: B Version: −40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

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TIMING CHARACTERISTICS[1,2]

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Conditions/Comments
t_1	33	ns min	SCLK Cycle time
t_2	13	ns min	SCLK High Time
t_3	13	ns min	SCLK Low Time
t_4	13	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	40	ns min	Minimum $\overline{SYNC}$ low time
t_6	5	ns min	Data Setup Time
t_7	4.5	ns min	Data Hold Time
t_8	33	ns min	Minimum $\overline{SYNC}$ high time

NOTES
[1]See Figure 1.
[2]All input signals are specified with tr =tf = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

Specifications subject to change without notice.
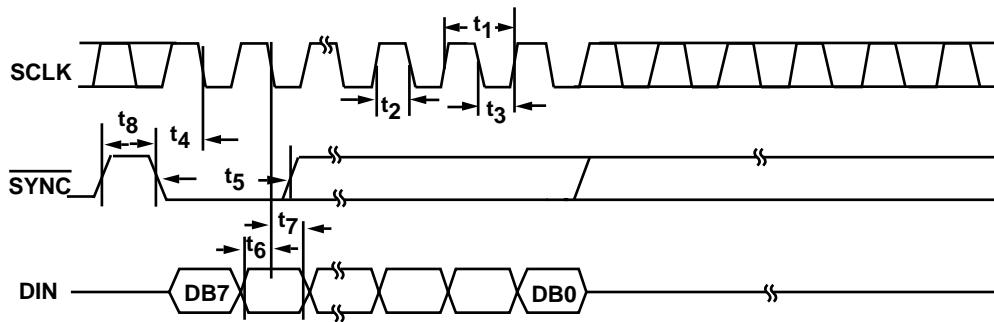
Figure 1. 3-Wire Serial Interface Timing Diagram.
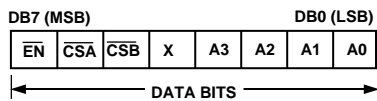
Figure 2. ADG725 Input Shift Register Contents
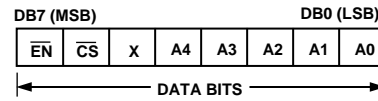
Figure 3. ADG731 Input Shift Register Contents

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS}	+7 V
V_{DD} to GND	–0.3 V to +7 V
V_{SS} to GND	+0.3 V to -7 V
Analog Inputs[2]	V_{SS} - 0.3 V to V_{DD} +0.3 Vor
	30 mA, Whichever Occurs First
Digital Inputs[2]	-0.3V to V_{DD} +0.3 V or
	30 mA, Whichever Occurs First
Peak Current, S or D	60mA
	(Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D	30mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C

Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
48 lead CSP θ_{JA} Thermal Impedance	TBD°C/W
48 lead TQFP θ_{JA} Thermal Impedance	TBD°C/W
Lead Temperature, Soldering (10seconds)	300°C
IR Reflow, Peak Temperature	+220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at SCLK, $\overline{SYNC}$, DIN, $\overline{RS}$, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG725BCP	-40 °C to +85 °C	Chip Scale Package (CSP)	CP-48
ADG725BSU	-40 °C to +85 °C	Thin Quad Flatpack	SU-48
ADG731BCP	-40 °C to +85 °C	Chip Scale Package (CSP)	CP-48
ADG731BSU	-40 °C to +85 °C	Thin Quad Flatpack	SU-48

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ADG725/ADG731

PIN FUNCTION DESCRIPTION

ADG725	ADG731	Mnemonic	Function
		SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. These devices can accomodate serial input rates of up to 30MHz.
		$\overline{RS}$	Active low control input that clears the input register and turns all switches to the OFF condition.
		DIN	Serial Data Input. Data is clocked into the 8-bit input register on the falling edge of the serial clock input.
		SXX	Source. May be an input or output.
		DX	Drain. May be an input or output.
		V_{DD}	Power Supply Input. These parts can be operated from a supply of +1.8V to +5.5V and dual supply of +/-2.5V.
		GND	Ground reference.
		$\overline{SYNC}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it powers on the SCLK and DIN buffers and the input shift register is enabled. An 8-bit counter is also enabled. Data is transferred on the falling edges of the following clocks. After 8 falling clock edges, switch conditions are automaticaly updated. $\overline{SYNC}$ may be used to frame the signal, or just pulled low for a short period of time to enable the counter and input buffers.

PIN CONFIGURATIONS
CSP & TQFP
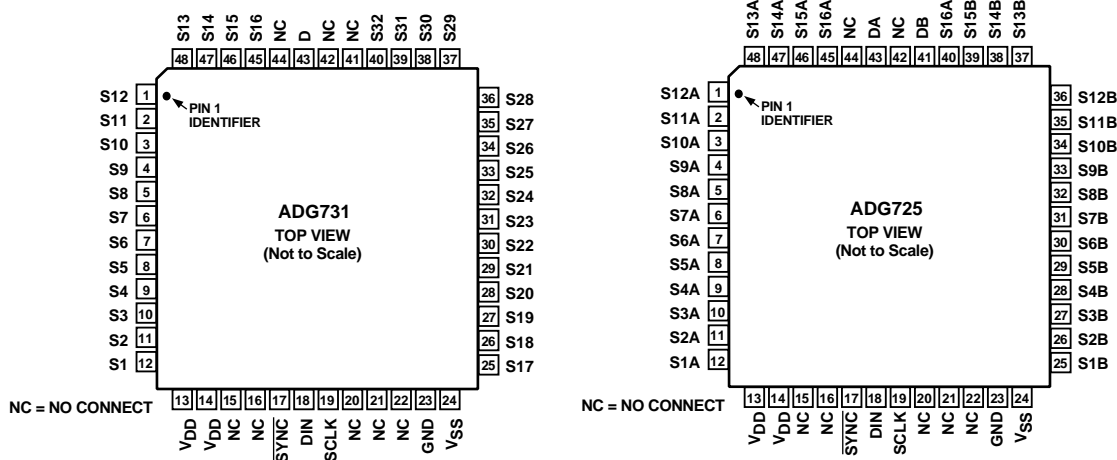
ADG725/ADG731

Table 1. ADG725 Truth Table

A3	A2	A1	A0	$\overline{E}\,\overline{N}$	$\overline{C}\,\overline{S}\,\overline{A}$	$\overline{C}\,\overline{S}\,\overline{B}$	Switch Condition
X	X	X	X	X	1	1	Retains previous switch condition
X	X	X	X	1	1	1	All Switches OFF
0	0	0	0	0	0	0	S1A - DA, S1B - DB
0	0	0	1	0	0	0	S2A - DA, S2B - DB
0	0	1	0	0	0	0	S3A - DA, S3B - DB
0	0	1	1	0	0	0	S4A - DA, S4B - DB
0	1	0	0	0	0	0	S5A - DA, S5B - DB
0	1	0	1	0	0	0	S6A - DA, S6B - DB
0	1	1	0	0	0	0	S7A - DA, S7B - DB
0	1	1	1	0	0	0	S8A - DA, S8B - DB
1	0	0	0	0	0	0	S9A - DA, S9B - DB
1	0	0	1	0	0	0	S10A - DA, S10B - DB
1	0	1	0	0	0	0	S11A - DA, S11B - DB
1	0	1	1	0	0	0	S12A - DA, S12B - DB
1	1	0	0	0	0	0	S13A - DA, S13B - DB
1	1	0	1	0	0	0	S14A - DA, S14B - DB
1	1	1	0	0	0	0	S15A - DA, S15B - DB
1	1	1	1	0	0	0	S16A - DA, S16B - DB

Table 2. ADG731 Truth Table

A4	A3	A2	A1	A0	$\overline{E}\,\overline{N}$	$\overline{C}\,\overline{S}$	Switch Condition
X	X	X	X	X	X	1	Retains previous switch condition
X	X	X	X	X	1	1	All Switches OFF
0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	2
0	0	0	1	0	0	0	3
0	0	0	1	1	0	0	4
0	0	1	0	0	0	0	5
0	0	1	0	1	0	0	6
0	0	1	1	0	0	0	7
0	0	1	1	1	0	0	8
0	1	0	0	0	0	0	9
0	1	0	0	1	0	0	10
0	1	0	1	0	0	0	11
0	1	0	1	1	0	0	12
0	1	1	0	0	0	0	13
0	1	1	0	1	0	0	14
0	1	1	1	0	0	0	15
0	1	1	1	1	0	0	16
1	0	0	0	0	0	0	17
1	0	0	0	1	0	0	18
1	0	0	1	0	0	0	19
1	0	0	1	1	0	0	20
1	0	1	0	0	0	0	21
1	0	1	0	1	0	0	22
1	0	1	1	0	0	0	23
1	0	1	1	1	0	0	24
1	1	0	0	0	0	0	25
1	1	0	0	1	0	0	26
1	1	0	1	0	0	0	27
1	1	0	1	1	0	0	28
1	1	1	0	0	0	0	29
1	1	1	0	1	0	0	30
1	1	1	1	0	0	0	31
1	1	1	1	1	0	0	32

X = Don't Care

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ADG725/ADG731

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most Negative power supply in a dual supply application. In single supply applications, connect to GND.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
$V_D (V_S)$	Analog voltage on terminals D, S
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	On resistance match between any two channels, i.e. R_{ON}max - R_{ON}min
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
I_S (OFF)	Source leakage current with the switch "OFF."
I_D (OFF)	Drain leakage current with the switch "OFF."
I_D, I_S (ON)	Channel leakage current with the switch "ON."
V_{INL}	Maximum input voltage for logic "0".
V_{INH}	Minimum input voltage for logic "1".
$I_{INL}(I_{INH})$	Input current of the digital input.
C_S (OFF)	"OFF" switch source capacitance. Measured with reference to ground.
C_D (OFF)	"OFF" switch drain capacitance. Measured with reference to ground.
C_D, C_S(ON)	"ON" switch capacitance. Measured with reference to ground.
C_{IN}	Digital input capacitance.
$t_{TRANSITION}$	Delay time measured between the 50% and 90% points of the SYNC and the switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between the 80% points of both switches when switching from one address state to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal is coupled through from one channel to another as a result of parasitic capacitance.
On Response	The Frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch.

ADG725/ADG731

TYPICAL PERFORMANCE CHARACTERISTICS

TBD
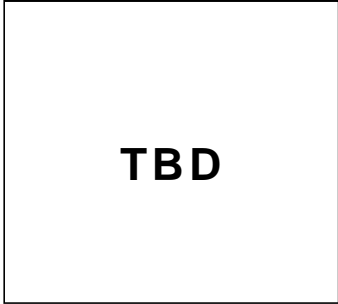
TPC 1. On Resistance vs. $V_D(V_S)$ for for Single Supply

TBD
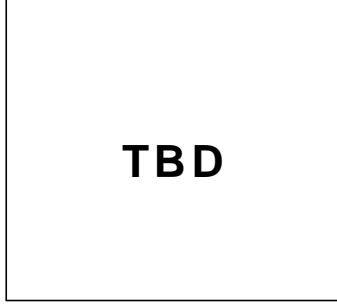
TPC 4. On Resistance vs. $V_D(V_S)$ for Different Temperatures, Single Supply

TBD
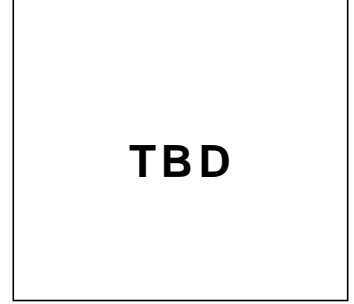
TPC 7. Leakage Currents vs. $V_D(V_S)$

TBD
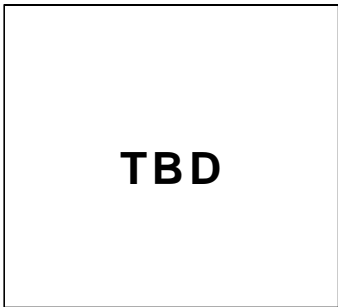
TPC 2. On Resistance vs. $V_D(V_S)$ for Dual Supply

TBD
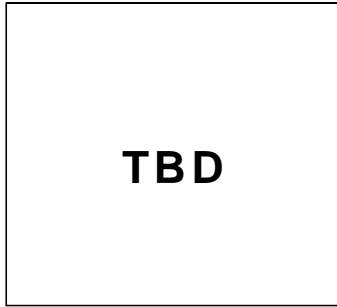
TPC 5. On Resistance vs. $V_D(V_S)$ for Different Temperatures, Dual Supply
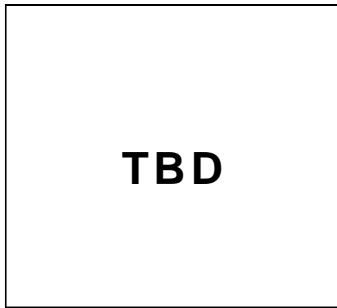
TBD
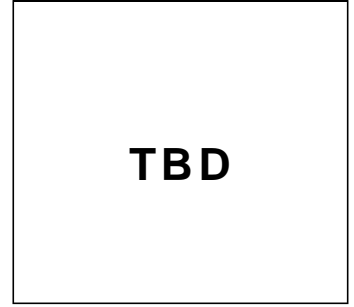
TPC 8. Leakage Currents vs. $V_D(V_S)$

TBD
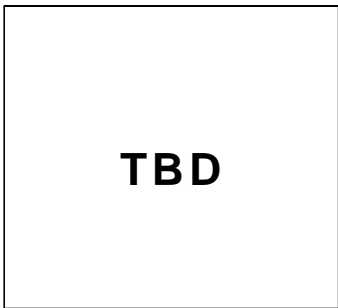
TPC 3. On Resistance vs. $V_D(V_S)$ for Different Temperatures, Single Supply

TBD
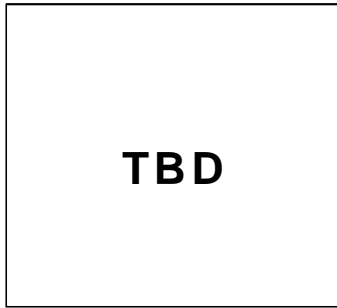
TPC 6. Leakage Currents vs. $V_D(V_S)$

TBD
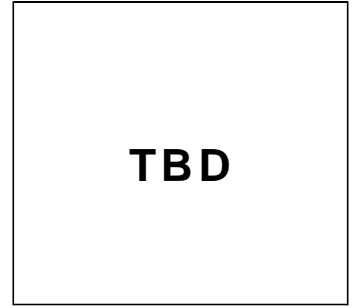
TPC 9. Leakage Currents vs. Temperature

REV. PrD

TBD

TPC 10. Leakage Currents vs. Temperature

TBD
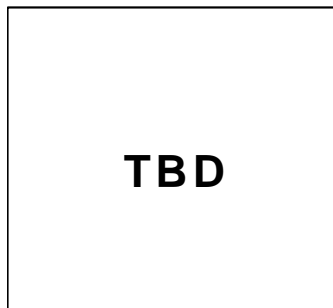
TPC 13. T_{ON}/T_{OFF} Times vs. Temperature

TBD
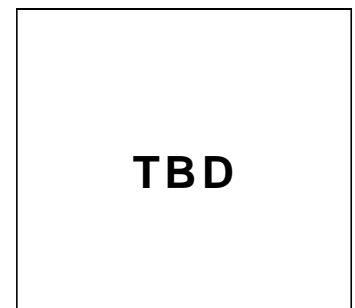
TPC 16. On Response vs. Frequency

TBD
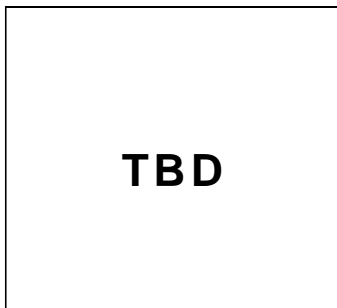
TPC 11. Supply Currents vs. Input Switching Frequency

TBD
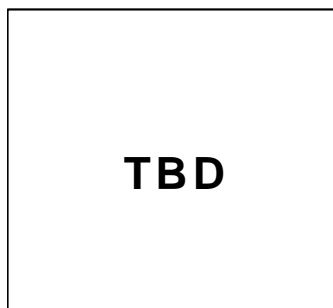
TPC 14. Off Isolation vs. Frequency

TBD
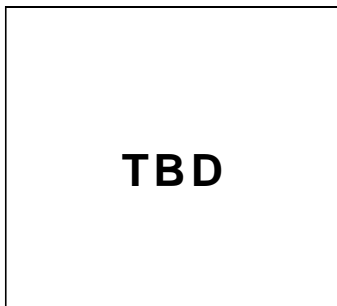
TPC 12. Charge Injection vs. Source Voltage

TBD
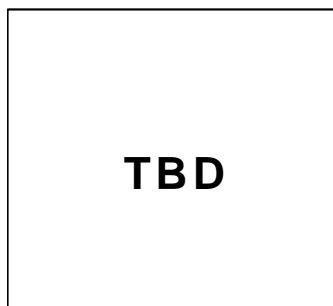
TPC 15. Crosstalk vs. Frequency

ADG725/ADG731

GENERAL DESCRIPTION

The ADG725 and ADG731 are serially controlled, 32 channel and dual/differential 16 channel multiplexers respectively.

POWER ON RESET

On power up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

SERIAL INTERFACE

The ADG725 and ADG731 have a three wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN), which is compatible with SPI, QSPI, MICROWIRE interface standards and most DSP's. Figure 1 shows the timing diagram of a typical write sequence.

Data is written to the 8-bit shift register via DIN under the control of the $\overline{\text{SYNC}}$ and SCLK signals.

When $\overline{\text{SYNC}}$ goes low, the input shift register is enabled. An 8-bit counter is also enabled. Data from DIN is clocked into the shift register on the falling edge of SCLK. Figures 2 & 3 show the contents of the input shift registers for these devices. When the part has received eight clock cycles after $\overline{\text{SYNC}}$ has been pulled low, the switches are automatically updated with the new configuration and the input shift register is disabled. With $\overline{\text{SYNC}}$ held high, any further data or noise on the DIN line will have no effect on the shift register.

The ADG725 $\overline{\text{CSA}}$ and $\overline{\text{CSB}}$ data bits allow the user the flexibility to change the configuration of either or both banks of the multiplexer.
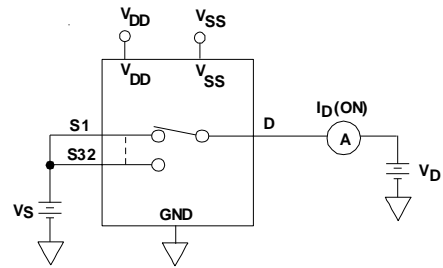
REV. PrD
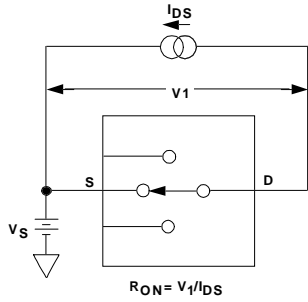
Test Circuits

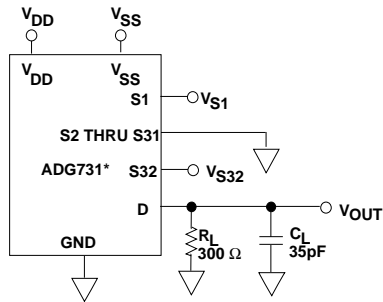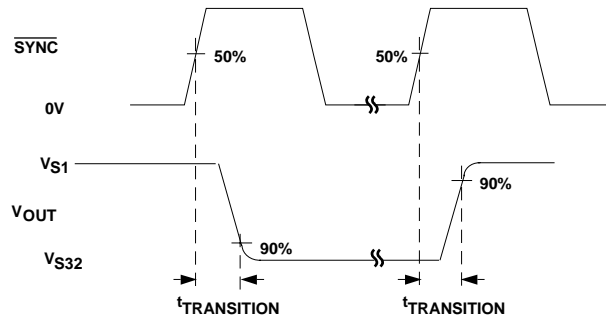Test Circuit 1. On Resistance.
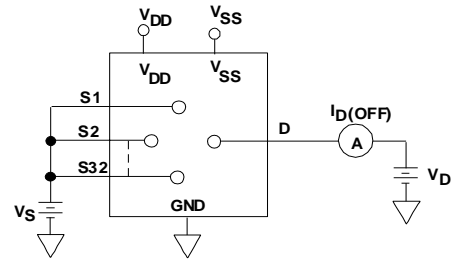
Test Circuit 3. I_D (OFF)
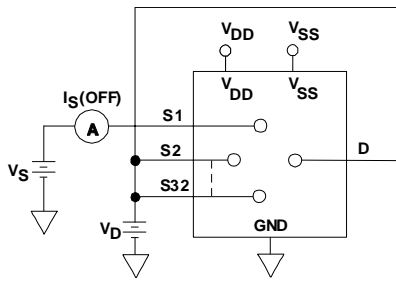
Test Circuit 2. I_S (OFF).

Test Circuit 4. I_D (ON)

Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$.
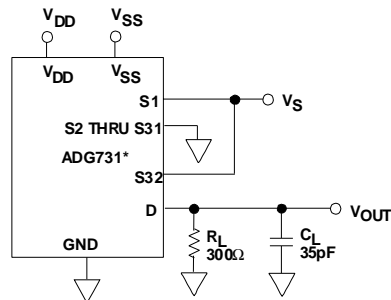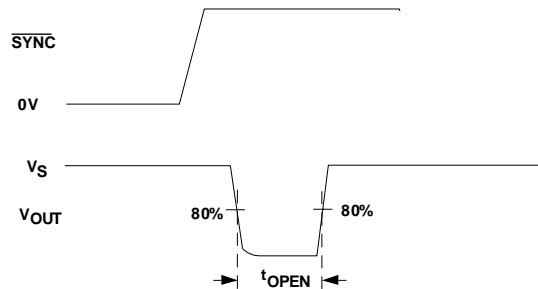
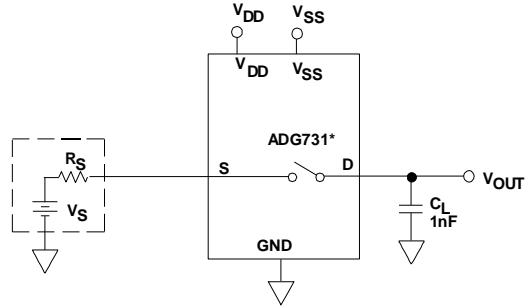Test Circuit 6. Break Before Make Delay, t_{OPEN}.

ADG725/ADG731

$*$SIMILAR CONNECTION FOR ADG725

$Q_{INJ} = C_L \times \Delta V_{OUT}$

Test Circuit 7. Charge Injection.
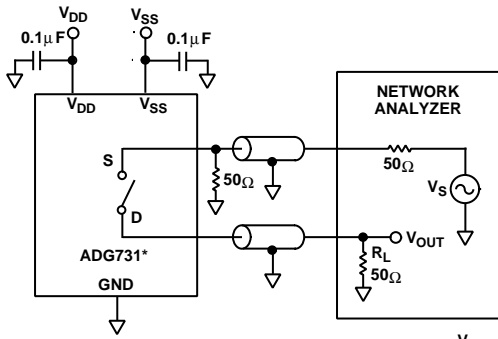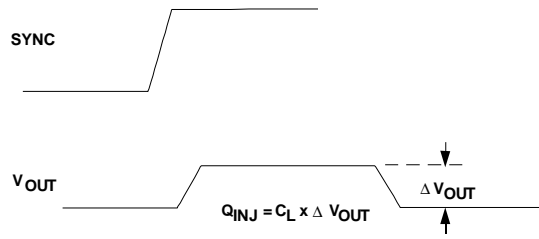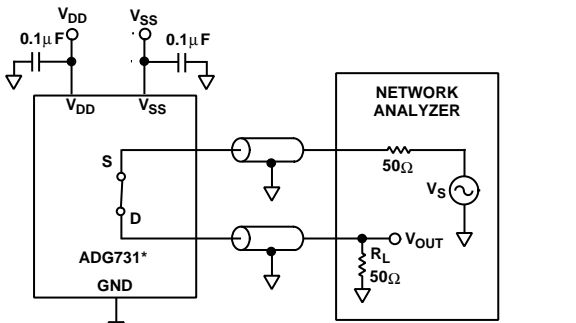
OFF ISOLATION = $20 \, LOG \, \dfrac{V_{OUT}}{V_S}$

$*$SIMILAR CONNECTION FOR ADG725

Test Circuit 8. OFF Isolation
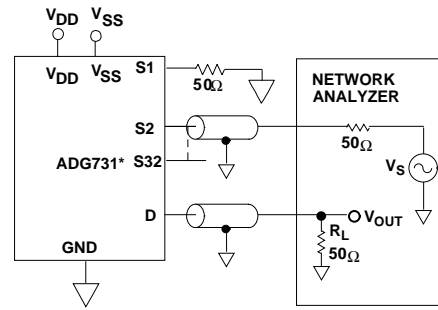
$*$SIMILAR CONNECTION FOR ADG725
CHANNEL TO CHANNEL CROSSTALK=
$20LOG_{10}(V_{OUT}/V_S)$

Test Circuit 9. Channel-to-Channel Crosstalk.

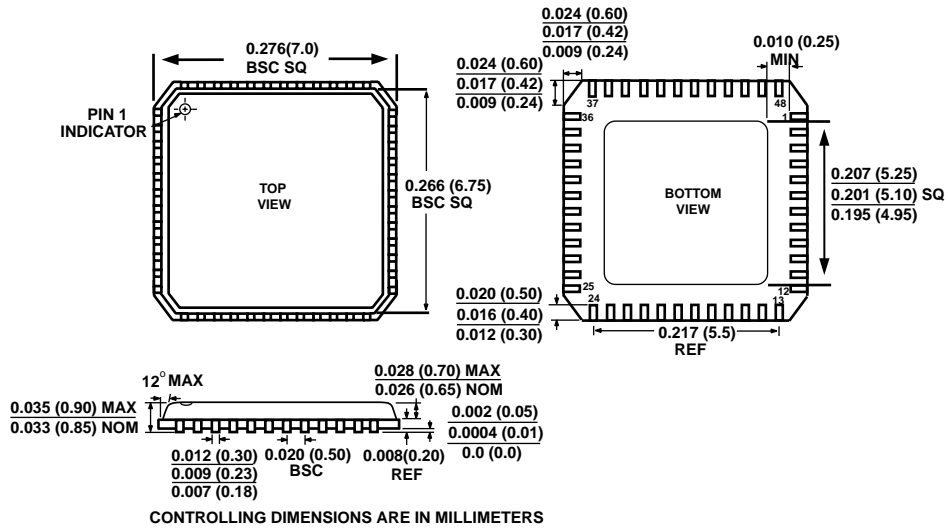INSERTION LOSS = 20 LOG $\dfrac{VOUT \ WITH \ SWITCH}{VOUT \ WITHOUT \ SWITCH}$

$*$SIMILAR CONNECTION FOR ADG725

Test Circuit 10. Bandwidth

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead CSP
(CP-48)

CONTROLLING DIMENSIONS ARE IN MILLIMETERS

48-Lead TQFP
(SU-48)