SONY

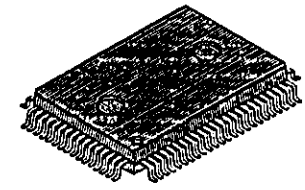
CXP50120/50124

CMOS 4-bit 1 Chip Microcomputer

Description

The CXP50120/CXP50124 is a CMOS 4-bit microcomputer which consists of 4-bit CPU, ROM, RAM, I/O port, 8-bit timer, 8-bit timer/counter, 18-bit time base timer, 8-bit serial I/O, vector interruption, power on reset function, fluorescent display tube controller/driver, D/A conversion PWM output port. a remote control receive circuit, 3-bit A/D converters, a 32kHz timer/event counter 8-bit timer and a power supply voltage detection reset function. They are integrated into a single chip with the standby function, etc. which are to be operated at a low power consumption.

80pin QFP (Plastic)



Features

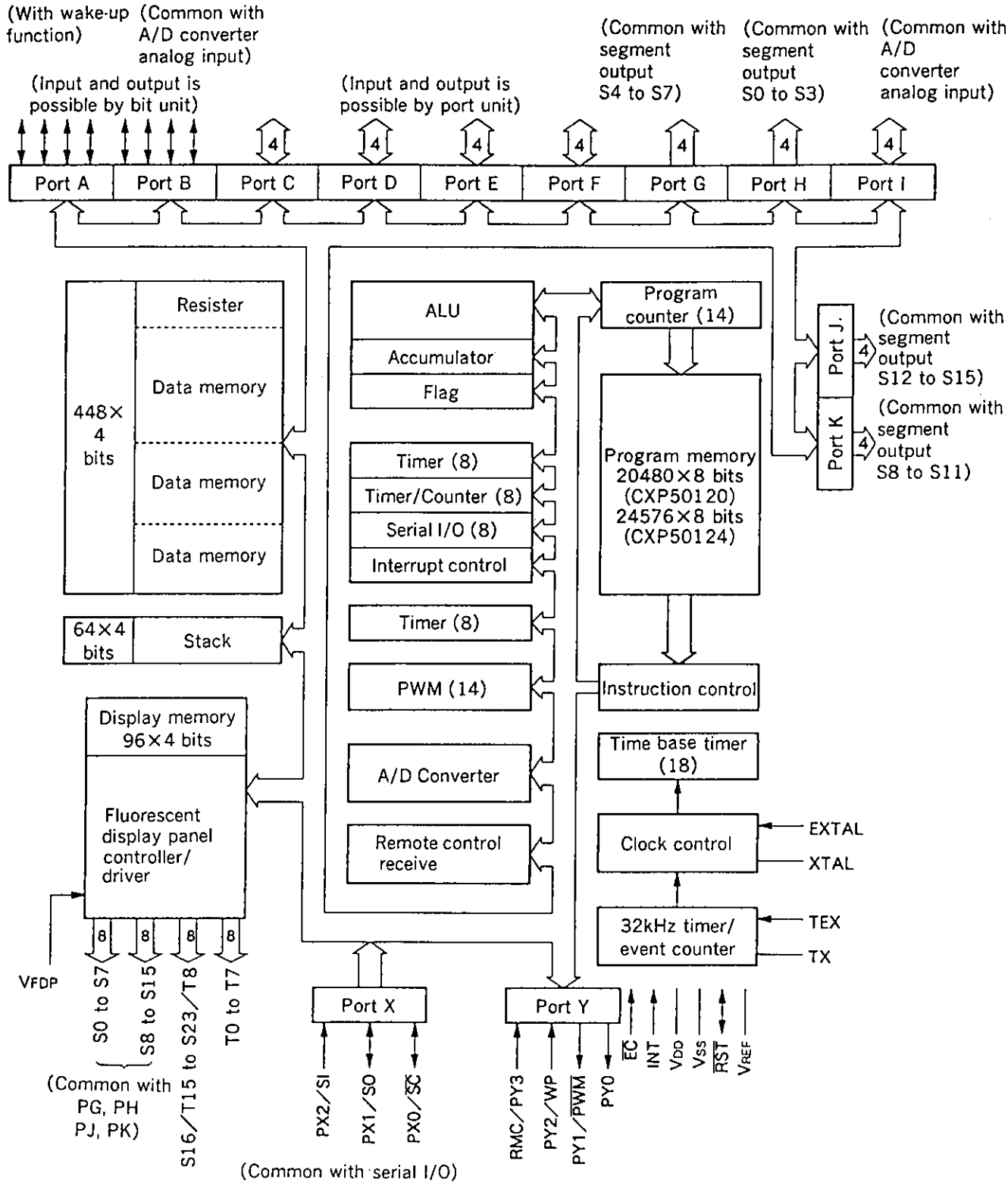
- Instruction cycle 1.9μs/4.19MHz
  122μs/32kHz
  (Selectable at programming)
- ROM capacitance
  20,480×8 bits (CXP50120)
  24,576×8 bits (CXP50124)
- RAM capacitance 544×4 bits
  (Display area included)
- 51 general purpose I/O ports
- 8 large current ports (Ports C, D)
- Fluorescent display tube controller/driver
  (Maximum 256 segments display possible)
  — 1 to 16 digits dynamic scan display
  (1 to 8 digits at 24 segments)
  — Page mode/variable mode
  — Dimmer function
  — High tension proof output (40V)
  — Pull-down resistance
  (mask option for each bit)
- 14-bit PWM output for D/A conversion
- Remote control receiving circuit
  (Be independent of the timer/counter)
- 3-bit A/D converter (8 channels per circuit)
- 32kHz reload timer/event counter
- Power supply voltage detection reset circuit
- Rich wake-up functions
  WP pin
  4 general purpose ports (edge detection)
  32kHz timer/counter
  Remote control receiving circuit
- 8-bit/4-bit variable prescaler serial I/O
- 8-bit timer with prescaler, 8-bit timer with prescaler/event counter and 18-bit time base timer, 8-bit reload timer with prescaler, independently controlled
- Arithmetic and logical operations possible between the entire ROM area, I/O area and the accumulator by means of memory mapped I/O
- Referance to the entire ROM area is possible with the table look-up instruction
- 2 kinds of power down modes, sleep and stop
- Power on reset circuit (mask option)
- Provided with 80-pin plastic QFP
- Provided with 80-pin piggyback QFP
  (CXP50100)

Structure

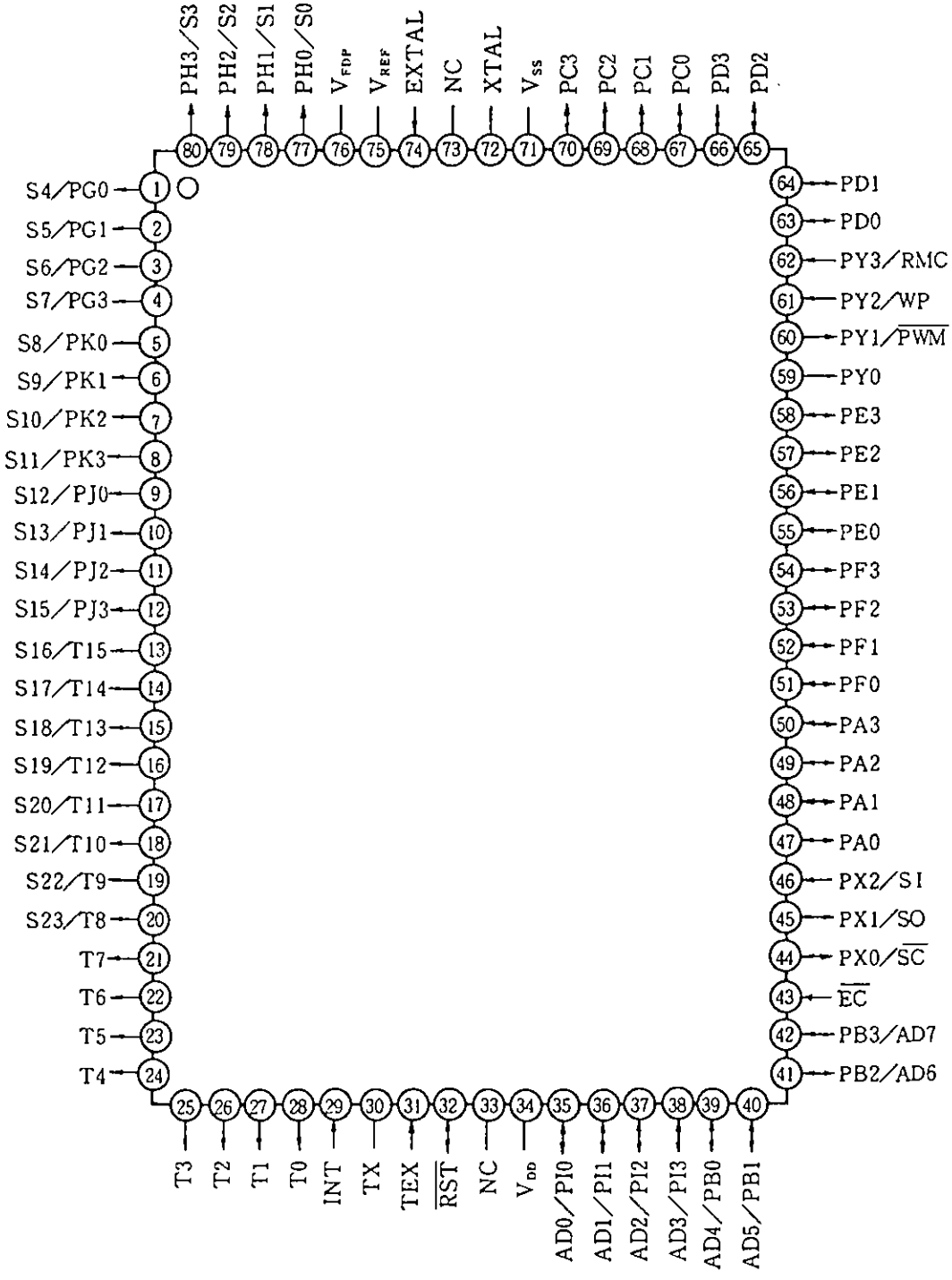
Silicon gate CMOS IC

E90379-HP

Block Diagram

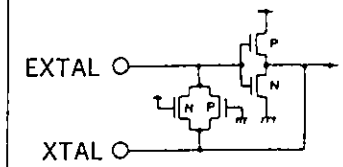
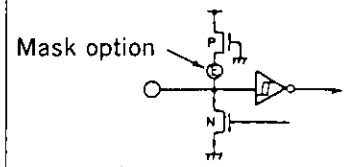
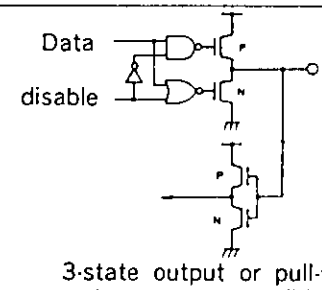


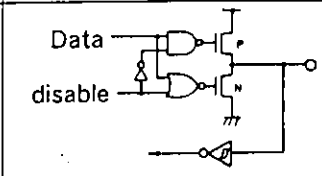
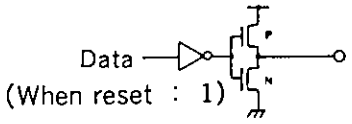
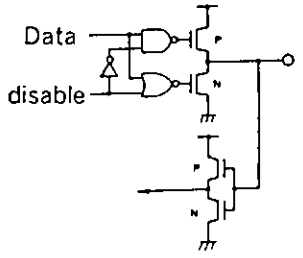
Pin Configuration (Top View)

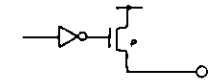
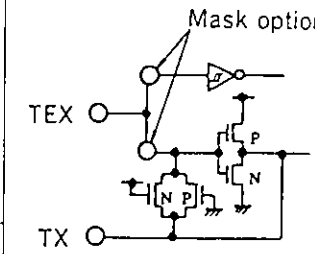


Note) Do not make any connections to NC pins.

Pin Description

Symbol	Name	I/O	Description	Equivalent circuit
V_{DD}	Supply voltage	—	Positive power supply pin	
V_{SS}	Grounding voltage	—	GND pin	
EXTAL	Clock input	I	Clock generation circuit input pin. Connect the crystal oscillator or ceramic resonator between the EXTAL and XTAL. To use an external clock input, connect the clock oscillation source to the EXTAL pin and open the XTAL pin.	
XTAL	Clock output	O	Output pin of the clock generation circuit	
$\overline{RST}$	Reset	I/O	Serves as the incorporated power on reset circuit output pin. When inputting a reset signal from the outside, provide 2 instruction cycles or longer of an "L" level (0V).	 Output pull-up resistor (P-ch Tr) N-ch Tr output Schmitt inverter input
INT	External interrupt	I	Serves as interrupt input pin. Permits the selection with a program of the edge and the level modes.	 Schmitt inverter
$\overline{EC}$	Event count input	I	Event counter input pin	
SI/PX2	Serial input Port X	I	Doubles as a serial interface (8 bits) input pin and as bit "2" (input) of port X	
SO/PX1	Serial output Port X	I/O	Doubles as a serial interface (8 bits) output pin and as bit "1" (input) of port X	 3-state output or pull-up resistor output possible Inverter input

Symbol	Name	I/O	Description	Equivalent circuit
$\overline{SC}$/PX0	Serial clock Port X	I/O	Doubles as clock input/output pin for the serial interface and as bit "0" (input) of port X	 3-state output or pull-up resistor output possible Schmitt input
RMC/PY3	Remote control input Port Y	I	Doubles as a remote control reciver input pin and as bit "3" (input) of port Y	 Schmitt inverter
WP/PY2	Wake-up input Port Y	I	Doubles as a wake-up input pin to release the standby state and as bit "2" (input) or port Y.	
$\overline{PWM}$/PY1	PWM output Port Y	O	Doubles as a PWM generator (14 bits) output and as bit "1" (output) of port Y	 Inverter output
PY0	Port Y	O	Output pin for bit "0" of port Y	
PA0toPA3	Port A	I/O	This 4-bit input/output port permits its each individual port to be programmed to serve for input or output. Its output format is a 3-state or pull-up resistor output.	 3-state output or pull-up resistor output possibl Inverter input
PB0/AD4to PB3/AD7	Port B/ Analog input	I/O	This 4-bit input/output port has the functions that are equivalent to those of port A. It is also used for A/D converter input.	
PC0toPC3	Port C	I/O	This 4-bit input/output port permits its each individual port to be programmed to serve for input or output. Its output format is a 3-state or pull-up resistor output.	
PD0toPD3	Port D	I/O	This 4-bit input/output port has the functions that are equivalent to those of port C.	
PE0toPE3	Port E	I/O	This 4-bit input/output port has the functions that are equivalent to those of port C.	
PF0toPF3	Port F	I/O	This 4-bit input/output port has the functions that are equivalent to those of port C.	
PI0/AD0to PI3/AD3	Port I/ Analog input	I/O	This 4-bit input/output port has the functions that are equivalent to those of port C. It is also used for A/D converter input.	

Symbol	Name	I/O	Description	Equivalent circuit
V_{FDP}	Power supply for FDP	—	Load power supply pin needed when load resistance is built in to output driver for FDP (Fluorescent Display Tube).	
T0toT7	Timing	O	Lower 8-digit output pin of the FDP timing signal	 P-ch open drain output Pull-down resitance (Mask option)
T8/S23to T15/S16	Timing/ Segment	O	Combination output pin of higher 8-digit of the FDP timing signal and as the segment signal	
PG0/S4to PG3/S7	Port G/ Segment	O	Doubles as 4-bit output port and as FDP segment signal output	
PH0/S0to PH3/S3	Port H/ Segment	O	The same as Port G	
PJ0/S12to PJ3/S15	Port J/ Segment	O	The same as Port G	
PK0/S8to PK3/S11	Port K Segment	O	The same as Port G	
TEX	32kHz T/C Clock input	I	Input pin of the 32kHz timer clock generation circuit. Connect 32.768kHz crystal oscillator between TEX and TX. To use as event clock input, connect the clock oscillation source to the TEX pin and open the TX pin.	
TX	32kHz T/C Clock output	O	Output pin of the clock generation circuit	
V_{REF}	Reference voltage input	I	Reference voltage input for power supply voltage reset circuit. Connect the zener diode normally.	

Absolute Maximum Ratings (Ta=−20°Cto+75°C, V_{SS}=0V)

Item	Symbol	Ratings	Unit	Remarks
Power supply voltage	V_{DD}	−0.3to+7.0	V	
Input voltage	V_{IN}	−0.3to+7.0*1	V	
Output voltage	V_{OUT}	−0.3to+7.0*1	V	
Display output voltage	V_{OD}	V_{DD}−40toV_{DD}+0.3	V	As P channel transistor is open drain, V_{DD} voltage is determined as standard.
High level output current	I_{OH}	−5	mA	Other than display output pins*2 : per pin
	I_{ODH1}	−15	mA	Display output S0 to S15 : per pin
	I_{ODH2}	−35	mA	Display output T0 to T7, T8/S23 to T15/S16 : per pin
High level total output current	ΣI_{OH}	−40	mA	Total of other than display output pins
	ΣI_{ODH}	−100	mA	Total of display output pins
Low level output current	I_{OL}	15	mA	Port 1 pin
	I_{OLC}	20	mA	High current port : per pin*3
Low lovel total output current	ΣI_{OL}	100	mA	Total of entire pins
Operating temperature	T_{opr}	−20to+75	°C	
Storage temperature	T_{stg}	−55to+150	°C	
Allowable power dissipation	P_D	600	mW	

*1) V_{IN} and V_{OUT} should not exceed V_{DD} +0.3V.

*2) Specifies the output current of the general purpose I/O port PA to PF, PI, SO, $\overline{SC}$, PY0 and PY1.

*3) The high current operation transistors are the N-ch transistors of ports PC and PD.

Note) Usage exceeding absoute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (V_{SS}=0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	4.5	5.5	V	Guaranteed range of operation by EXTAL clock
		2.5	5.5	V	Guaranteed range of operation by TEX clock, guaranteed range of data hold during STOP
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*1
	V_{IHEX}	V_{DD}−0.4	V_{DD}+0.3	V	EXTAL pin*2
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*1
	V_{ILEX}	−0.3	0.4	V	EXTAL pin*2
Operating temperature	T_{opr}	−20	+75	°C	

*1) The TEX pin when the counter mode is selected by each of INT, $\overline{EC}$, PX0, PX2, PY2, PY3 and $\overline{RST}$ pins and mask option.

*2) Specified only during external clock input.

Electrical Characteristics

DC characteristics (Ta=−20°Cto+75°C, V_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA~PF, PI PX0, PX1	V_{DD}=4.5, I_{OH}=−0.5mA	4.0			V
			V_{DD}=4.5V, I_{OH}=−1.0mA	3.5			V
Low level output voltage	V_{OL}	PY0, PY1	V_{DD}=4.5V, I_{OL}=1.8mA			0.4	V
		$\overline{RST}$(V_{OL} only)	V_{DD}=4.5V, I_{OL}=3.6mA			0.6	V
		PC, PD	V_{DD}=4.5V, I_{OL}=12mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD}=5.5V, V_{IH}=5.5V	0.5		40	μA
	I_{ILE}		V_{DD}=5.5V, V_{IL}=0.4V	−0.5		−40	μA
	I_{IHT}	TEX*3	V_{DD}=5.5V, V_{IH}=5.5V	0.1		10	μA
	I_{ILT}		V_{DD}=5.5V	−0.1		−10	μA
	I_{ILR}	$\overline{RST}$*2	V_{IL}=0.4V	−1.5		−400	μA
Display output current	I_{OH}	S0toS15	V_{DD}=4.5V V_{OH}=V_{DD}−2.5V	−7			mA
		S16/T15toS23/T8 T0toT7		−18			mA
Open drain output leakage current (P-ch Tr OFF in state)	I_{LOL}	S0toS15 S16/T15toS23/T8 T0toT7	V_{DD}=5.5V V_{OL}=V_{DD}−35V			−20	μA
Pull-down resistance*1	R_L	S0toS15 S16/T15toS23/T8 T0toT7	V_{DD}=5V V_{FDP}=V_{DD}−35V	60	100	270	kΩ
High impedance I/Oleakage current	I_{IZ}	PAtoPF, PI PX0toPX2, PY2, PY3, EC INT, TEX*3, $\overline{RST}$*2	V_{DD}=5.5V V_I=0, 5.5V			±10	μA
Current power supply	I_{DD1}	V_{DD}	Entire output pins open V_{DD}=5.5V, 4.19MHz crystal oscillation (C1=C2=22pF)		7	20	mA
	I_{DD2}		V_{DD}=3V, 32kHz crystal oscillation (C1=C2=18pF)		50	250	μA
	I_{DDSP1}		SLEEP mode V_{DD}=5.5V, 4.19MHz oscillation		5	12	mA
	I_{DDSP2}		V_{DD}=3V, 32kHz oscillation		40	200	μA
	I_{DDS1}		STOP mode V_{DD}=3V, 32kHz with T/C		7	40	μA
	I_{DDS2}		V_{DD}=5.5V, 32kHz without T/C (For mask option select counter, Pin is fixed.)			10	μA
Input capacitance	C_{IN}	PAtoPF, PI, PX PY2, PY3, EXTAL, TEX, $\overline{RST}$, INT, EC	Fc=1MHz 0V other than the measured pins		10	20	pF

*1) In case the incorporated pull-down resistance has been selected with mask option.

*2) $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when nonresistance is selected.

*3) The TEX pin specifies the input current when the 32kHz oscillation is selected by the mask option, and specifies the leakage current when the counter mode is selected.

AC characteristics

(1) Clock timing (Ta=−20°Cto+75°C, V_{DD}=4.5V to 5.5V, V_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig.1, Fig.2	1		5	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig.1, Fig.2 External clock drive	90			ns
System clock input rising and falling times	t_{CR} t_{CF}	EXTAL	Fig.1, Fig.2 External clock drive			200	ns
System clock frequency	f_{CS}	TEX*2 TX	V_{DD}=2.5 to 5.5V Fig.3		32.768		kHz
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{EC}$	Fig.4	tsys*1 +0.05			μs
Event count clock input rising and falling times	t_{ER} t_{EF}	$\overline{EC}$	Fig.4			20	ms
Event count input clock pulse width	t_{TL} t_{TH}	TEX*3	Fig.4	10			μs
Event count input clock rising and falling times	t_{TR} t_{TF}	TEX*3	Fig.4			20	ms

*1) tsys in the EXTAL input clock is tsys=8/fc
tsys in the TEX input clock is tsys=4/fcs

*2) Specified when the crystal oscillation mode is selected by the mask option.

*3) Specified when the counter mode is selected by the mask option

Note) When adjusting the frequency accurately, there may be cases in which they may differ from Fig.2.

Fig.1 Clock timing

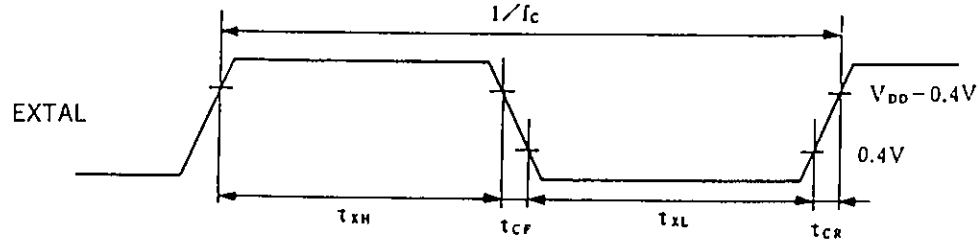


Fig.2 Clock applying condition

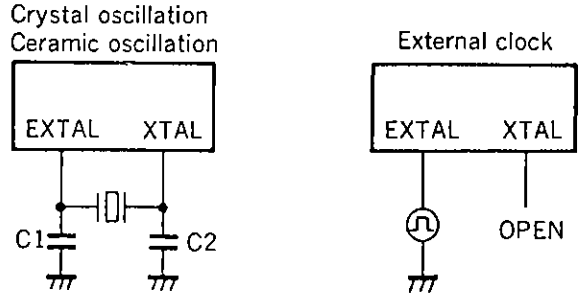


Fig.3 32kHz clock applying condition

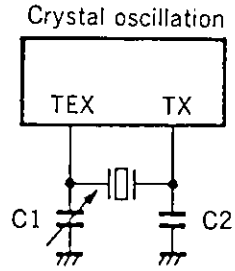
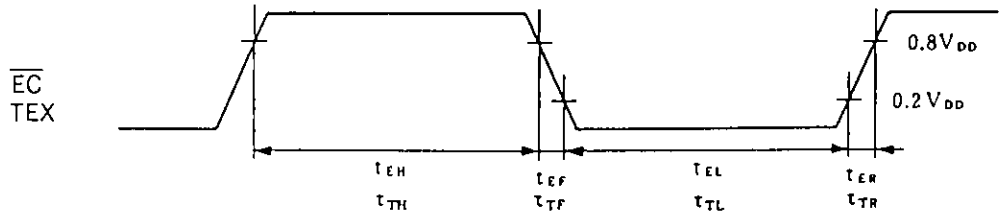


Fig.4 Event count clock timing

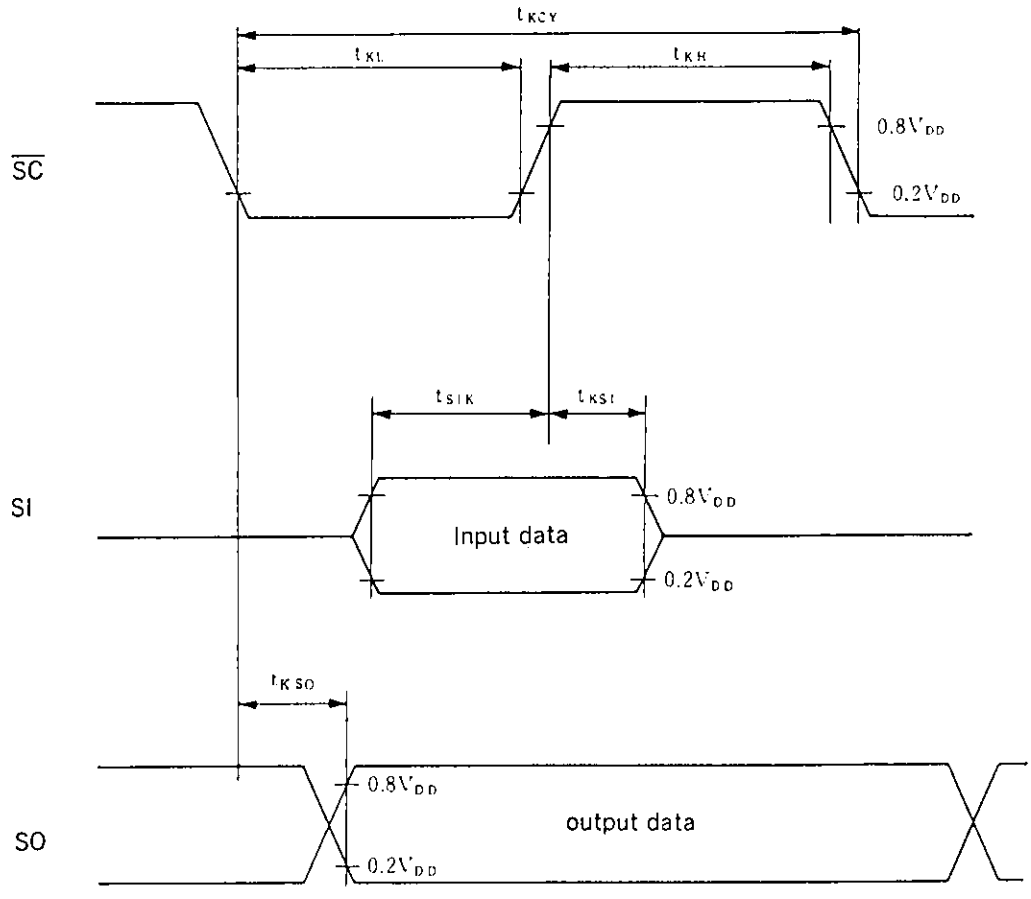


(2) Serial transfer (Ta=−20°Cto+75°C, V_{DD}=4.5V to 5.5V, V_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Serial transfer clock ($\overline{SC}$) cycle time	t_{KCY}	$\overline{SC}$	Input mode	tsys/4+1.42		μs
			Output mode	t_{SIO}		μs
Serial transfer clock ($\overline{SC}$) high and low level widths	t_{KH} t_{KL}	$\overline{SC}$	Input mode	tsys/8+0.7		μs
			Output mode	t_{SIO}/2−0.1		μs
Serial data input setup time (against $\overline{SC}$ ↑)	t_{SIH}	SI	$\overline{SC}$ input mode	0.1		μs
			$\overline{SC}$ output mode	0.2		μs
Serial data input hold time (against $\overline{SC}$ ↑)	t_{KSI}	SI	$\overline{SC}$ input mode	tsys/8+0.5		μs
			$\overline{SC}$ output mode	0.1		μs
Data output delay time from $\overline{SC}$ falling	t_{KSO}	SO			tsys/8+0.5	μs

Note) 1.tsys in the EXTAL input clock is tsys=8/fc (It cannot be used in the TEX input clock.)
t_{SIO} in turned into either 2tsys, 4tsys or 16tsys by means of a program.
Note) 2.The load of data output delay time is 50pF +1TTL.

Fig.5 Serial transfer timing



(3) A/D converter (Ta=−20°Cto+75°C, V_{SS}=0V)

Analog input voltage	Pin	Condition	Digital conversion value
0.0to0.33V	AD0toAD7	V_{DD}=5V	000
0.82to1.29V			001
1,78to2.21V			010
2.69to3.06V			011
3.56to4.06V			100
4.62to5.0V			101

Note) The digital conversion value are the values when FF_H address in the program are read.

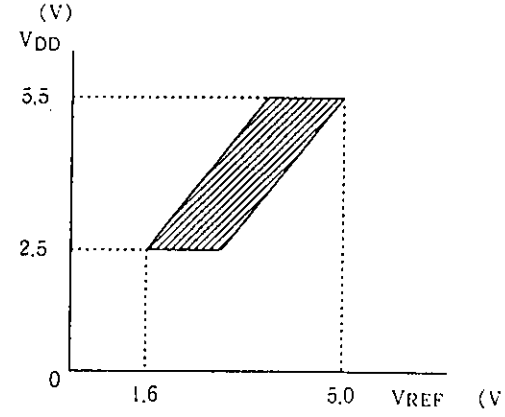
(4) Power supply voltage detection reset function (Ta=−20°Cto+75°C, V_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply voltage detection reset function operating voltage range	V_{LPOP}	V_{DD}	Voltage range allowing system operation (32kHz system operation at V_{DD}=4.5V or less.)	2.5		5.5	V
Power supply voltage drop detection function	V_{POP}	V_{DD}	When V_{REF} pin voltage is 3.3V Flag set during voltage falling System reset during voltage rising	3.8	4.0	4.2	V

The chart in Fig.6 shows the relationship between the power supply voltage V_{DD} and referance voltage V_{REF} of the power supply voltage detection reset function.

Note) The chart in Fig.6 serves as guide to the function operation area obtained using average devices. Individual adjustment is needed when zener diodes and others are connected to the V_{REF} pin.

Fig.6 Power supply voltage detection reset function chart



(5) Others (Ta=−20°Cto+75°C, V_{DD}=4.5V to 5.5V, V_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH}, t_{IL}	INT	Edge detection mode	tsys+0.05		μs
Reset input low leve width	t_{RSL}	$\overline{RST}$		2tsys*1		μs
Wake-up input high level width	t_{WPH}	WP	STOP mode	500		ns
			SLEEP mode	tsys+0.05		μs
Wake-up input high and low level widths	t_{PWH}, t_{PWL}	PA		500		ns

Note) tsys in the EXTAL input clock is 8.fc
tsys in the TEX input clock is 4/fcs

*1) For reset during operating in TEX input clock, hold the low level more than the oscillation stabilizing time of EXTAL input clock.

Fig.7 Interruption input timing

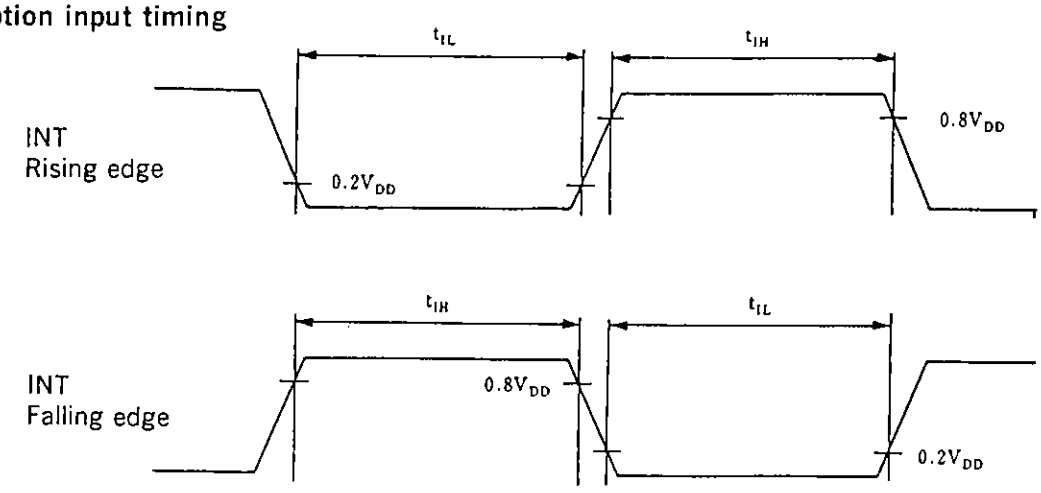


Fig.8 $\overline{\text{Reset}}$ input timing

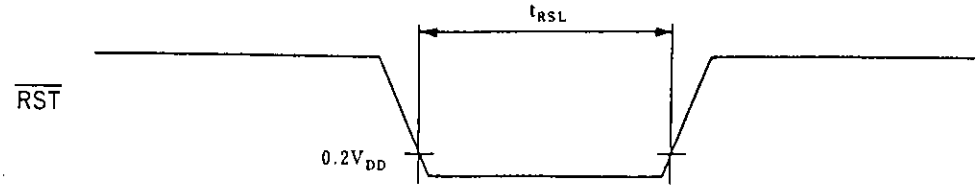


Fig.9 Wake-up input timing

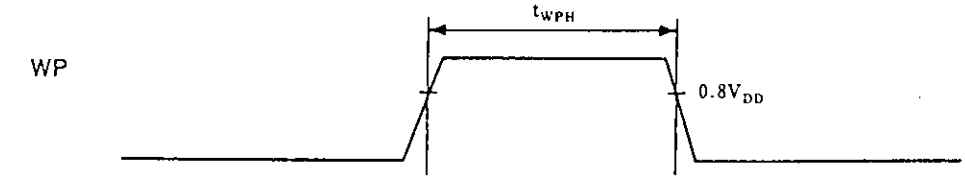
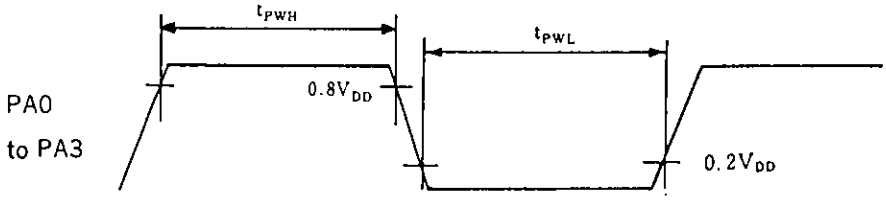


Fig.10 Wake-up input timing

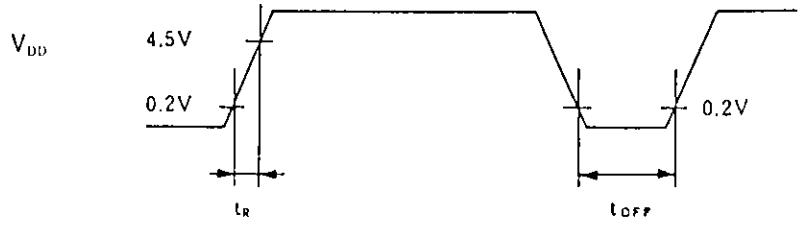


Power on reset* (Ta=−20°Cto+75°C, V_{SS}=0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specified only when power on reset function is selected.

Fig.11 Power on reset

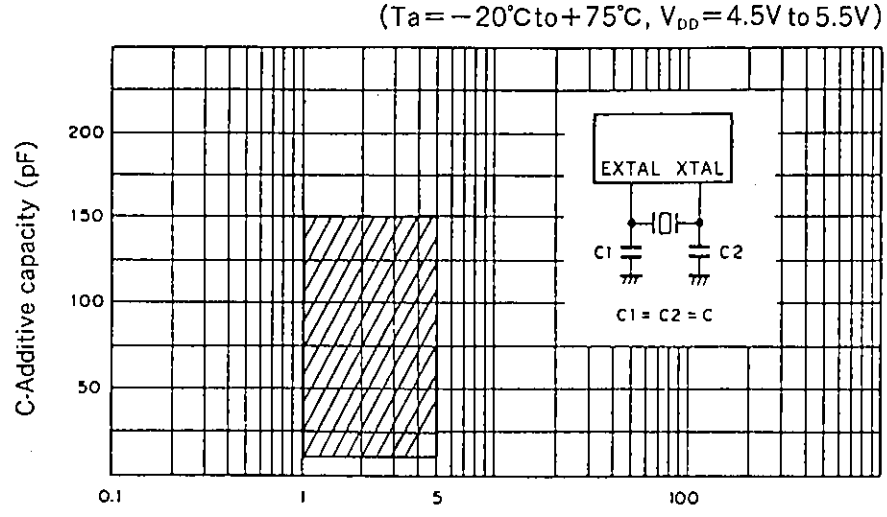


The power supply should rise smoothly.

Notes on Operation

See Fig.12 additive capacity calculation chart and select the appropriate capacity when using the crystal oscillator.

Fig.12 Crystal oscillation circuit additive capacity calculation chart

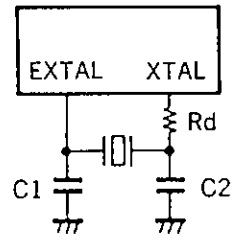


(Note) The above chart shows a range in which the average quartz resonator has a relatively fast oscillation rising edge and stable characteristics. The capacity should be selected to correspond to the appropriate constant for each quartz resonator, should the frequency of the quartz resonator be accurately adjusted.

Fig.13 shows recommended circuits and oscillators. Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

Fig.13 Oscillation recommended circuit

(i) Main clock (4.19MHz)

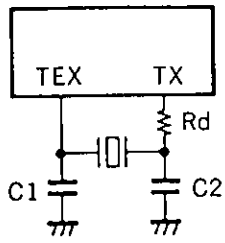


(i)

Manufacturer	Model	Frequency	C1	C2	Rd
MURATA MFG CO., LTD.	CSA4.19MG040	4.19 MHz	100pF	100pF	—
	CST4.19MGW040	4.19 MHz	— (built in)	— (built in)	—

Manufacturer	Model	Frequency	C1	C2	Rd
CITIZEN WATCH CO., LTD.	CSA-309	4.19 MHz	10pF (20pF trimmer)	10pF	—
NIHON DENPA KOGYO CO., LTD.	AT-51	4.19 MHz	15pF (20pF trimmer)	15pF	6.8kΩ
KINSEKI LTD.	HC-49/U-S	4.19 MHz	22pF	22pF	3.3kΩ

(ii) Sub clock (32kHz)

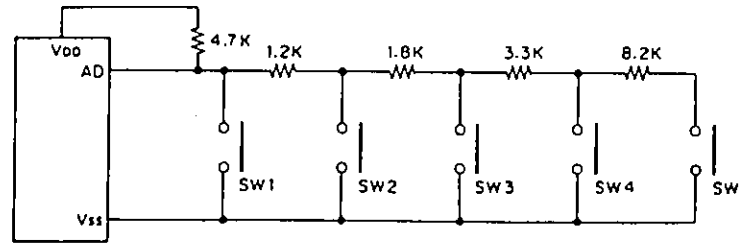


(ii)

Manufacturer	Model	Frequency	C1	C2	Rd
CITIZEN WATCH CO., LTD.	CFS-308	32.768 kHz	18pF (20pF trimmer)	18pF	—
NIHON DENPA KOGYO CO., LTD.	MX-38T	32.768 kHz	22pF (20pF trimmer)	22pF	470kΩ
KINSEKI LTD.	P3	32.768 kHz	22pF (20pF trimmer)	22pF	330kΩ

When using the A/D converter as the key input, it is recommended that the circuit structure shown in Fig.14 be used.

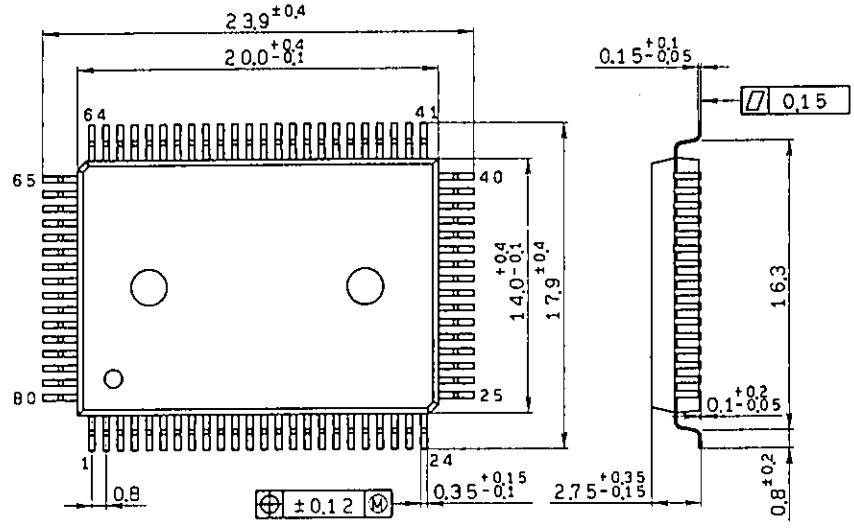
Fig.14 Recommended example of key input circuit by A/D converter



(Precision of resistance is all whithin ±5%)

Package Outline Unit : mm

80pin QFP (Plastic) 1.6g



SONY NAME	QFP-80P-L01
EIAJ NAME	•QFP080-P-1420-A
JEDEC CODE	———