I. GENERAL DESCRIPTION

EM78P447S is an 8-bit microprocessor with low-power and high-speed CMOS technology. There is a 4096*13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM) within it. It provides a PROTECTION bit to prevent a user's code from intruding as well as 8 other OPTION bits to match the user's requirements.

Because of the OTP-ROM, the EM78P447S offers users a convenient way to develop and verify their programs. Moreover, a user's developed code can be programmed easily by an EMC writer.

II. FEATURES

- Operating voltage range: 2.2V~5.5V
- Available in temperature range: 0°C~70°C
- Operating frequency range: DC ~ 20MHz
- Low power consumption:
  * less than 2.2 mA at 5V/4MHz
  * typical of 30μA at 3V/32KHz
  * typical of 1μA during the sleep mode
- 4096 x 13 bits on chip ROM
- 148 x 8 bits on chip registers (SRAM)
- 3 bi-directional I/O ports
- 5 level stacks for subroutine and interrupt
- 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
- Power-down mode (SLEEP mode)
- Two available interruptions
  * TCC overflow interrupt
  * External interrupt(INT pin)
- Programmable free running watchdog timer
- 10 programmable pull-high I/O pins
- 2 programmable R-option I/O pins
- 2 programmable open-drain I/O pins
- Two clocks per instruction cycle
- 99.9% single instruction cycle commands
- Package type:
  * 28 pin DIP and SOIC (EM78P447SA)
  * 32 pin DIP and SOIC (EM78P447SB)

III. PIN ASSIGNMENTS

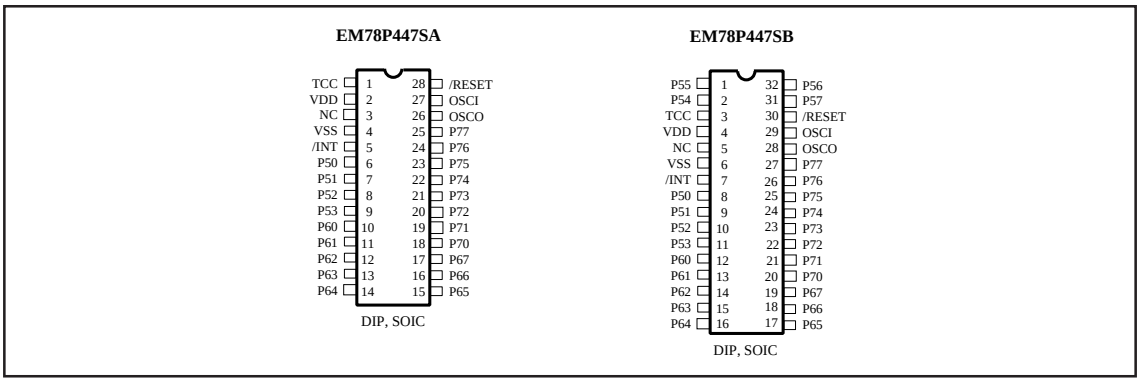


Fig. 1 Pin assignments

IV. FUNCTIONAL BLOCK DIAGRAM

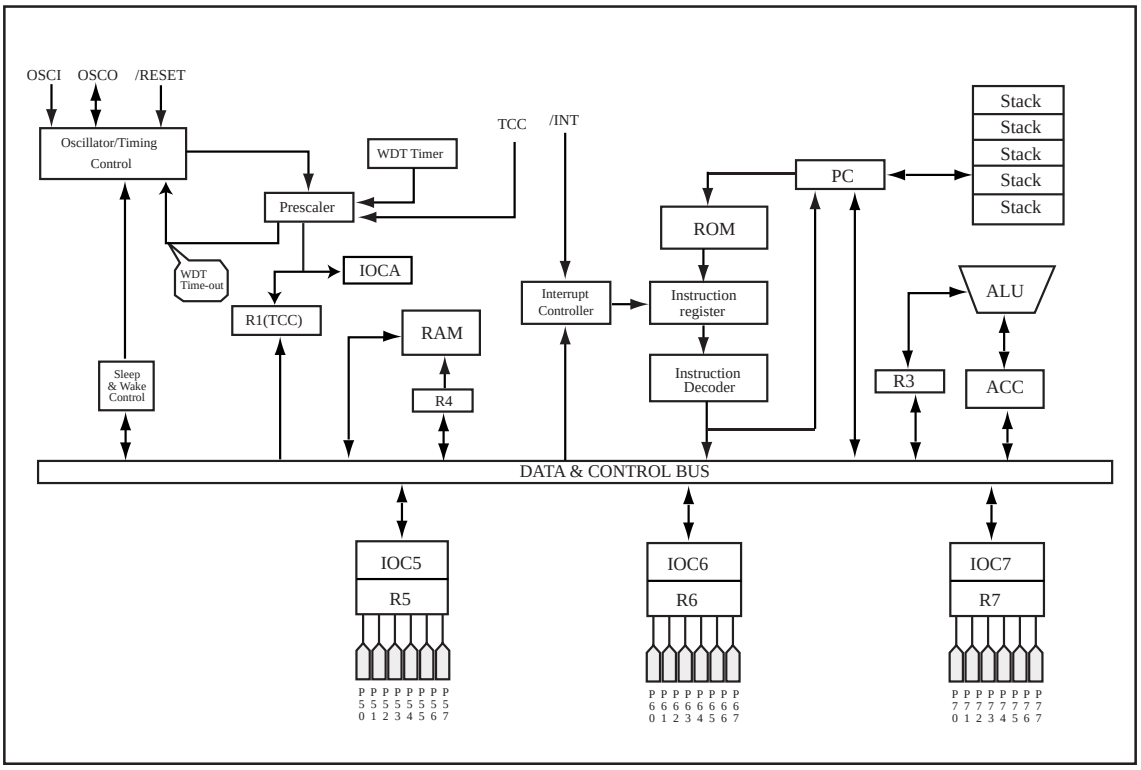


Fig. 2 Functional block diagram

V. PIN DESCRIPTION

Table 1 Pin description -EM78P447SA

Symbol	Type	Function
VDD	-	* Power supply.
OSCI	I	* XTAL type : Crystal input terminal or external clock input pin. * RC type : RC oscillator input pin.
OSCO	I/O	* XTAL type : Output terminal for crystal oscillator or external clock input pin. * RC type : Instruction clock out. * External clock signal input.
/INT	I	* External interrupt pin triggered by falling edge.
P70~P77	I/O	* General-purpose I/O pin.
P60~P67	I/O	* General-purpose I/O pin.
P50~P53	I/O	* General-purpose I/O pin.
/RESET	I	* If the pin remains logic low, the device will be in reset.
NC	-	* No connection.
TCC	I	* External Counter input.
VSS	-	* Ground.

Table 2 Pin description -EM78P447SB

Symbol	Type	Function
VDD	-	* Power supply.
OSCI	I	* XTAL type : Crystal input terminal or external clock input pin. * RC type : RC oscillator input pin.
OSCO	I/O	* XTAL type : Output terminal for crystal oscillator or external clock input pin. * RC type : Instruction clock out. * External clock signal input.
/INT	I	* External interrupt pin triggered by falling edge.
P70~P77	I/O	* General-purpose I/O pin.
P60~P67	I/O	* General-purpose I/O pin.
P50~P57	I/O	* General-purpose I/O pin.
/RESET	I	* If the pin remains logic low, the device will be in reset.
NC	-	* No connection.
TCC	I	* External Counter input.
VSS	-	* Ground.

VI. FUNCTION DESCRIPTIONS

VI.1 Operational Registers

1. R0 (Indirect Addressing Register)

R0 is not a physically implemented register. Its major function is to be an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses the data pointed by the RAM Select Register (R4).

2. R1 (Time Clock /Counter)

- Increased by an external signal edge which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.
- The signals to increase the counter are decided by bit 4 and bit 5 of the CONT register.
- Writable and readable as any other registers.

3. R2 (Program Counter) & Stack

- Depending on the device type, R2 and hardware stacks are 12-bit wide. The structure is depicted in Fig. 3.
- Generating 4096x13 bits on-chip OTP ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are set all “0”s upon a RESET condition.
- “JMP” instruction allows the direct loading of the lower 10 program counter bits. Thus, “JMP” allows PC to go to any location within a page.
- “CALL” instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can locate anywhere within a page.
- “RET” (“RETL K”, “RETI”) instruction loads the program counter with the contents of the top-level stack.
- “ADD R2, A” allows a relative address to be added to the current PC, and the ninth and tenth bits of the PC are cleared.
- “MOV R2, A” allows to load an address from the “A” register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC are cleared.
- Any instruction which would modify the contents of R2 (e.g. “ADD R2, A”, “MOV R2, A”, “BC R2, 6”,.....) will cause the ninth bit and the tenth bits (A8~A9) of the PC to be cleared. Thus, the computed jump is limited to the first 256 locations of a page.
- The two most significant bits (A11 and A10) will be loaded with the contents of PS1 and PS0 in the status register (R3) upon the execution of a “JMP”, “CALL”, or any other instructions which would change the contents of R2.
- All instructions are single instruction cycle (*f*clk/2) except the instructions which would change the contents of R2 need one more instruction cycle.

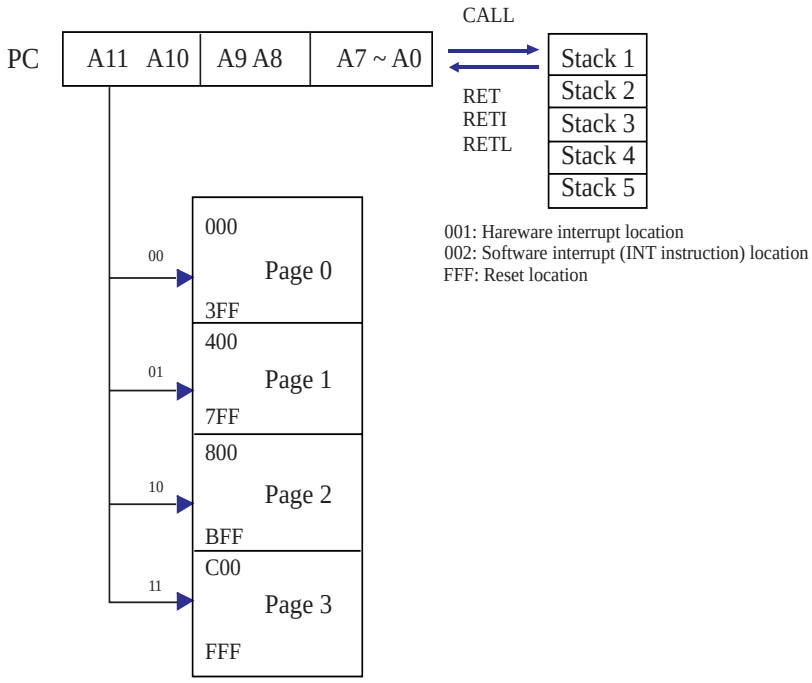


Fig. 3 Program counter organization

4. R3 (Status Register)

7	6	5	4	3	2	1	0
GP	PS1	PS0	T	P	Z	DC	C

- Bit 0 (C) Carry flag
- Bit 1 (DC) Auxiliary carry flag
- Bit 2 (Z) Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.
- Bit 3 (P) Power-down bit. Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.
- Bit 4 (T) Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands, or during power-up and reset to 0 by WDT time-out.
- Bit 5 (PS0) ~ 6 (PS1) Page-selecting bits.
  PS0~PS1 are used to select a program memory page. When executing "JMP", "CALL", or other instructions which cause the program counter to be changed (e.g. MOV R2,A), PS0~PS1 are loaded to the 11th and 12th bits of the program counter which would select one of the available program memory pages. Note that RET, RETL and RETI instructions do not change the PS0~PS1 bits. That is, the return will be always to the page from the place where the subroutine was called, regardless of the current setting of PS0~PS1 bits.

PS1	PS0	Program memory page [Address]
0	0	Page 0 [000-3FF]
0	1	Page 1 [400-7FF]
1	0	Page 2 [800-BFF]
1	1	Page 3 [C00-FFF]

- Bit 7(GP) General read/write bit.

5. R4 (RAM Select Register)

- Bits 0~5 are used to select registers (address: 00~3F) in the indirect addressing mode.
- Bit 6~7 are used to select bank 0 ~ 4.
- See the configuration of the data memory in Fig. 4.

6. R5 ~ R7 (Port 5 ~ Port 7)

- R5, R6 and R7 are I/O registers.

7. R8~R1F, R20~R3E(General-purpose Register)

- R8~R1F and R20~R3E (including Bank 0~3) are general-purpose registers.

8. R3F (Interrupt Status Register)

7	6	5	4	3	2	1	0
-	-	-	-	EXIF	-	-	TCIF

- Bit 0 (TCIF) TCC overflowing interrupt flag. Set when TCC overflows, reset by software.
- Bit 3 (EXIF) External interrupt flag. Set by falling edge on /INT pin, reset by software.
- Bits1~2 and 4~7 Not used.
- “1” means interrupt request, and “0” means non-interrupt occurrence.
- R3F can be cleared by instruction but can not be set.
- IOCF is the interrupt control register.
- Note that the result of reading R3F is the “logic AND” of R3F and IOCF.

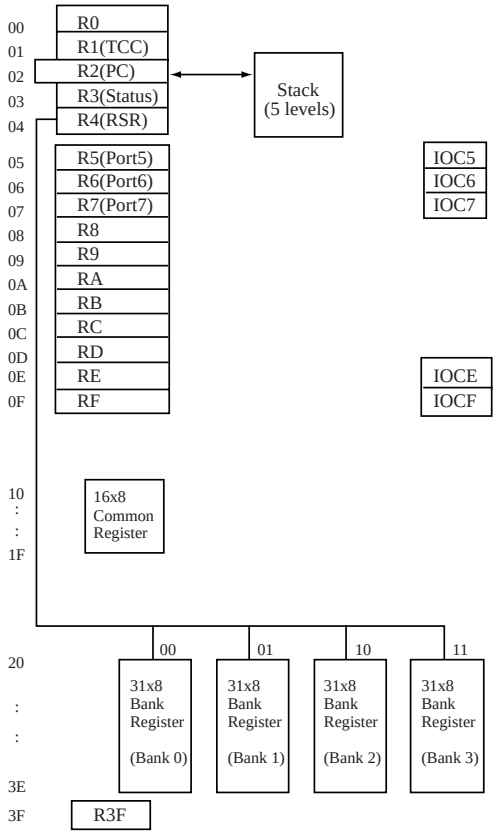


Fig. 4 Data memory configuration

VI.2 Special Purpose Registers

1. A (Accumulator)

- Internal data transfer, or instruction operand holding
- It can not be addressed.

2. CONT (Control Register)

7	6	5	4	3	2	1	0
/PHEN	/INT	TS	TE	PAB	PSR2	PSR1	PSR0

- Bit 0 (PSR0) ~ Bit 2 (PSR2) TCC/WDT prescaler bits.

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- Bit 3 (PAB) Prescaler assignment bit.
  0: TCC.
  1: WDT.
- Bit 4 (TE) TCC signal edge
  0: increment if the transition from low to high takes place on the TCC pin.
  1: increment if the transition from high to low takes place on the TCC pin.
- Bit 5 (TS) TCC signal source
  0: internal instruction cycle clock.
  1: transition on the TCC pin.
- Bit 6 (INT) Interrupt enable flag
  0: masked by DISI or hardware interrupt.
  1: enabled by the ENI/RETI instruction.
- Bit 7 (/PHEN) Control bit used to enable the pull-high of the P60~P67, P74 and P75 pins.
  0: Enable internal pull-high.
  1: Disable internal pull-high.
- CONT register is both readable and writable.

3. IOCB (Wake-up Control Register for Port6)

7	6	5	4	3	2	1	0
/WUE7	/WUE6	/WUE5	/WUE4	/WUE3	/WUE2	/WUE1	/WUE0

- Bit 0 (/WUE0) Control bit used to enable the wake-up function of P60 pin.
  0: Enable the wake-up function.
  1: Disable the wake-up function.
- Bit 1 (/WUE1) Control bit used to enable the wake-up function of P61 pin.
- Bit 2 (/WUE2) Control bit used to enable the wake-up function of P62 pin.
- Bit 3 (/WUE3) Control bit used to enable the wake-up function of P63 pin.
- Bit 4 (/WUE4) Control bit used to enable the wake-up function of P64 pin.
- Bit 5 (/WUE5) Control bit used to enable the wake-up function of P65 pin.
- Bit 6 (/WUE6) Control bit used to enable the wake-up function of P66 pin.
- Bit 7 (/WUE7) Control bit used to enable the wake-up function of P67 pin.

4. IOCE (WDT Control Register)

7	6	5	4	3	2	1	0
-	ODE	WTE	SLPC	ROC	-	-	/WUE

- Bit 0 (/WUE) Control bit used to enable the wake-up function of P74 and P75.
  0: Enable the wake-up function.
  1: Disable the wake-up function.
- Bit 3 (ROC) ROC is used for the R-option. Setting ROC to "1" will enable the status of R-option pins (P70, P71) to be read by the controller. Clearing ROC will disable the R-option function. Otherwise, the R-option function is introduced. Users must connect the P71 pin or/and P70 pin to VSS by a 560KΩ external resistor (Rex). If Rex is connected/disconnected with VDD, the status of P70 (P71) will be read as "0"/"1". Refer to Fig. 7(b).
- Bit 4 (SLPC) This bit is set by hardware at the falling edge of wake-up signal and is cleared in software. SLPC is used to control the operation of oscillator. The oscillator is disabled (oscillator is stopped, and the controller enters the SLEEP2 mode) on the high-to-low transition and is enabled (the controller is awakened from SLEEP2 mode) on the low-to-high transition. In order to ensure the stable output of the oscillator, once the oscillator is enabled again, there is a delay for approximately 18 ms (oscillator start-up timer, OST) before the next instruction of program being executed. The OST is always activated by wake-up from sleep mode whether the Code option bit WTC is "0" or not. After waking up, the WDT is enabled if Code Option WTC is "1". The block diagram of SLEEP2 mode and wake-up caused by input triggered are depicted in Fig. 5.
- Bit 5 (WTE) Control bit used to enable Watchdog Timer.
  The WTE bit is used only if WTC, the CODE option bit, is "1". If the WTC bit is "1", then WDT can be disabled/enabled by the WTE bit.
  0: Disable WDT.
  1: Enable WDT.
  The WTE bit is not used if WTC, the CODE option bit WTC, is "0". That is, if the WTC bit is "0", WDT is always disabled no matter what the WTE bit is.
- Bit 6 (ODE) Control bit used to enable the open-drain of P76 and P77 pins.
  0: Disable open-drain output
  1: Enable open-drain output
- IOCE register is both readable and writable.
- Bits 1~2,7 Not used.

5. IOCF (Interrupt Mask Register)

7	6	5	4	3	2	1	0
-	-	-	-	EXIE	-	-	TCIE

- Bit 0 (TCIE) TCIF interrupt enable bit.
  0: disable TCIF interrupt
  1: enable TCIF interrupt
- Bit 2 (EXIE) EXIF interrupt enable bit.
  0: disable EXIF interrupt
  1: enable EXIF interrupt
- Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

- Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 9.
- IOCF register is both readable and writable.

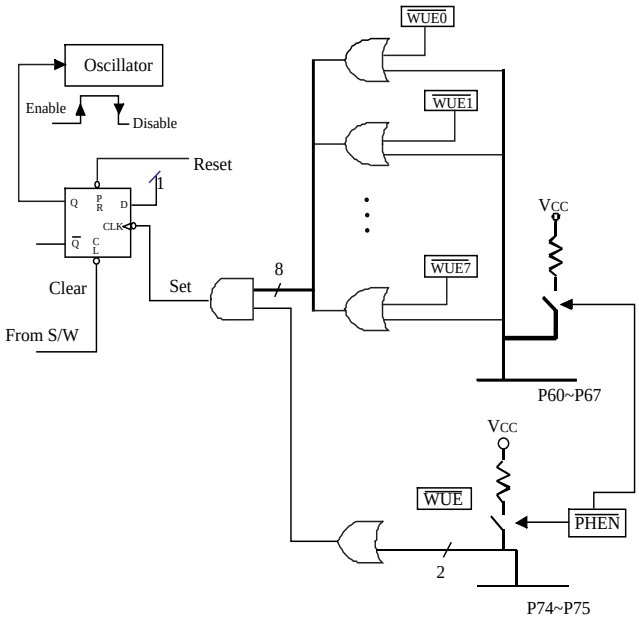


Fig. 5 Block diagram of sleep mode and wake-up circuits on I/O ports

VI.3 TCC/WDT & Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available only for either the TCC or the WDT at the same time and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler will be cleared by the instructions which write to TCC each time, when assigned to TCC mode. The WDT and prescaler, when assigned to WDT mode, will be cleared by the WDTC" and "SLEP" instructions. Fig. 6 depicts the circuit diagram of TCC/WDT.

- R1(TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external clock input (edge selectable from TCC pin). If TCC signal source is from internal clock, TCC will increase by 1 in every instruction cycle (without prescaler). Refer to Fig. 6, CLK=Fosc/2 or CLK=Fosc/4 is depended on the CODE option bit CLKS. CLK=Fosc/2 if CLKS bit is "0", and CLK=Fosc/4 if CLKS bit is "1".

- If TCC signal source is from external clock input, TCC will increase by 1 on every falling edge or rising edge of TCC pin.

- The watchdog timer is a free running on-chip RC oscillator. The WDT will keep running even the oscillator driver has been turned off (i.e. in sleep mode). During the normal operation or the sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during the normal mode by software programming. Refer to WDTE bit of IOC0E register. With no presacler, the WDT time-out period is approximately 18 ms.

VI.4 I/O Ports

The I/O registers, Port 5, Port 6 and Port 7, are bi-directional tri-state I/O ports. The function of Pull-high, R-option and Open-drain can be enabled internally by CONT and IOCE respectively. There is an input status changed interrupt (or wake-up) function on Port 6, P74 and P75. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC7). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6 and Port 7 are shown in Fig. 7 (a) & (b) respectively.

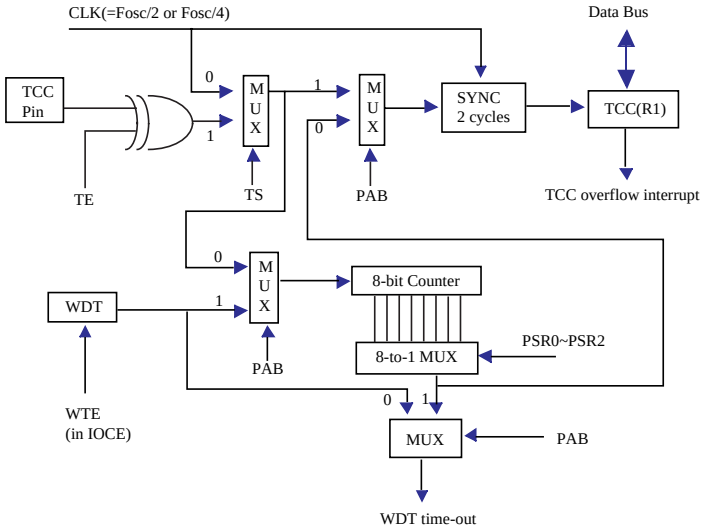


Fig. 6 Block diagram of TCC and WDT

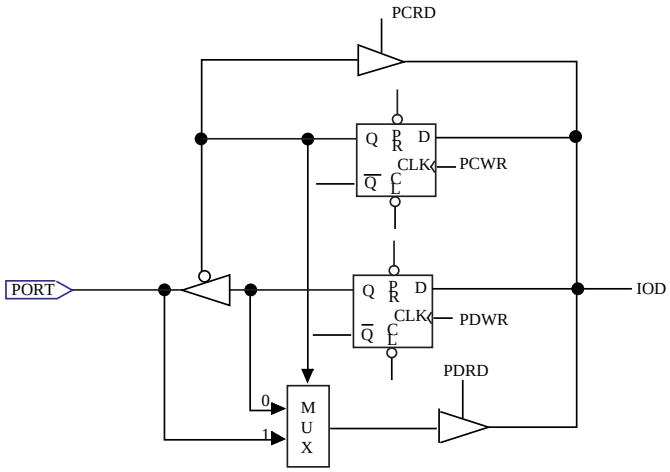
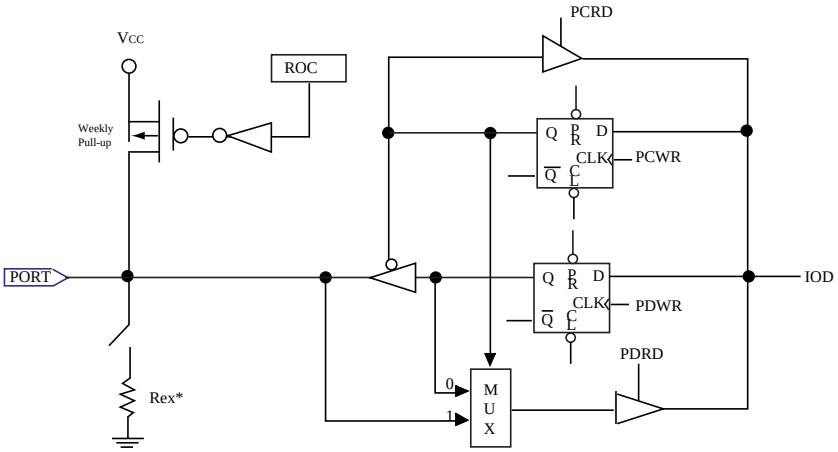


Fig. 7(a) The circuit of I/O port and I/O control register



* The Rex is 560K ohm external resistor

Fig. 7(b) The circuit of I/O port with R-option (P70,P71)

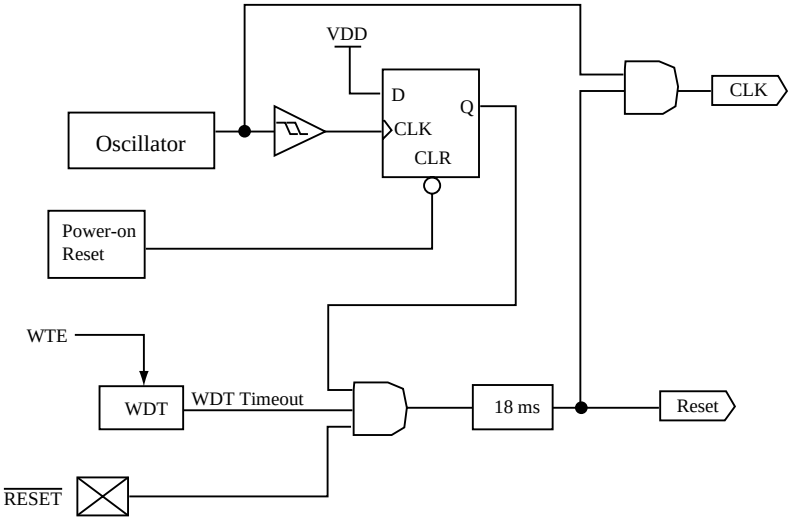


Fig. 8 Block diagram of Reset of controller

VI.5 RESET and Wake-up

1. RESET

The RESET can be caused by

(1) Power-on reset,
(2) /RESET pin input “low”, or
(3) WDT timeout. (if enabled)

Note that only power-on reset, or only voltage detector in Case (1) is enabled in the system by CODE option bit. Refer to Fig. 8. The device will be kept in a RESET condition for a period of approx. 18ms (one-oscillator start-up timer period) after the reset is detected. Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "1".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- Upon power-on, the bits 5~6 of R3 are cleared.
- Upon power-on, the upper 2 bits of R4 are cleared.
- The bits of the CONT register are set to all "1" except the bit 6 (INT flag).
- IOCB register is set to all "1" (disable P60~P67 wake-up function).
- Bits 3 and 6 of the IOCE register are cleared, and Bits 0,4 and 5 are set to "1".
- Bits 0 and 3 of R3F register and bits 0 and 3 of IOCF register are cleared.

Executing the "SLEP" instruction (named as SLEEP1 mode) can perform the sleep mode. While entering sleep mode, WDT (if enabled) is cleared but keeps running. The controller can be awakened by

(1) External reset input on /RESET pin;
(2) WDT time-out (if enabled).

The two cases will cause the controller EM78P447S to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up).

In addition to the basic SLEEP1 MODE, EM78P447S has another sleep mode (caused by clearing "SLPC" bit of IOCE register, named as SLEEP2 MODE). In the SLEEP2 MODE, the controller can be awakened by

(a). Any one of wake-up pins is "0". Please refer to Fig. 5. When waking, the controller will continue to execute the successive address. In this case, before entering SLEEP2 MODE, the wake-up function of the trigger sources (P60~P67, and P74~P75) should be selected (e.g. input pin) and enabled (e.g. pull-high, wake-up control). One caution should be noticed is that after waking up, the WDT is enabled if Code Option bit WTC is "1". The WDT operation (to be enabled or disabled) should be appropriately controlled by software after waking up.
(b). WDT time-out (if enabled) or external reset input on /RESET pin will cause the controller to reset.

Table 3 The summary of the initialized values for registers

Address	Name	Reset Type	Bit 7		Bit 6		Bit 5		Bit 4		Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57		C56		C55		C54		C53	C52	C51	C50
		TYPE	A	B	A	B	A	B	A	B	-	-	-	-
		Power-on	0	1	0	1	0	1	0	1	1	1	1	1
		/RESET and WDT	0	1	0	1	0	1	0	1	1	1	1	1
		Wake-up from Pin Changed	0	P	0	P	0	P	0	P	P	P	P	P
N/A	IOC6	Bit Name	C67		C66		C65		C64		C63	C62	C61	C60
		Power-on	1		1		1		1		1	1	1	1
		/RESET and WDT	1		1		1		1		1	1	1	1
		Wake-up from Pin Changed	P		P		P		P		P	P	P	P
N/A	IOC7	Bit Name	C77		C76		C75		C74		C73	C72	C71	C70
		Power-on	1		1		1		1		1	1	1	1

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	/PHEN	/INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	P	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0X00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0X01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0X02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	**0/P	**0/P	**0/P	**0/P	**0/P	**0/P	**0/P	**0/P
0X03	R3(SR)	Bit Name	GP	PS1	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Changed	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	RSR1	RSR0	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET and WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x05	R5(P5)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x06	R6(P6)	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x07	R7(P7)	Bit Name	P77	P76	P75	P74	P73	P72	P71	P70
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x3F	R3F(ISR)	Bit Name	X	X	X	X	EXIF	X	X	TCIF
		Power-on	U	U	U	U	0	U	U	0
		/RESET and WDT	U	U	U	U	0	U	U	0
		Wake-up from Pin Changed	U	U	U	U	P	U	U	P
0x0B	IOCB	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P
0x0E	IOCE	Bit Name	X	ODE	WTE	SLPC	ROC	X	X	/WUE
		Power-on	U	0	1	1	0	U	U	1
		/RESET and WDT	U	0	1	1	0	U	U	1
		Wake-up from Pin Changed	U	P	1	1	P	U	U	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	IOCF	Bit Name	X	X	X	X	EXIE	X	X	TCIE
		Power-on	U	U	U	U	0	U	U	0
		/RESET and WDT	U	U	U	U	0	U	U	0
		Wake-up from Pin Changed	U	U	U	U	P	U	U	P
0x08	R8~R3E	Bit Name	-	-	-	-	-	-	-	-
~		Power-on	U	U	U	U	U	U	U	U
0x3E		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Changed	P	P	P	P	P	P	P	P

** To execute next instruction after the "SLPC" bit status of IOCE register being on high-to-low transition.
X: not used. U: unknown or don't care. P: previous value before reset.
t: check Table 4.

2. The status of T and P of STATUS register

A RESET condition can be caused by the following events:

(1) A power-on condition,
(2) A high-low-high pulse on /RESET pin, and
(3) Watchdog Timer time-out.

The values of T and P, listed in Table 4 can be used to check how the processor wakes up. Table 5 shows the events which may affect the status of T and P.

Table 4 The values of T and P after RESET

Reset Type	T	P
Power-on	1	1
/RESET during operating mode	*P	*P
/RESET wake-up during SLEEP1 mode	1	0
/RESET wake-up during SLEEP2 mode	*P	*P
WDT during operating mode	0	*P
WDT wake-up during SLEEP1 mode	0	0
WDT wake-up during SLEEP2 mode	0	*P
Wake-up on pin changed during SLEEP2 mode	*P	*P

* P: Previous status before reset

Table 5 The status of T and P being affected by events

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during SLEEP2 mode	*P	*P

* P: Previous value before reset

VI.6 Interrupt

The EM78P447S has two interrupts listed below:

(1) TCC overflow interrupt.
(2) External interrupt (/INT) .

R3F, the interrupt status register, records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from address 001H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in R3F. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (R3F) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of R3F and IOCF. Refer to Fig. 9. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

When an interrupt is generated by the INT instruction (when enabled), the next instruction will be fetched from address 002H.

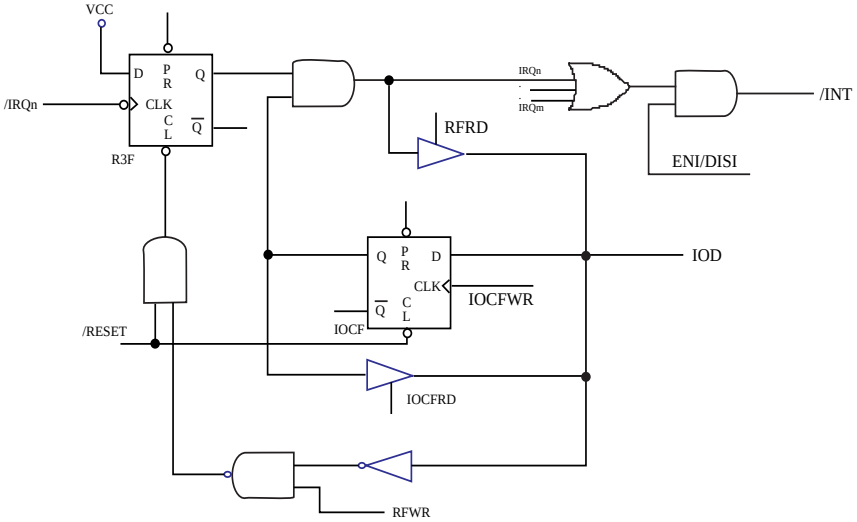


Fig. 9 Interrupt input circuit

VI.7 Oscillator

1 . Oscillator Modes

The EM78P447S can be operated in three different oscillator modes. There are External RC oscillator mode (ERC), High XTAL oscillator mode (HXT) and Low XTAL oscillator mode(LXT). Users can select one of them by programming MS, HLF, and HLP in the CODE Option Register. Table 6 depicts how these three modes to be defined.

The up-most limited operation frequency of crystal/resonator on the different VDDs is listed in Table 7.

Table 6 Oscillator Modes defined by MS, HLF, HLP

Mode	MS	HLF	HLP
External RC oscillator mode	0	*X	*X
High XTAL oscillator mode	1	1	*X
Low XTAL oscillator mode	1	0	0

<Note> 1. X, Do not care
2. The transient point of system frequency between HXT and LXY is around 400 KHz.

Table 7 The summary of maximum operating speeds

Conditions	VDD (V)	Fxt max. (MHz)
Two clocks	2.5	8
	3	12
	5	20
	6.4	21
Four clocks	2.5	16
	3	24
	5	40
	6.5	42

2. Crystal Oscillator/Ceramic Resonators(XTAL)

EM78P447S can be driven by an external clock signal through the OSCI pin as shown in Fig. 10.

In the most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 11 depicts the circuit. It is the same no matter in the HXT mode or in the LXT mode. Table 8 recommends the values of C1 and C2. Since each resonator has its own attribute, users should refer to their specifications for appropriate values of C1 and C2. RS, a serial resistor may be necessary for AT strip cut crystal or low frequency mode.

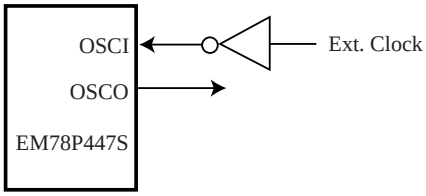


Fig. 10 Circuit for External Clock Input

Table 8 Capacitor Selection Guide for Crystal Oscillator Ceramic Resonators

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonator	HXT	455 KHz	100~150	100~150
		1.00 MHz	40~80	40~80
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Crystal Oscillator	LXT	32.768 KHz	25	15
		100 KHz	25	25
		200 KHz	25	25
	HXT	455 KHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

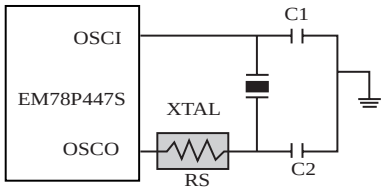


Fig. 11 Circuit for Crystal/Resonator

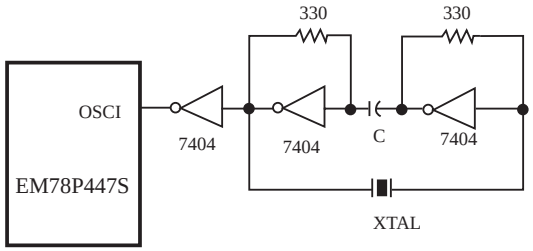


Fig. 12 Circuit for Crystal/Resonator (Series Mode)

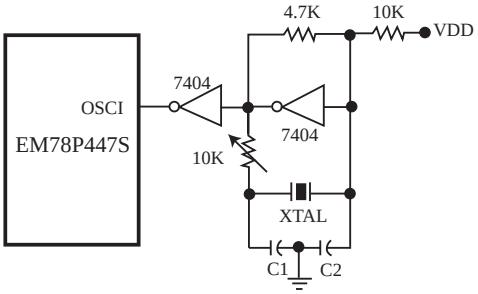


Fig. 13 Circuit for Crystal/Resonator (Parallel Mode)

3. RC Oscillator Mode

For some applications whose timing need not be calculated precisely, the RC oscillator (Fig. 14) offers a lot of cost savings. Nevertheless, it should be aware that the frequency of the RC oscillator is the function of the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even the operation temperature. Moreover to this, the

frequency also changes slightly from one chip to another due to the process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, as well as the value of Rext should not be greater than 1M ohm. If they can not be kept in this range, the frequency is affected easily by noise, humidity and leakage.

The smaller Rext the RC oscillator has, the faster frequency it gets. On the contrary, for very low Rext values, for instance, 1KΩ, the oscillator becomes unstable because the NMOS can not discharge the current of the capacitance correctly.

On a basis of the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types and the ways of PCB layout will effect the system frequency.

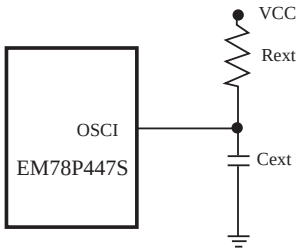


Fig. 14 Circuit for External RC Oscillator Mode

Table 9 RC Oscillator Frequencies

Cext	Rext	Average Fosc @ 5V, 25°C	Average Fosc @ 3V, 25°C
20pF	3.3k	4.32 MHz	3.56 MHz
	5.1k	2.83 MHz	2.8 MHz
	10k	1.62 MHz	1.57 MHz
	100k	184 KHz	187 KHz
100pF	3.3k	1.39 MHz	1.35 KHz
	5.1k	950 KHz	930 KHz
	10k	500 KHz	490 KHz
	100k	54 KHz	55 KHz
300pF	3.3k	580 KHz	550 KHz
	5.1k	390 KHz	380 KHz
	10k	200 KHz	200 KHz
	100k	21 KHz	21 KHz

* 1. Measured on DIP packages.
2. Design reference only

VI.8 CODE Option Register

The EM78P447S has one CODE option word which is not a part of the normal program memory. The option bits can not be accessed during normal program execution.

12	11	10	9	8	7	6	5~0
MS	ENWDTB	CLKS	/PT	HLF	HLP	TYP	------

- **Bit 12 (MS)**: Oscillator type selection.
  0: RC type
  1: XTAL type
- **Bit 11 (/ENWTDB**): Watchdog Timer enable bit.
  0: Enable
  1: Disable
- **Bit 10 (CLKS)**: Instruction period option bit.
  0: two oscillator periods
  1: four oscillator periods
  Refer to the section of Instruction Set.
- **Bit 9(/PT)**: Protect Bit.
  0: Protect Enable
  1: Protect Disable
- **Bit 8(HLF)**: XTAL frequency selection.
  0: XTAL2 type (Low frequency, 32.768KHz)
  1: XTAL1 type (High frequency)
  This bit is useful only when Bit 0 (MS) is “1”. When MS is “0”, HLF must be “0”.
- **Bit 7(HLP)**: Power consumption selection.
  0: Low power
  1: High power
- **Bit 6(Type)**: Type selection for EM78P447SA or B.
  0: EM78P447SB
  1: EM78P447SA
- **Bit 5 and Bit 4** : Reserved.
  The bit5 set to"1" all the time
  The bit4 set to "0" all the time
- **Bit 3~0**: User’s ID code.

VI.9 Power-on Considerations

Any microcontroller is not warranted to start proper operation before the power supply stays in its steady state. EM78P447S is equipped with Power On Voltage Detector (POVD) which detective level is 2.0V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (10 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

VI.10 External Power-on Reset Circuit

The circuit shown in Fig. 15 implements an external RC to produce the reset pulse. The pulse width (time constant) should keep long enough until Vdd has reached minimum operation voltage. This circuit is used when the power

supply has slow rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40K. In this way, the voltage in pin /RESET will be held below 0.2V. The diode (D) acts a short circuit at the moment of power-down. The capacitor, C, will be discharged rapidly and fully. Rl, the current-limited resistor, protects against a high discharging current or ESD (electrostatic discharge) flowing to pin /RESET.

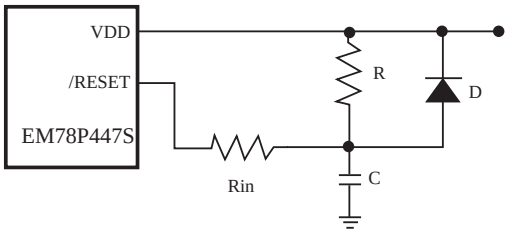


Fig. 15 External Power-up Reset Circuit

VI.11 Residue Voltage Protection

In some applications, replacing battery as an instance, device power (Vdd) is taken off and recovered within a few seconds. A residue voltage which trips below Vdd min but not to zero may exist. This condition may cause a poor power-on reset. Fig. 16 and Fig. 17 show how to build the residue voltage protection circuit

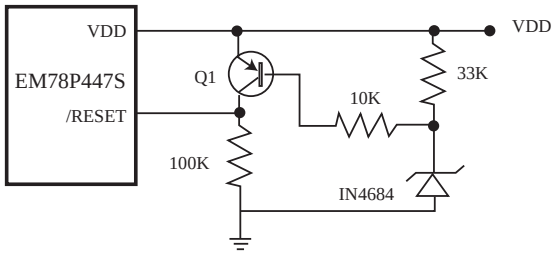


Fig. 16 Circuit 1 for the residue voltage protection

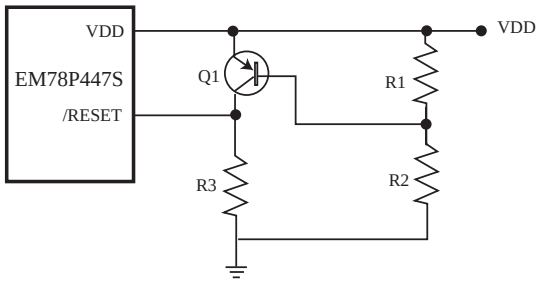


Fig. 17 Circuit 2 for the residue voltage protection

VI.12 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator periods), unless the program counter is changed by instruction “MOV R2,A”, “ADD R2,A”, or instructions of arithmetic or logic operation on R2 (e.g. “SUB R2,A”, “BS(C) R2,6”, “CLR R2”, ...). In this case, the execution takes two instruction cycles.

Under some conditions, if the specification of the instruction cycle is not suitable for some applications, they can be modified as follows:

(A) One instruction cycle consists of 4 oscillator periods.

(B) “JMP”, “CALL”, “RET”, “RETL”, “RETI”, and the conditional skip (“JBS”, “JBC”, “JZ”, “JZA”, “DJZ”, “DJZA”) tested to be true are executed within two instruction cycles. The instructions that write to the program counter also take two instruction cycles.

The Case (A) is selected by the CODE option bit, called CLKS. One instruction cycle consists of two oscillator clocks if CLKS is low, and consists of four oscillator clocks if CLKS is high.

Note that once 4 oscillator periods within one instruction cycle is selected in Case (A), the internal clock source to TCC is CLK=Fosc/4 instead of Fosc/ 2 that is shown in Fig. 6.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O registers can be operated as general registers. That is, the same instruction can operate on I/O register.

The symbol “R” represents a register designator which specifies which one of the registers (including operational registers and general purpose registers) to be utilized by the instruction. The symbol “b” represents a bit field designator which selects the number of the bit located in the register “R” affected by the operation. The symbol “k” represents an 8 or 10-bit constant or literal value.

Table 10 The list of the instruction set of EM78P447S

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A→CONT	None
0 0000 0000 0011	0003	SLEP	0→WDT, Stop oscillator	T,P
0 0000 0000 0100	0004	WDTC	0→WDT	T,P
0 0000 0000 rrrr	000r	IOW R	A→IOCR	None <Note1>
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] PC Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT→A	None
0 0000 0001 rrrr	001r	IOR R	IOCR→A	None <Note1>
0 0000 0010 0000	0020	TBL	R2+A→R2 Bits 8~9 of R2 unchanged	Z,C,DC
0 0000 01rr rrrr	00rr	MOV R,A	A→R	None
0 0000 1000 0000	0080	CLRA	0→A	Z
0 0000 11rr rrrr	00rr	CLR R	0→R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A→A	Z,C,DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A→R	Z,C,DC
0 0001 10rr rrrr	01rr	DECA R	R-1→A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1→R	Z
0 0010 00rr rrrr	02rr	OR A,R	A∨VR→A	Z
0 0010 01rr rrrr	02rr	OR R,A	A∨VR→R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R→A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R→R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R→A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R→R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R→A	Z,C,DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R→R	Z,C,DC
0 0100 00rr rrrr	04rr	MOV A,R	R→A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R→R	Z
0 0100 10rr rrrr	04rr	COMA R	/R→A	Z
0 0100 11rr rrrr	04rr	COM R	/R→R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1→A	Z
0 0101 01rr rrrr	05rr	INC R	R+1→R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1→A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1→R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n)→A(n-1) R(0)→C, C→A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n)→R(n-1) R(0)→C, C→R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n)→A(n+1) R(7)→C, C→A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n)→R(n+1) R(7)→C, C→R(0)	C

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None <Note2>
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None <Note3>
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1→[SP], (Page, k) →PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → ANone	
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 0000 0001	1E01	INT	PC+1 → [SP], 001H → PC	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC

<Note 1> This instruction can operate on IOC5~IOC7, IOCB, IOCE, IOCF only.

<Note 2> This instruction is not recommended to operate on RF.

<Note 3> This instruction cannot operate on RF.

VII. ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Rating
Temperature under bias	T_{OPR}		0°C to 70°C
Storage temperature	T_{STR}		-65°C to 150°C
Input voltage	V_{IN}		-0.3V to +6.0V
Output voltage	V_O		-0.3V to +6.0V

VIII. DC ELECTRICAL CHARACTERISTIC (Ta=0°C ~ 70°C, V_{DD}=5.0V, V_{SS}=0V)

Parameter	Sym.	Condition	Min.	Typ.	Max.	Unit
XTAL: VDD to 3V	Fxt	Two clocks	DC		4.0	MHz
XTAL: VDD to 5V			DC		20.0	MHz
RC : VDD to 5V	F_{RC}	R : 5.1KΩ , C : 100pF	F±20%	950	F±20%	KHz
Input Leakage Current for input pins	I_{IL}	V_{IN} = V_{DD}, V_{SS}			±1	µA
Input High Voltage	V_{IH}	Ports 5, 6	2.0			V
Input Low Voltage	V_{IL}	Ports 5, 6			0.8	V
Input High Threshold Voltage	V_{IHT}	/RESET, TCC,INT	2.0			V
Input Low Threshold Voltage	V_{ILT}	/RESET, TCC,INT			0.8	V
Clock Input High Voltage	V_{IHX}	OSCI	3.5			V
Clock Input Low Voltage	V_{ILX}	OSCI			1.5	V
Output High Voltage (Port 5,6,7)	V_{OH1}	I_{OH} = -10.0mA	2.4			V
Output Low Voltage (Port 5,6)	V_{OL1}	I_{OL} = 9.0mA			0.4	V
Output Low Voltage (Port7)	V_{OL2}	I_{OL} = 14.0mA			0.4	V
Pull-high current	I_{PH}	Pull-high active, input pin at V_{SS}	-50	-100	-240	µA
Power-down current	I_{SB1}	All input and I/O pins at V_{DD}, output pin floating, WDT enabled			7	µA
Power-down current	I_{SB2}	All input and I/O pins at V_{DD}, output pin floating, WDT disabled			1	µA
Operating supply current (VDD=5V) at two cycles/two clocks	I_{CC1}	/RESET='High', Fosc=4MHz (HLF="1", CK2="0"), output pin floating, WDT disabled			2.2	mA
Operating supply current (VDD=5V) at two cycles/two clocks	I_{CC2}	/RESET='High', Fosc=10MHz (HLF="1",CK2="0"),output pin floating, WDT disabled			5	mA
Operating supply current (V_{DD}=3V) at two cycles/two clocks	I_{CC3}	/RESET='High', Fosc=32.768KHz (HLF="0",CK2="0"), output pin floating, WDT disabled	15	25	30	µA
Operating supply current (V_{DD}=3V) at two cycles/two clocks	I_{CC4}	/RESET='High', Fosc=32.768KHz (HLF="0",CK2="0"), output pin floating, WDT enabled	-	30	35	µA

IX. VOLTAGE DETECTOR ELECTRICAL CHARACTERISTIC (Ta = 25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	Vdet		1.9	2.0	2.1	V
Release voltage	Vrel			Vdet x1.05		V
Current consumption	Iss	V_{DD} = 5V			5	μA
Operating voltage	Vop		0.7*		5.5	V
Temperature characteristic of Vdet	ΔVdet/ ΔTa	0°C ≤Ta≤ 70°C			-2	mV/°C
VDD reset voltage	Vreset	Ta=25°C			1.9	V

* When the voltage of V_{DD} rises between Vop=0.7V and Vdet, the output of voltage detector must be "Low".

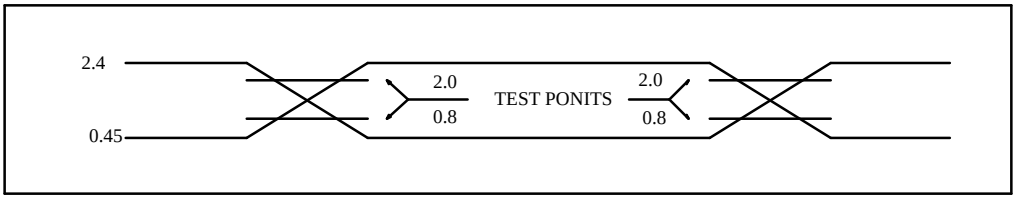
X. AC ELECTRICAL CHARACTERISTICS (Ta=0°C ~ 70°C, V_{DD}=5.0V±5%, V_{SS}=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	XTAL Type	100		DC	ns
(CLKS="0")		RC Type	500		DC	ns
TCC input period	Ttcc		(Tins+20)/N*			ns
Device reset hold time	Tdrh	Ta = 25°C		16.2		ms
Watchdog Timer period	Twdt	Ta = 25°C		16.2		ms
Input pin setup time	Tset			0		ns
Input pin hold time	Thold			20		ns
Output pin delay time	Tdelay	Cload=20pF		50		ns

Note : N* = selected prescaler ratio.

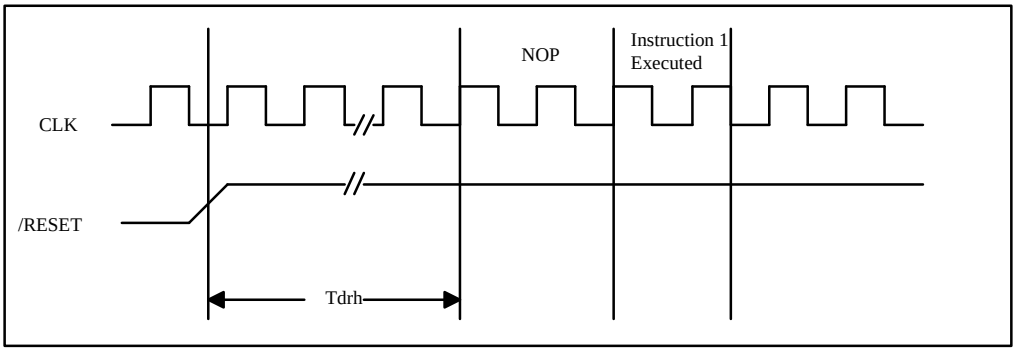
XI. TIMING DIAGRAMS

AC Test Input/Output Waveform



AC Testing : Input is driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLK="0")