OKI Semiconductor

MSM514265B/BSL

262,144-Word × 16-Bit DYNAMIC RAM : HYPER PAGE MODE TYPE

DESCRIPTION

The MSM514265B/BSL is a new generation Dynamic RAM organized as 262,144-word × 16-bit configuration.
The technology used to fabricate the MSM514265B/BSL is OKI's CMOS silicon gate process technology.
The device operates at a single 5V power supply. Its I/O pins are TTL compatible.

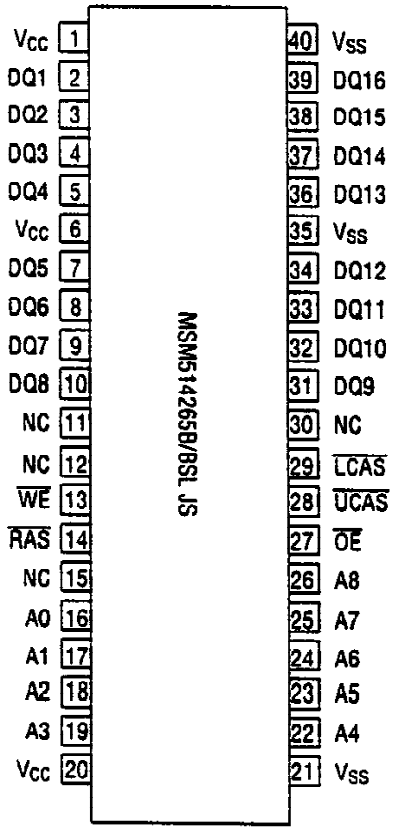
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 262,144-word × 16-bit organization
- Single 5V power supply, ±10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate
- Refresh: 512 cycles/8ms, 512 cycles/128ms (SL version)
- Hyper page mode, read modify write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- $\overline{CAS}$ before $\overline{RAS}$ self-refresh capability (SL version)
- Package :
  40-Pin 400mil Plastic SOJ (SOJ40-P-400)

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM514265B/BSL-50	50ns	22ns	12ns	12ns	84ns	1210mW	5.5mW/ 1.1mW (SL version)
MSM514265B/BSL-60	60ns	30ns	15ns	15ns	104ns	1100mW	
MSM514265B/BSL-70	70ns	35ns	20ns	20ns	124ns	990mW	

PIN CONFIGURATION (TOP VIEW)

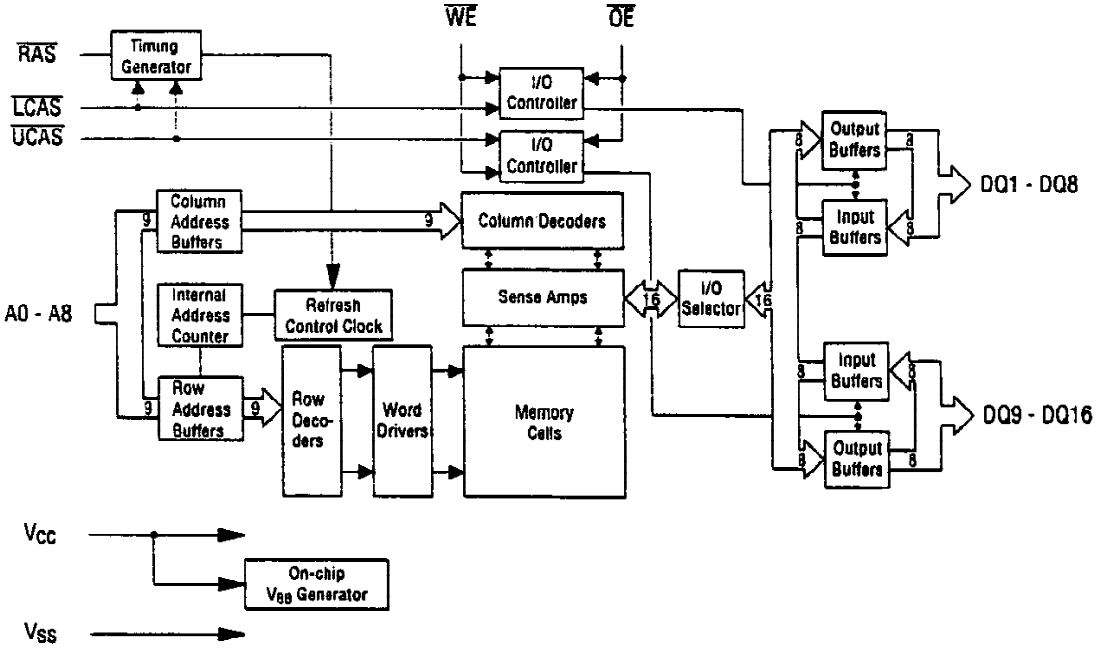


40-PIN SOJ

Pin Name	Function
A0 - A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$	Lower Byte Column Address Strobe
$\overline{UCAS}$	Upper Byte Column Address Strobe
DQ1 - DQ16	Data - Input / Data - Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (5V)
V_{SS}	Ground (0V)
NC	No Connection

Note: Same power supply voltage must be provided to every V_{CC} pin, and same GND voltage level must be provided to every V_{SS} pin.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL TABLE

Input Pin					DQ Pin		Functional Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ1 - DQ8	DQ9 - DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−1.0	—	0.8	V

Capacitance

(V_{CC} = 5V ± 10%, Ta = 25°C, f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	C_{IN1}	—	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	10	pF

DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM514265B/BSL-50		MSM514265B/BSL-60		MSM514265B/BSL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = −2.0mA	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0mA	0	0.8	0	0.8	0	0.8	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ 6.5V; All other pins not under test = 0V	−10	10	−10	10	−10	10	µA	
Output Leakage Current	I_{LO}	DQi Disable 0V ≤ V_O ≤ 5.5V	−10	10	−10	10	−10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = Min.	—	220	—	200	—	180	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V	—	1	—	1	—	1		
			—	200	—	200	—	200	µA	1, 5
Average Power Supply Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ = cycling $\overline{CAS}$ = V_{IH} t_{RC} = Min.	—	220	—	200	—	180	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = Enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	I_{CC6}	$\overline{RAS}$ = cycling $\overline{CAS}$ before $\overline{RAS}$	—	220	—	200	—	180	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = Min.	—	220	—	200	—	180	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	t_{RC} = 125µs $\overline{CAS}$ before $\overline{RAS}$ t_{RAS} ≤ 1µs	—	300	—	300	—	300	µA	1, 2, 4, 5
Average Power Supply Current ($\overline{CAS}$ Before $\overline{RAS}$ Self-refresh)	I_{CC8}	$\overline{RAS}$ ≤ 0.2V $\overline{CAS}$ ≤ 0.2V	—	200	—	200	—	200	µA	1, 5

Notes:
1. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} − 0.2V ≤ V_{IH} ≤ 6.5V, −1.0V ≤ V_{IL} ≤ 0.2V.
5. SL version.

AC Characteristics (1/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM514265B/BSL-50		MSM514265B/BSL-60		MSM514265B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	84	—	104	—	124	—	ns	
Read Modify Write Cycle Time	t_{RMW}	109	—	134	—	159	—	ns	
Hyper Page Mode Cycle Time	t_{HPC}	20	—	25	—	25	—	ns	
Hyper Page Mode Read Modify Write Cycle Time	t_{PRMW}	54	—	67	—	77	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{CAS}$	t_{CAC}	—	12	—	15	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	22	—	30	—	35	ns	4, 6
Access Time from $\overline{OE}$	t_{OEA}	—	12	—	15	—	20	ns	4
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	27	—	35	—	40	ns	4, 13
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	ns	4
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	12	0	15	0	20	ns	7
Transition Time	t_T	1	50	1	50	1	50	ns	3
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
Refresh Period (SL version)	t_{REF}	—	128	—	128	—	128	ms	16
$\overline{RAS}$ Precharge Time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{RAS}$ Pulse Width (Hyper Page Mode)	t_{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	7	—	10	—	15	—	ns	
$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	t_{ROH}	7	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	7	—	10	—	10	—	ns	15
$\overline{CAS}$ Pulse Width	t_{CAS}	7	10,000	10	10,000	10	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	35	—	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	10	—	ns	13
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	11	38	14	45	14	50	ns	5
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	9	28	12	30	12	35	ns	6
$\overline{RAS}$ to Second $\overline{CAS}$ Delay Time	t_{RSCD}	50	—	60	—	70	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	12
Column Address Hold Time	t_{CAH}	5	—	7	—	10	—	ns	12
Column Address Hold Time from $\overline{RAS}$	t_{AR}	38	—	45	—	50	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	22	—	30	—	35	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	12
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	9, 12
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	9

AC Characteristics (2/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note 1, 2, 3

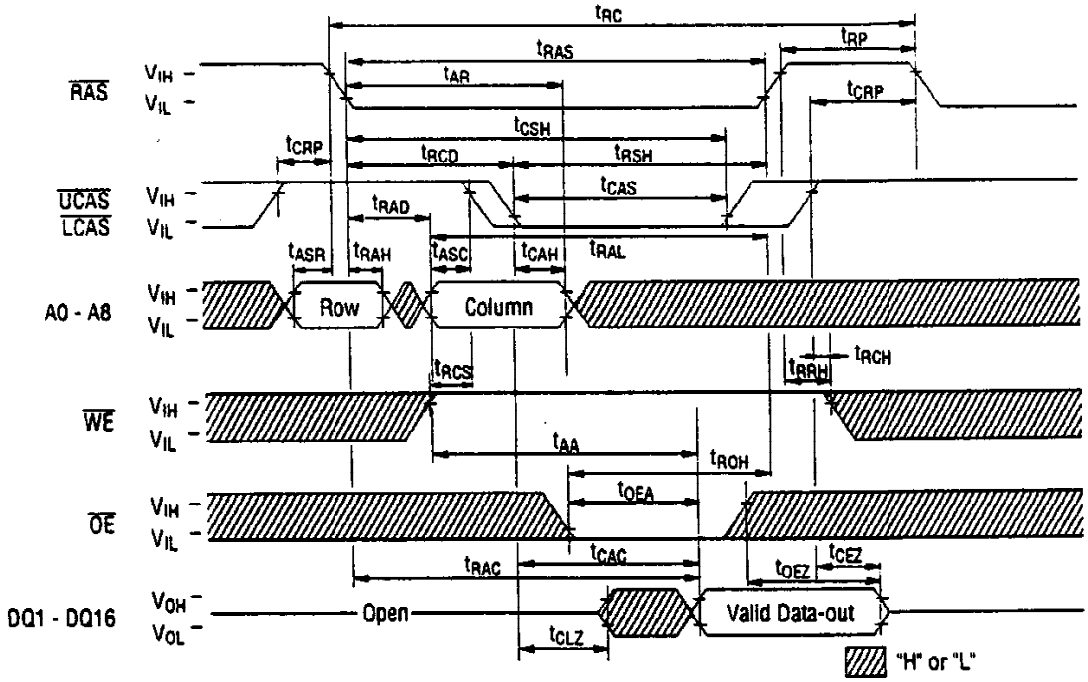
Parameter	Symbol	MSM514265B/BSL-50		MSM514265B/BSL-60		MSM514265B/BSL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10, 12
Write Command Hold Time	t_{WCH}	5	—	7	—	7	—	ns	12
Write Command Pulse Width	t_{WP}	5	—	7	—	7	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	38	—	45	—	50	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	12	—	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	7	—	9	—	9	—	ns	14
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	7	—	9	—	9	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11, 12
Data-in Hold Time	t_{DH}	5	—	7	—	7	—	ns	11, 12
Data-in Hold Time from $\overline{RAS}$	t_{DHR}	38	—	45	—	50	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	12	—	15	—	20	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	28	—	34	—	44	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	38	—	49	—	59	—	ns	10
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	66	—	79	—	94	—	ns	10
$\overline{CAS}$ Precharge $\overline{WE}$ Delay Time	t_{CPWD}	43	—	54	—	64	—	ns	10
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	5	—	5	—	5	—	ns	12
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CSR}	5	—	5	—	5	—	ns	12
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$)	t_{CHR}	7	—	10	—	10	—	ns	13
$\overline{CAS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	20	—	20	—	20	—	ns	13
$\overline{CAS}$ Precharge Time	t_{CPN}	10	—	10	—	10	—	ns	15
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ Before $\overline{RAS}$ Self-refresh)	t_{RASS}	100	—	100	—	100	—	µs	16
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Self-refresh)	t_{RPS}	84	—	104	—	124	—	ns	16
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Self-refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	16
Data Output Hold After $\overline{CAS}$ Low	t_{DOH}	5	—	5	—	5	—	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	12	0	15	0	20	ns	7, 8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	12	0	15	0	20	ns	7, 8
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	12	0	15	0	20	ns	7
$\overline{OE}$ Hold Time from $\overline{CAS}$ (D_{OUT} Disable)	t_{CHO}	5	—	5	—	10	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	7	—	10	—	10	—	ns	
$\overline{OE}$ Command Hold Time	t_{OCH}	7	—	10	—	10	—	ns	
$\overline{WE}$ Pulse Width (D_{OUT} Disable)	t_{WPE}	5	—	7	—	7	—	ns	

Notes:

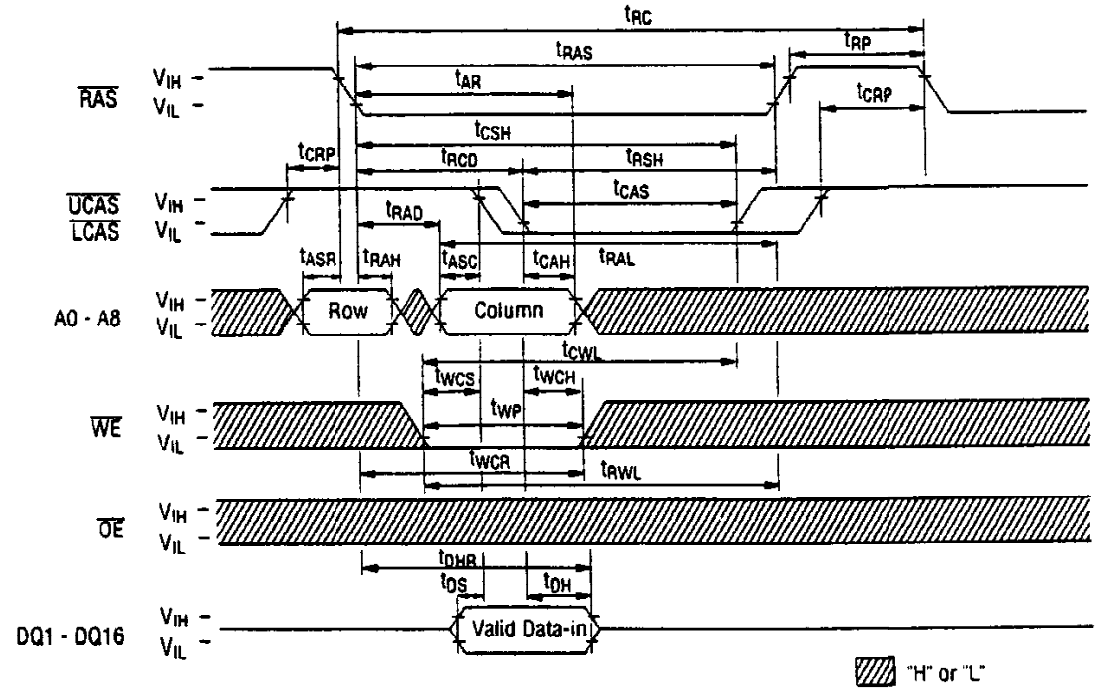
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only refresh) before proper device operation is achieved.
2. The AC characteristics assume t_T = 2ns.
3. V_{IH}(Min.) and V_{IL}(Max.) are reference levels of input signals for timing measurement. Transition times(t_T) are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 1 TTL loads and 50pF.
5. Operation within the t_{RCD}(Max.) limit insures that t_{RAC}(Max.) can be met. t_{RCD}(Max.) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD}(Max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD}(Max.) limit insures that t_{RAC}(Max.) can be met. t_{RAD}(Max.) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD}(Max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{CEZ}(Max.), t_{REZ}(Max.), t_{WEZ}(Max.) and t_{OEZ}(Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
8. Both t_{CEZ} and t_{REZ} must be satisfied for the open circuit condition.
9. Either t_{RRH} and t_{RCH} must be satisfied for a read cycle.
10. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$(Min.), the cycle is an early write cycle and data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$(Min.), $t_{RWD} \geq t_{RWD}$(Min.), $t_{AWD} \geq t_{AWD}$(Min.) and $t_{CPWD} \geq t_{CPWD}$(Min.), the cycle is a read modify write cycle and data out will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{UCAS}$, $\overline{LCAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a $\overline{OE}$ control write cycle or a read modify write cycle.
12. t_{ASC}, t_{CAH}, t_{RCS}, t_{RCH}, t_{WCS}, t_{DS}, t_{DH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
13. t_{CRP}, t_{CHR} and t_{CPA} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
14. t_{CWL} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
15. t_{CPN}, t_{CP} and t_{CPT} are determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
16. SL version.

TIMING WAVEFORM

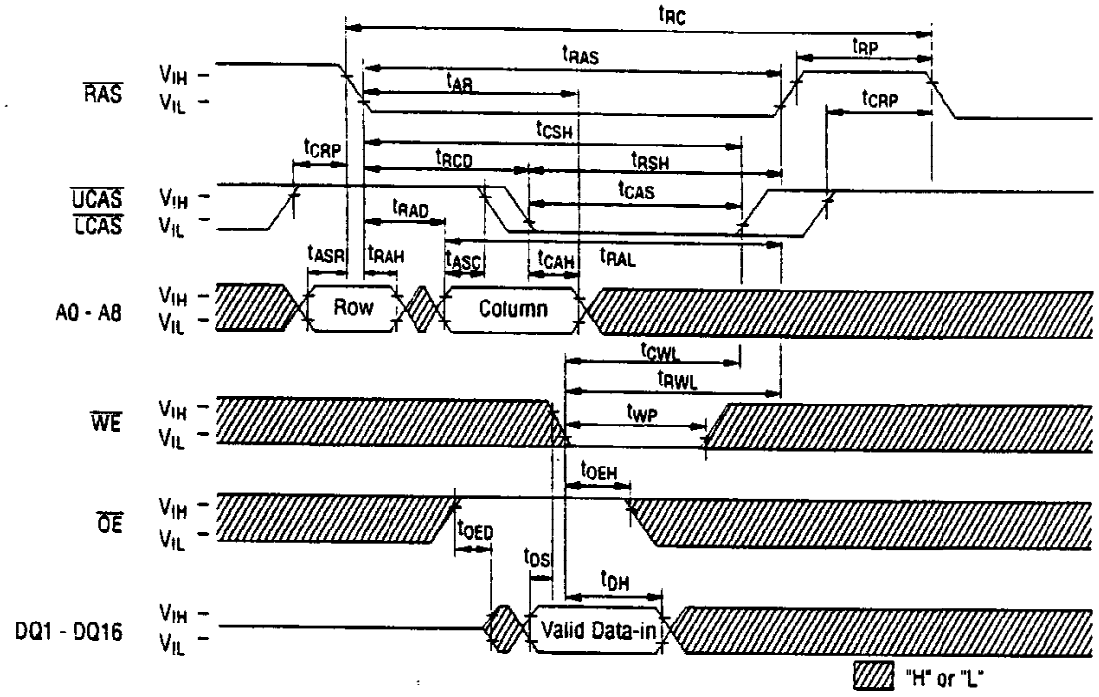
Read Cycle



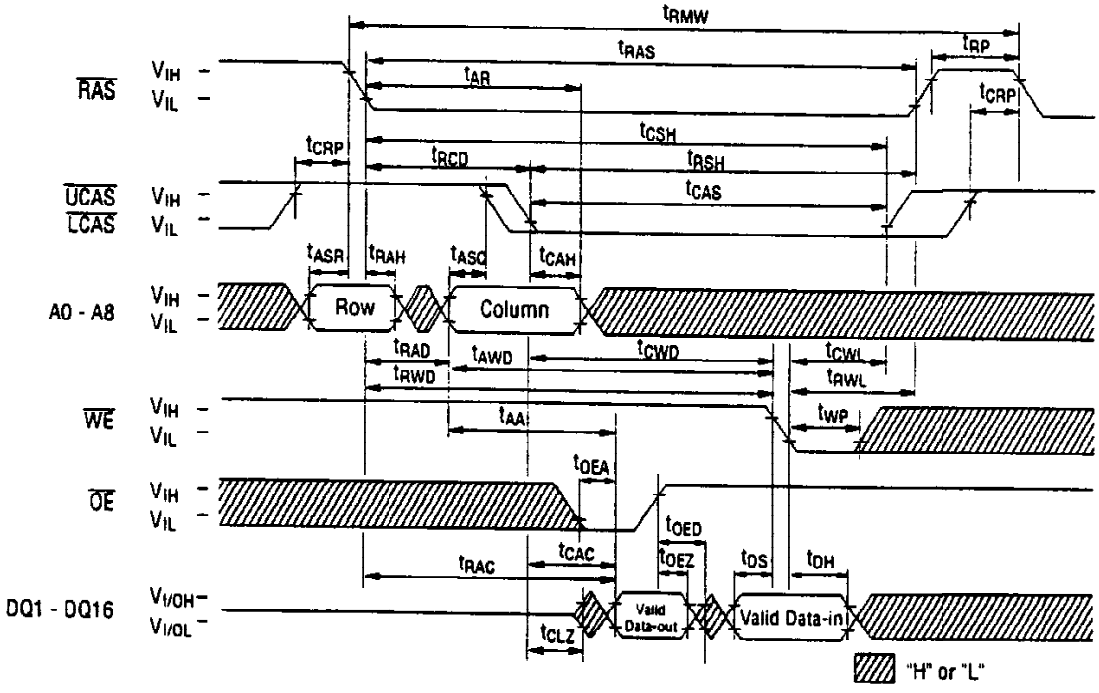
Write Cycle (Early Write)



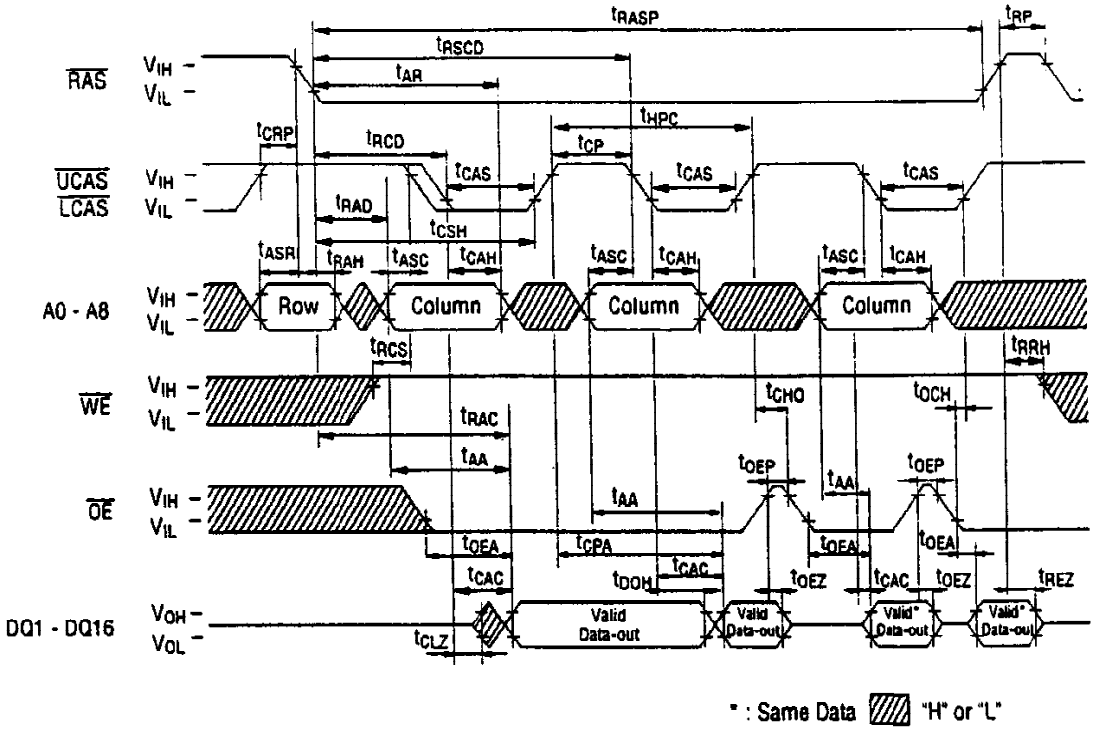
Write Cycle ($\overline{OE}$ Control Write)



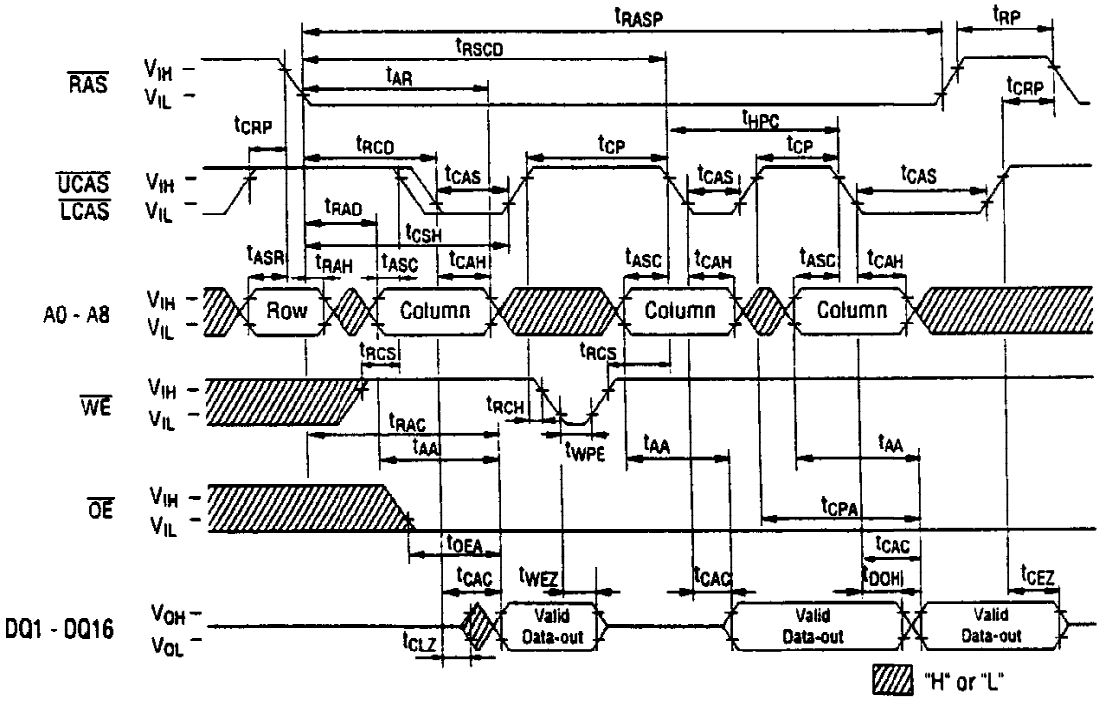
Read Modify Write Cycle



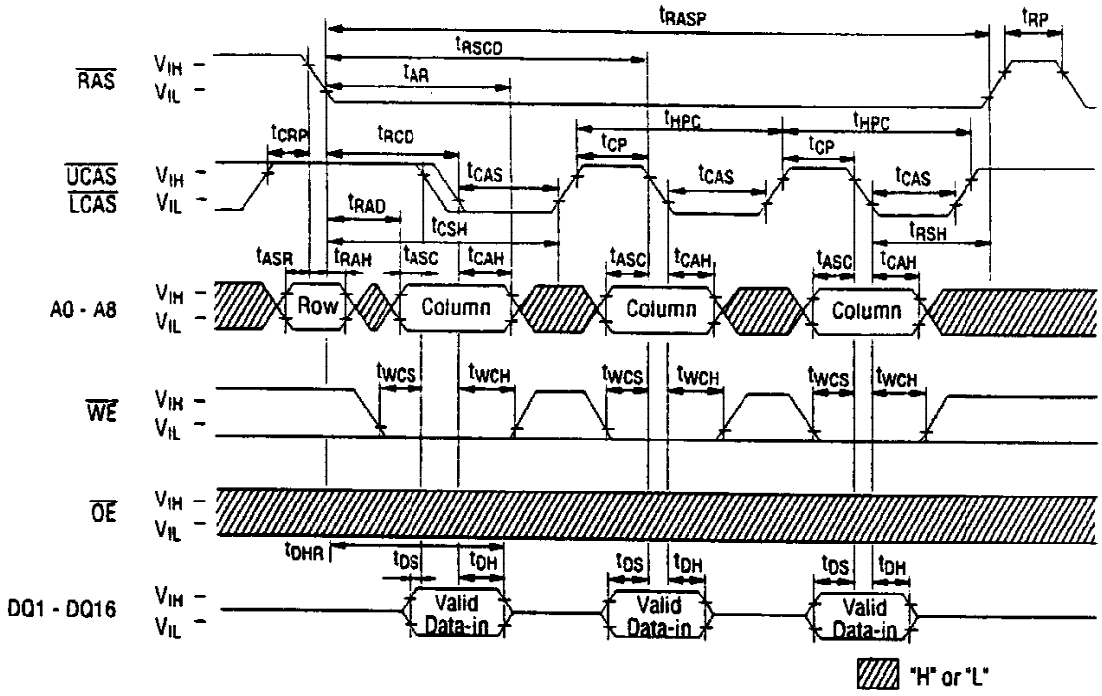
Hyper Page Mode Read Cycle (Part-1)



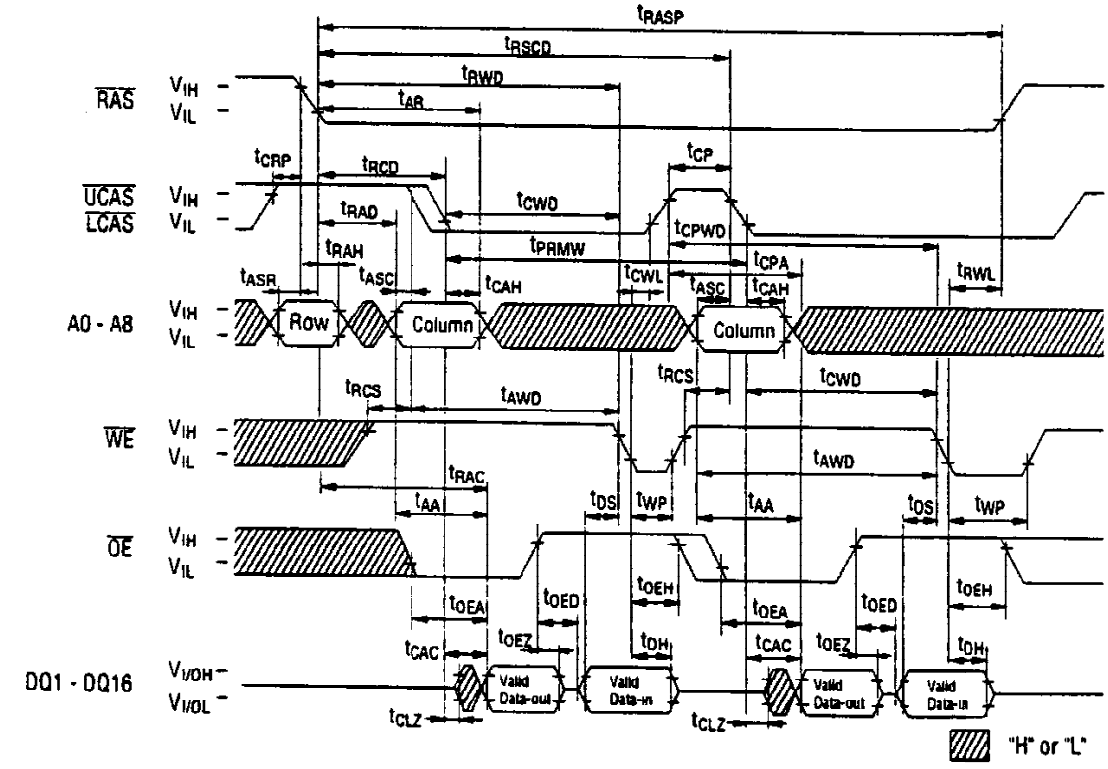
Hyper Page Mode Read Cycle (Part-2)



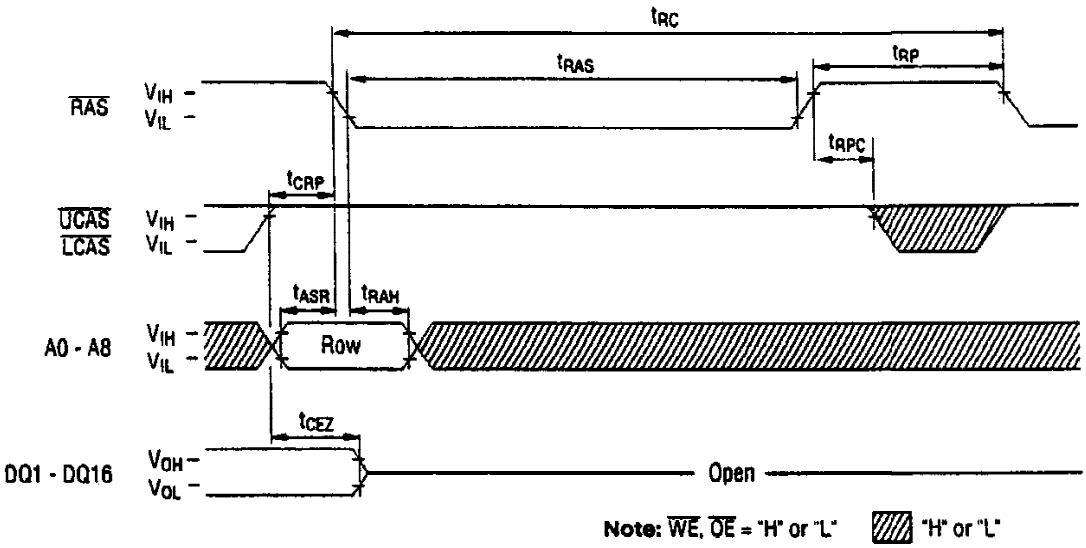
Hyper Page Mode Write Cycle (Early Write)



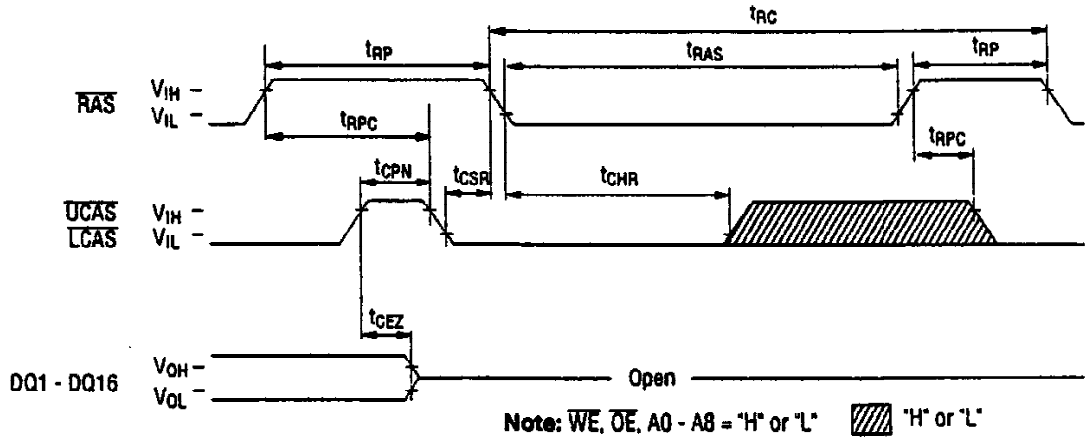
Hyper Page Mode Read Modify Write Cycle



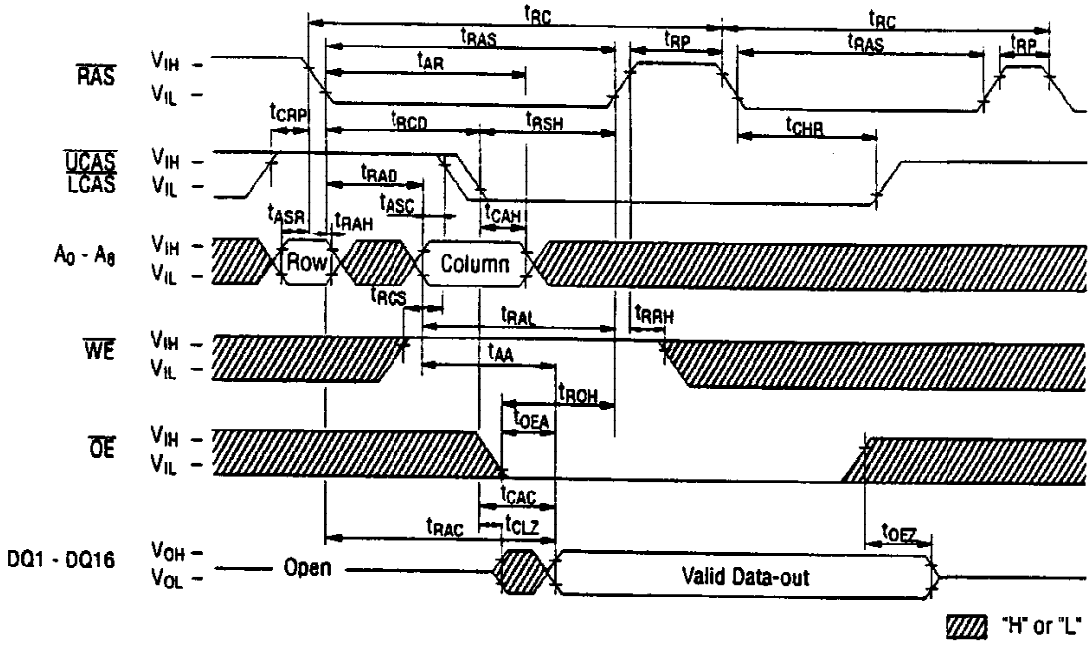
$\overline{RAS}$-only Refresh Cycle



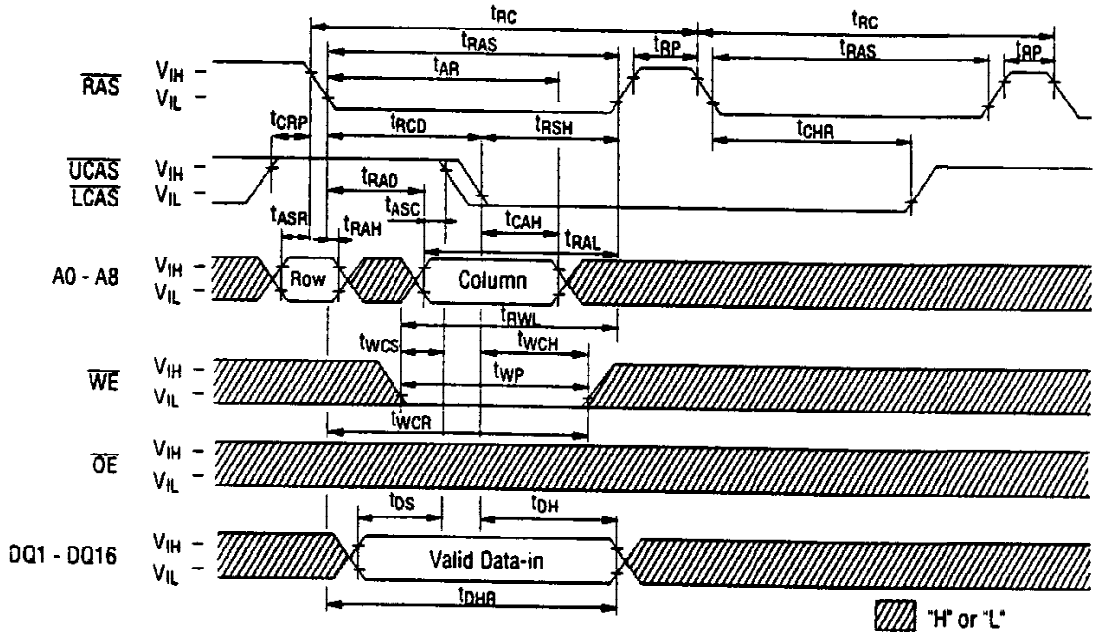
$\overline{CAS}$ Before $\overline{RAS}$ Auto Refresh Cycle



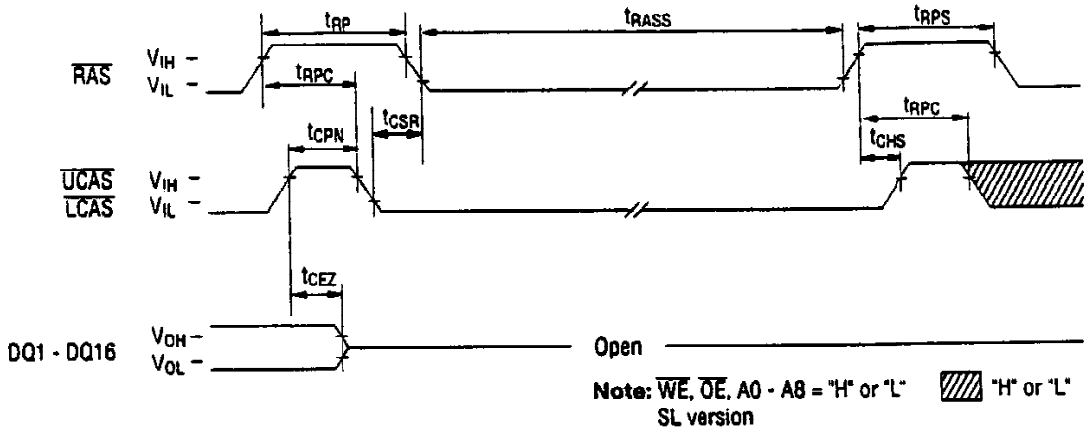
Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Self-refresh Cycle



CAS Before RAS Refresh Counter Test Cycle