

# DATA SHEET

## **SAA7282** Terrestrial Digital Sound Decoder (TDSD2)

Product specification  
File under Integrated Circuits, IC02

July 1993

# Terrestrial Digital Sound Decoder (TDSD2)

# SAA7282

## FEATURES

- Full EBU NICAM 728 specification decoder
- Microcomputer controlled via I<sup>2</sup>C-bus
- Automatic decoding and output configuration depending upon transmission:
  - digital stereo
  - digital mono and data
  - 2 independent mono signals
- On board RAM for de-interleaving and 10 to 14-bit word expansion
- Automatic mute function which silences the digital data and switches to FM sound (if valid) when error rate exceeds user definable limit
- User mute function ( $\overline{\text{MUTE}}$  pin) to enable user to perform muting to their own software algorithm if required, or to simply silence the output
- 4 times over-sampling digital filter
- Selectable digital de-emphasis
- 256 times over-sampling Noise Shapers
- Fully integrated 1-bit DACs
- Integrated switching networks allowing selection between NICAM Sound, FM Sound or external "Daisy-Chain" input
- Digital Audio Interface conforming with EBU/IEC 958
- I<sup>2</sup>C-bus transceiver enabling a master device to read
  - status information
  - error count byte
  - additional data bits and write:
    - switch control codes
    - decoder control
    - upper and lower error rate limits.



## APPLICATIONS

- Television receivers
- Video cassette recorders.

## GENERAL DESCRIPTION

Performing all digital decoding functions for a NICAM 728 digital stereo sound system, the SAA7282 is a highly integrated CMOS circuit which only requires a DQPSK (Differential Quadrature Phase Shift Keying) demodulator (TDA8732) and minimum external components to achieve a full NICAM solution.

The device may also be interfaced to other DQPSK demodulators.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>DD</sub>	positive supply voltage	4.5	5.0	5.5	V
I <sub>DD</sub>	supply current	–	50	100	mA
f <sub>XTAL</sub>	crystal frequency	–	8.192	–	MHz
T <sub>amb</sub>	operating ambient temperature	0	–	70	°C

## ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7282ZP	32	DIL32SHR	plastic	SOT232A <sup>(1)</sup>
SAA7282GP	44	QFP	plastic	SOT205AG <sup>(2)</sup>

## Note

1. SAA7282ZP: 32-DIL32SHR; plastic (SOT232A); SOT232-1; 1996 November 28.
2. SAA7282GP: 44-QFP; plastic (SOT205AG); SOT205-1; 1996 November 28.

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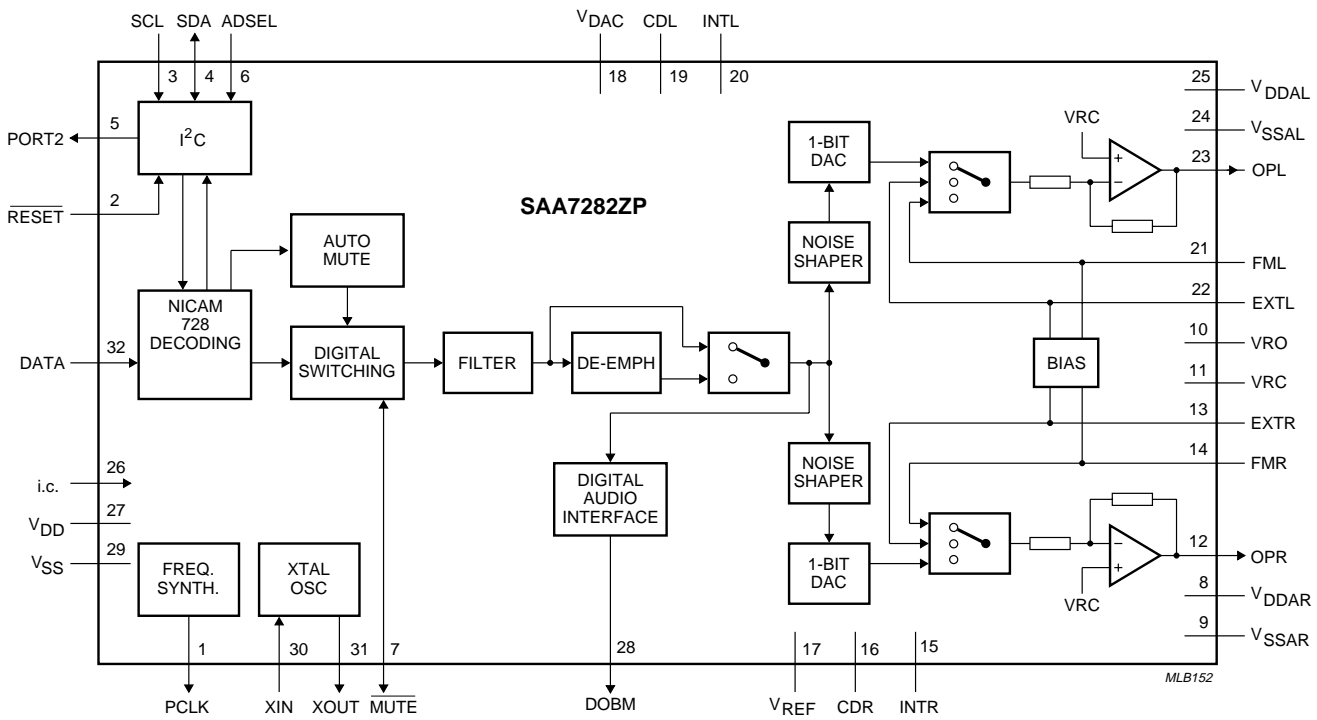


Fig.1 Block diagram; pin numbering for SOT232A.

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## PINNING

SYMBOL	SOT205AG	SOT232A	DESCRIPTION
DOBM	1	28	digital audio interface output
V <sub>SS</sub>	2	29	ground connection for the digital section
n.c.	3	–	not connected
XIN	4	30	crystal input at 256fs (8.192 MHz)
XOUT	5	31	crystal output at 256fs (8.192 MHz)
DATA	6	32	serial data input at 728 kbits/s from DQPSK demodulator
PCLK	7	1	output clock at 728 kHz to DQPSK demodulator
RESET	8	2	active LOW reset; used to set the device in a valid initial condition
SCL	9	3	clock input for I <sup>2</sup> C control bus
SDA	10	4	data port for I <sup>2</sup> C control bus, input/open drain output
PORT2	11	5	output mirroring the I <sup>2</sup> C control register bit PORT2
n.c.	12	–	not connected
ADSEL	13	6	I <sup>2</sup> C-bus slave address selection input; allows selection of one of two separate slave addresses, defaults to logic 1
MUTE	14	7	active LOW mute input; when set LOW, sets the digital data to zero and either silences the output or switches it to analog FM, depending on the status of MUTEDEF (control bit in the I <sup>2</sup> C register) and RSSF; overridden by automute (if automute is used, then MUTE is automatically pulled LOW)
n.c.	15 to 17	–	not connected
V <sub>DDAR</sub>	18	8	analog supply voltage for the right audio channel
V <sub>SSAR</sub>	19	9	analog ground connection for the right audio channel
VRO	20	10	internal reference voltage buffer output
VRC	21	11	internal reference voltage buffer HIGH impedance node
n.c.	22	–	not connected
OPR	23	12	analog output from the right audio channel
EXTR	24	13	external analog input to the right audio channel
FMR	25	14	FM sound input to the right audio channel
INTR	26	15	integrator output from the right audio channel
CDR	27	16	integrator connection to an external damping capacitor
n.c.	28	–	not connected
V <sub>REF</sub>	29	17	reference voltage input; 2.5 V (typical)
V <sub>DAC</sub>	30	18	quiet V <sub>SS</sub> to DACs
CDL	31	19	integrator connection to an external damping capacitor
INTL	32	20	integrator output from the left audio channel
FML	33	21	FM sound input to the left audio channel
EXTL	34	22	external analog input to the left audio channel
OPL	35	23	analog output from the left audio channel
n.c.	36	–	not connected
V <sub>SSAL</sub>	37	24	analog ground connection for the left audio channel
V <sub>DDAL</sub>	38	25	analog supply voltage for the left audio channel

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SYMBOL	SOT205AG	SOT232A	DESCRIPTION
n.c.	39 to 41	–	not connected
i.c.	42	26	internally connected; must be left open-circuit in application
n.c.	43	–	not connected
V <sub>DD</sub>	44	27	digital supply voltage

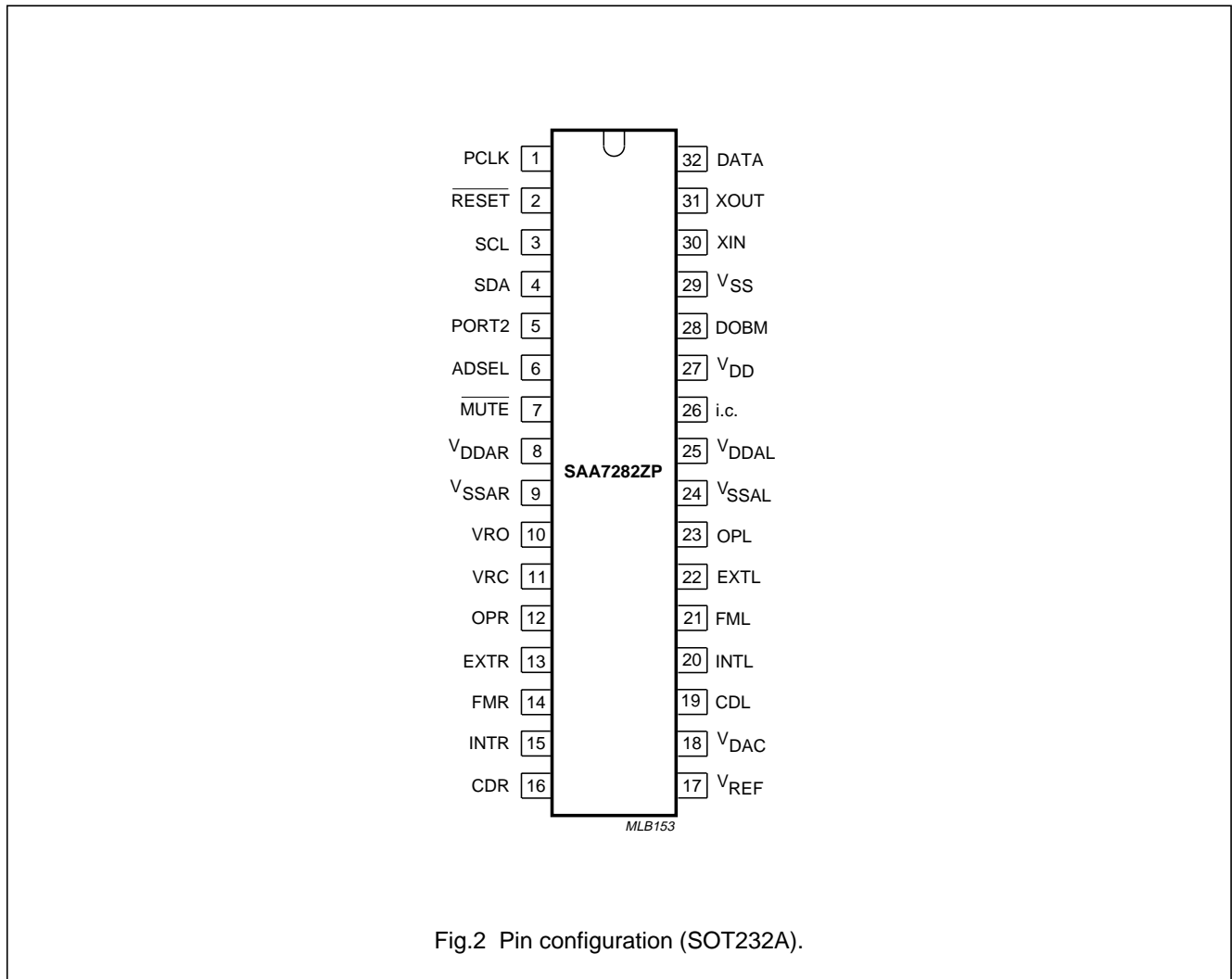


Fig.2 Pin configuration (SOT232A).

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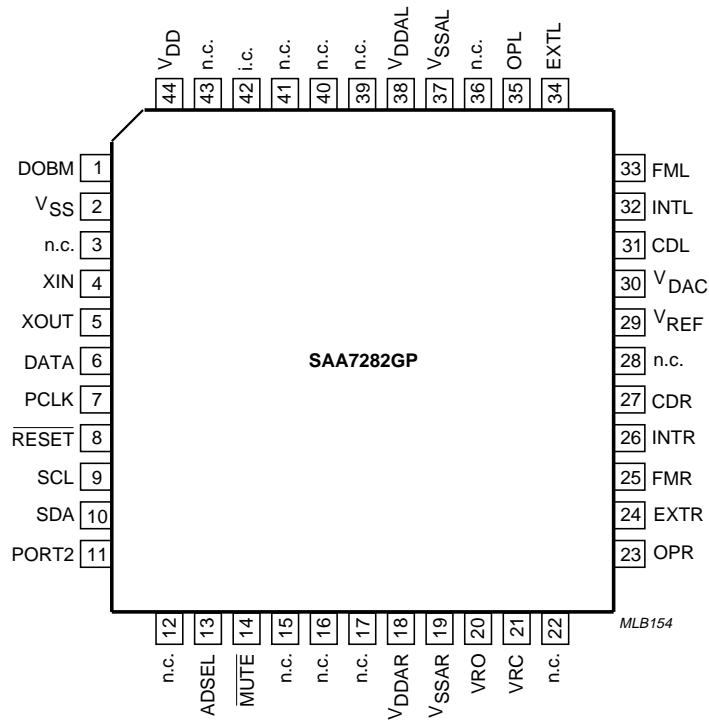


Fig.3 Pin configuration (SOT205AG).

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**I<sup>2</sup>C-BUS FORMATS**

The SAA7282 contains an I<sup>2</sup>C-bus slave transceiver permitting a master device to:

- Read decoder status information derived from the transmitted digital audio signal
- Read an error count byte to determine the bit error rate for user mute purposes and to indicate quality of NICAM signal
- Read additional transmitted data bits. Their purpose has yet to be defined but accessibility is provided to allow future services to be implemented in receiver software
- Write control codes to select the available analog switching configurations
- Write upper and lower error count limits for automatic muting function

The device slave address is  $A(7:1)(\overline{R/\overline{W}}) = 101101X(\overline{R/\overline{W}})$ . An ADSEL pin is provided to allow selection of one of two different slave addresses via programmable address bit A1. (X = ADSEL logic level).

The SAA7282 does not acknowledge the I<sup>2</sup>C-bus general call address.

**The slave receiver format is:**

S SLAVE\_ADDR.0 ACK SUB\_ADDR ACK DATA BYTE ACK P

<-n bytes->

Where S = start, ACK = acknowledge, P = stop.

Auto-increment of the sub-address is provided with wrap-around from 02 (HEX) to 00 (HEX).

The slave receiver data byte format, as a function of sub-address, is as shown in Table 1.

**Table 1** Slave receiver data byte.

SUB-ADDRESS	RESET VALUE HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	90	M1/ $\overline{M2}$	DMSEL	SSWIT3	SSWIT2	SSWIT1	PORT2	MUTEDEF	AMDIS
01	50	EMAX7	EMAX6	EMAX5	EMAX4	EMAX3	EMAX2	EMAX1	EMAX0
10	14	EMIN7	EMIN6	EMIN5	EMIN4	EMIN3	EMIN2	EMIN1	EMIN0

**M1/ $\overline{M2}$** 

This bit in conjunction with DMSEL bit, determines the output configuration in dual mono mode (see Table 2).

Power-on resets to logic 1.

**DMSEL**

This bit determines whether one or both of the dual mono signals are output (see Table 2). Power-on resets to logic 0.

**PORT2**

PORT2 controls a bit out, providing direct access to a dedicated output pin (PORT2) via the I<sup>2</sup>C-bus. See Table 3.

Power-on resets to logic 0.

**SSWIT3/2/1**

These bits control the analog switching, selecting between the FM, external, and NICAM signals. With the NICAM source the signals select whether the de-emphasis is performed and what gain is applied after the filtering and de-emphasis stage. The signal states and their meaning are listed in Table 4. Power-on resets to 0/1/0.

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## AMOGMDIS

This bit enables and disables the automute function (which is activated according to the error limit registers).

Power-on resets to enabled (i.e. AMDIS = logic 0). AMDIS should be disabled for the user definable mute ( $\overline{\text{MUTE}}$ ) to be used.

## MUTEDEF

This defines the operation of the user definable  $\overline{\text{MUTE}}$  pin when it is pulled LOW externally. If MUTEDEF is HIGH and RSSF = logic 1, the output of the device is switched to FM input. If MUTEDEF is HIGH and RSSF = logic 0, or if MUTEDEF is LOW, the output is muted. Power on resets to LOW.

## ERROR LIMIT REGISTERS

## UPPER ERROR LIMIT REGISTER

This defines the number of errors in 128 ms period which will cause automute to switch IN. User definable, but power on resets to 50 Hex.

## LOWER ERROR LIMIT REGISTER

This defines the number of errors in 128 ms period which will cause automute to switch OUT. User definable, but power on resets to 14 Hex.

**Table 2** Output as a function of  $\overline{\text{M1/M2}}$  and DMSEL.

DMSEL	$\overline{\text{M1/M2}}$	FUNCTION
0	0	selects DIGITAL; L = M2, R = M2
0	1	selects DIGITAL; L = M1, R = M1
1	0	selects DIGITAL; L = M2, R = M1
1	1	selects DIGITAL; L = M1, R = M2

**Table 3** Port 2 control.

PORT2	PIN OUTPUT STATE
0	LOW
1	HIGH

**Table 4** SSWIT signal states and function.<sup>(1)</sup>

SSWIT3	SSWIT2	SSWIT1	FUNCTION
0	0	0	NICAM source de-emphasis switched out, no gain
0	0	1	NICAM source de-emphasis switched in, no gain
0	1	0	NICAM source de-emphasis switched in, -6 dB gain; power-on reset state
0	1	1	NICAM source de-emphasis switched in, +12 dB gain
1	x	0	external inputs switched in, no change to previous de-emphasis/gain setting
1	x	1	FM inputs switched in, no change to previous de-emphasis/gain setting

**Note**

1. Where x = don't care.



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**Slave Transmitter**

The slave transmitter formats are illustrated thus:

- S SLAVE\_ADDR.1 A STATUS\_BYTE NA P

In this format the bus master reads the STATUS\_BYTE once.

- S SLAVE\_ADDR.1 A STATUS\_BYTE A ERROR\_BYTE NA P

In this format the bus master reads two bytes of STATUS\_BYTE and ERROR\_BYTE.

- S SLAVE\_ADDR.1 A STATUS\_BYTE A ERROR\_BYTE A AD\_BYTE\_0 A AD\_BYTE\_1 NA P

In this format the bus master reads four bytes of STATUS\_BYTE, ERROR\_BYTE and two additional bytes, AD\_BYTE\_0 and AD\_BYTE\_1. The additional data bytes contain the eleven additional data bits AD0 to AD10 together with information regarding their status.

Where NA = no acknowledge.

**Table 5** Data byte formats.

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
STATUS_BYTE	PONRES	$S/\bar{M}$	$D/\bar{S}$	VDSP	RSSF	$\bar{O}S$	AM	$\bar{C}FC$
ERROR_BYTE	E7	E6	E5	E4	E3	E2	E1	E0
AD_BYTE_0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
AD_BYTE_1	OVW	SAD	0	CI2	CI1	AD10	AD9	AD8

The bits may be defined as follows:

**PONRES**

This bit is a power-on reset detection bit. It is set HIGH after a power-on reset or supply reduction and is cleared LOW when the STATUS\_BYTE is read.

 **$S/\bar{M}$  (stereo/mono indication)**

$S/\bar{M}$  = logic 1 indicating an incoming stereo transmission.  
 $S/\bar{M}$  = logic 0 indicating that the incoming transmission is not stereo.

 **$D/\bar{S}$  (dual/single mono indication)**

$D/\bar{S}$  = logic 1 indicating an incoming dual mono transmission.  
 $D/\bar{S}$  = logic 0 indicating that the incoming transmission is not dual mono.

**VDSP**

This bit indicates that the decoded signal is valid digital sound. When VDSP = logic 0 the incoming transmission carries either a 704 kbit/s transparent data channel or a currently undefined format and the device automatically switches to FM regardless of RSSF.

**RSSF**

RSSF is the reserve sound switching flag indication equal to the C4 bit in the NICAM transmission. RSSF = logic 1 when the FM sound signal is carrying the same programme material as the digitally modulated carrier (specifically the M1 signal in the event of a dual mono transmission). RSSF = logic 0 when the FM signal is not reproduced within the digital signal.

 **$\bar{O}S$** 

This bit provides an active LOW indication that the decoder is out of sync. If  $\bar{O}S$  = logic 1 the decoder is frame synchronized and has obtained C0 (16 frame) sync. If  $\bar{O}S$  = logic 0, the decoder is out of sync and the indicator bits are as given in Table 6.

**AM**

This bit indicates when the automuting function has switched from the NICAM sound to the conventional FM sound. This enables the software controller to display the relevant information to the customer, for example, on screen display. If AM bit = logic 0 no switching has been carried out by the automuting function. If AM bit = logic 1 then the automuting function has switched to the FM inputs.

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 $\overline{\text{CFC}}$ 

Signals a change of configuration at the 16-frame boundary. It is cleared to logic 1 by the I<sup>2</sup>C-bus reading the status register.

## E7 to E0

This is an error count byte which counts the number of error flags in a 128 ms period. The register is updated every 128 ms.

## AD10 to AD0

These are the additional data bits from the transmission and are updated every 1 ms. This provides a data capacity of 11 kbit/s.

## SAD

SAD is the 'status additional data' bit. This is set to logic 1 when new bits AD10 to AD0 are latched into the I<sup>2</sup>C-bus registers. It is automatically reset to logic 0 when AD\_BYTE\_1 is read by the bus master.

## OVW

OVW is the overwrite indicator for the additional data. This bit is set when the transmission overwrites additional data bits which have not been read by the bus master. This bit is automatically reset to logic 0 when AD\_BYTE\_1 is read by the bus master.

## CI1 to CI2

These represent the CI bits which are extracted by a majority logic process from the parity checks of the last ten samples in a frame (samples 55 to 64). CI1 will be conveyed by the parity grouping of samples 55 to 59 and CI2 will be conducted by the parity grouping of samples 60 to 64. Both parity groups will be even for UK transmissions such that CI2 = logic 0 and CI1 = logic 0. The transmissions of countries following the specification issued by the EBU (Document SPB424; "Digital sound transmissions in terrestrial television") will allow odd or even parity groups, thus providing an additional 2 kbit/s data capacity.

**Table 6** Indicator bits functional truth table.

TRANSMISSION	C1	C2	C3	$\overline{\text{S/M}}$	$\overline{\text{D/S}}$	VDSP	$\overline{\text{OS}}$
Stereo	0	0	0	1	0	1	1
M1 + M2	0	1	0	0	1	1	1
M1 + data	1	0	0	0	0	1	1
Transparent data	1	1	0	0	0	0	1
Any currently undefined combination of C1, C2, C3				0	0	0	1
Decoder unsynchronized ( $\overline{\text{OS}}$ = logic 0)				note 1	note 1	0	0

**Note**

1. Holds last value before synchronization loss or stereo ( $\overline{\text{S/M}}$  = logic 1;  $\overline{\text{D/S}}$  = logic 0) if synchronization not achieved since power-on reset.

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## DIGITAL AUDIO INTERFACE IEC/EBU 958

### Block structure

The output is grouped into a block of 192 consecutive frames providing, for each channel the 192 channel status data bits. The start of a block is designated by a special sub-frame preamble.

### Frame structure

Each frame is uniquely composed of two sub-frames. The rate of transmission of frames corresponds exactly to the source sampling frequency. In the 2-channel operation, samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. Sub-frames related to Channel 1 (left or 'A' channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However the preamble is changed to preamble B once every 192 frames. This defines the block structure used to organize the channel status information. Sub-frames of Channel 2 (right or 'B' channel in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

### Sub-frame structure

Each frame is divided into 32 time-slots numbered 0 to 31.

Time-slots 0 to 3 carry one of three permitted preambles. These are used to affect synchronization of sub-frames, frames and blocks.

Time-slots 4 to 27 carry the audio sample word in linear two's complement representation. The most significant bit is carried by time-slot 27.

Time-slot 28 carries the validity flag associated with the audio sample word. This flag is set to logic 0 if the audio sample is reliable. If set to logic 1 then the sample is unreliable.

Time-slot 29 carries one bit of the user data channel. In this application this is not used and so is set to logic 0.

Time-slot 30 carries one bit of the channel status word associated with the audio channel transmitted in the same sub-frame.

Time-slot 31 carries a parity bit such that time-slots 4 to 31 inclusive will carry an even number of ones and an even number of zeros.

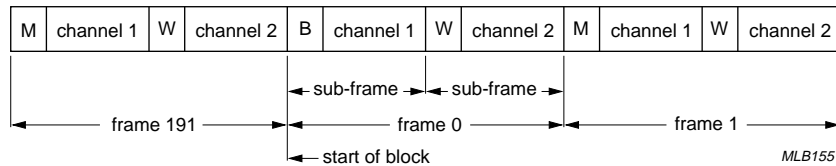


Fig.4 Frame format.

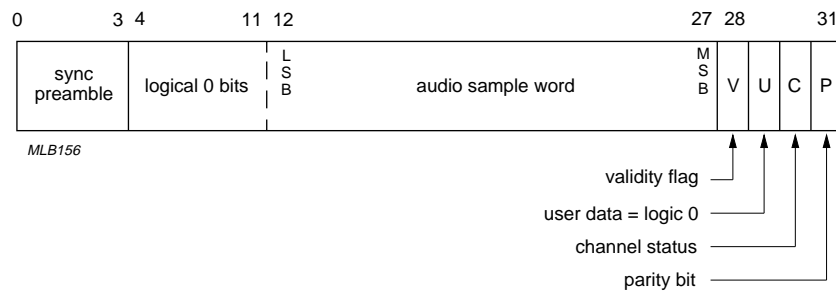


Fig.5 Sub-frame format.

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## Channel coding

Time-slots are encoded as biphase mark data. Each bit transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit being transmitted is logic 0, however it is different if the bit is logic 1 (see Table 7).

**Table 7** Channel coding.

Preceding state	0	1
Transmitted bit	Channel coding	
0	11	00
1	10	01

## Preambles

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks. A set of three preambles is used. These preambles are transmitted in the time allocated to four time-slots and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol. Depending on this state the preambles are as shown in Table 8.

**Table 8** Preambles.

Preceding state	0	1
Preamble	Channel coding	
B	11101000	00010111
M	11100010	00011101
W	11100100	00011011

The preambles preceding each digital audio sample are used to indicate the beginning of a sample as follows:

- **Preamble B** indicates the start of Channel A data and the beginning of a block
- **Preamble M** indicates the start of Channel A data but not the beginning of a block
- **Preamble W** indicates the start of Channel B data.

## Channel status

The channel status information is organized in 192-bit words. The first bit of each word is carried in the frame with Preamble B. The 192-bit word is organized into sections as shown in Table 9.

**Table 9** Channel status codes.

BIT	CODE	DESCRIPTION
0	0	consumer
1	0	sound data
2	1	digital copy permitted
3, 4	00	indicates digital de-emphasis switched in
	11	indicates digital de-emphasis switched out
5	0	
6, 7	00	
8 to 15	00110001	category code
16 to 19	0000	source code (don't care)
20 to 23	0000	channel number (don't care)
24 to 27	1100	sampling frequency (32 kHz)
28, 29	00	clock accuracy (level II)
30 to 191	all 0s	

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**LIMITING VALUES**

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD}$	supply voltage (all supplies)	note 1	-0.5	+6.5	V
$V_{I(max)}$	maximum input voltage (any input)		-0.5	$V_{DD}+0.5$	V
$V_{O(max)}$	maximum output voltage		-0.3	$V_{DD}+0.5$	V
$I_{IOK}$	DC input or output diode current		-	$\pm 20$	mA
$I_{O(max)}$	output current (each output)		-	$\pm 10$	mA
$T_{amb}$	ambient operating temperature		0	+70	°C
$T_{stg}$	storage temperature		-55	+125	°C
$V_{stat}$	electrostatic handling	notes 2 and 3	-2000	+2000	V

**Notes**

1. All  $V_{DD}$  and  $V_{SS}$  connections must be made externally to the same power supply.
2. Electrostatic handling is equivalent to discharging a 100 pF capacitor via a 1.5 k $\Omega$  series resistor with a 15 ns rise time.
3. 1000 V  $V_{SSAL}$  pin.

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**CHARACTERISTICS** $V_{DD} = 4.5$  to  $5.5$  V;  $T_{amb} = 0$  to  $+70$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{DD}$	supply voltage	see Fig.9	4.5	5.0	5.5	V
$I_{DD}$	total supply current		–	50	100	mA
$V_{SS}, V_{SSAL}$ $V_{SSAR}, V_{DAC}$	ground supply voltage		0	–	0	V
$V_{DDAL},$ $V_{DDAR}$	analog supply voltage	see Fig.9	4.5	5.0	5.5	V
<b>Digital inputs</b>						
DATA						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{DD}$	V
$I_{LI}$	input leakage current		–10	–	+10	$\mu$ A
$C_I$	input capacitance		–	–	10	pF
ADSEL (this pin is internally pulled HIGH when not connected)						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{DD}$	V
$Z_I$	input impedance		–	50	–	k $\Omega$
$C_I$	input capacitance		–	–	10	pF
$\overline{\text{RESET}}$ (Schmitt trigger input)						
$V_{IL}$	LOW level input voltage		0	–	1.5	V
$V_{IH}$	HIGH level input voltage		3.0	–	$V_{DD}$	V
$V_{hys}$	hysteresis		$0.05V_{DD}$	–	–	V
SCL						
$V_{IL}$	LOW level input voltage		0	–	1.5	V
$V_{IH}$	HIGH level input voltage		3.0	–	$V_{DD}$	V
$V_{hys}$	hysteresis		$0.05V_{DD}$	–	–	V
$I_{LI}$	input leakage current		–10	–	+10	$\mu$ A
$C_I$	input capacitance		–	–	10	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Digital input/output</b>						
SDA						
V <sub>IL</sub>	LOW level input voltage		0	–	1.5	V
V <sub>IH</sub>	HIGH level input voltage		3.0	–	V <sub>DD</sub>	V
V <sub>hys</sub>	hysteresis		0.05V <sub>DD</sub>	–	–	V
I <sub>LI</sub>	input leakage current		–10	–	+10	μA
C <sub>I</sub>	input capacitance		–	–	10	pF
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = 3 mA	0	–	0.4	V
C <sub>L</sub>	load capacitance					
	active pull-up		–	–	400	pF
	passive pull-up		–	–	200	pF
MUTE I/O (this pin has an internal pull-up)						
V <sub>IL</sub>	LOW level input voltage		0	–	0.8	V
V <sub>IH</sub>	HIGH level input voltage		2.0	–	V <sub>DD</sub>	V
C <sub>I</sub>	input capacitance		–	–	10	pF
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = 2.8 mA	0	–	0.4	V
V <sub>OH</sub>	HIGH level output voltage		2.4	–	V <sub>DD</sub>	V
C <sub>L</sub>	load capacitance		–	–	50	pF
Z <sub>I</sub>	input impedance		–	50	–	kΩ
<b>Digital outputs</b>						
PORT2, PCLK, DOBM						
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = 2.8 mA	0	–	0.4	V
V <sub>OH</sub>	HIGH level output voltage	I <sub>OH</sub> = 800 μA	2.4	–	V <sub>DD</sub>	V
C <sub>L</sub>	load capacitance		–	–	50	pF
<b>Crystal oscillator</b>						
f <sub>c</sub>	crystal frequency		–	8.192	–	MHz
gm	mutual conductance	at 100 kHz	1.5	–	–	mA/V
Av	small signal gain	Av = gm.Ro	3.5	–	–	V/V
C <sub>I</sub>	input capacitance		–	–	10	pF
C <sub>FB</sub>	feedback capacitance		–	–	5	pF
C <sub>O</sub>	output capacitance		–	–	10	pF
XIN						
V <sub>IL</sub>	LOW level input voltage		0	–	1	V
V <sub>IH</sub>	HIGH level input voltage		3.5	–	V <sub>DD</sub>	V
I <sub>LI</sub>	input leakage current		–10	–	+10	μA
C <sub>I</sub>	input capacitance		–	–	10	pF

## Terrestrial Digital Sound Decoder (TDSD2)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Digital filter specification</b>						
$f_s$	output sample frequency		–	128	–	kHz
PR	pass band ripple	at 0 Hz to 15 kHz	–	–	$\pm 0.01$	dB
SBA	stop band attenuation	at $f \geq 17$ kHz	30	–	–	dB
<b>Digital de-emphasis</b>						
DEV	deviation from ideal		–	–	$\pm 0.09$	dB
<b>ANALOG SECTION</b> (measured at $V_{DD} = 5$ V and $T_{amb} = 25$ °C)						
<b>Reference voltage buffer</b>						
VRC output						
$V_{rc}$	voltage reference at VRC	see Fig.10	$0.45V_{DDAR}$	$0.5V_{DDAR}$	$0.55V_{DDAR}$	V
<b>DACs</b>						
$V_{REF}$ input						
$V_{ref}$	reference input voltage		–	$0.5V_{DD}$	–	V
<b>Switching operational amplifiers</b>						
$C_L$	output load capacitance		–	–	300	pF
$R_L$	output load resistance		3	–	–	k $\Omega$
$Z_O$	output impedance		–	150	–	$\Omega$
G	output gain		–0.35	0	+0.35	dB
PSRR	power supply rejection ratio		–	40	–	dB
External inputs selected (FML, FMR, EXTL, EXTR)						
$V_{ain}$	input voltage level (RMS value)		–	–	1.1	V
S/N	signal-to-noise ratio (relative to 1 V RMS, unity gain)	FM or EXT	90	100	–	dB
THD	total harmonic distortion (unity gain, O/P = 1 V RMS)	FM or EXT	–	–90	–70	dB
CHM	channel matching	FM or EXT, 1 kHz	–	0	0.5	dB
NICAM inputs selected (INTL, INTR)						
$V_{ain}$	input voltage level (RMS value)	at 0 dB; $V_{REF} = 2.5$ V	0.9	1.0	1.1	V
THD+N	total harmonic distortion plus noise	NICAM 728; notes 2 and 3	–	–80	–75	dB
CHM	channel matching	0 dB, 1 kHz	–	0	0.5	dB
DIGS	digital silence level	$\overline{MUTE}$ on	–	–80	–	dB
<b>Timing (all timing values refer to <math>V_{IH}</math> and <math>V_{IL}</math> levels)</b>						
DATA with respect to PCLK (see Fig.7)						
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		250	–	–	ns



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>SDA with respect to SCL</b> (see Fig.8)						
f <sub>SCL</sub>	SCL clock frequency		0	–	400	kHz
t <sub>BUF</sub>	bus free time		1300	–	–	ns
t <sub>HD;STA</sub>	start code hold time		600	–	–	ns
t <sub>LOW</sub>	SCL clock LOW time		1300	–	–	ns
t <sub>HIGH</sub>	SCL clock HIGH time		600	–	–	ns
t <sub>SU;STA</sub>	start code set-up time		600	–	–	ns
t <sub>HD;DAT</sub>	data hold time	note 4	0	–	–	ns
t <sub>SU;DAT</sub>	data set-up time	note 5	100	–	–	ns
t <sub>r</sub>	SDA and SCL rise time		50	–	300	ns
t <sub>f</sub>	SDA and SCL fall time		50	–	300	ns
t <sub>SU;STO</sub>	stop code set-up time		600	–	–	ns
t <sub>of</sub>	output fall time	note 6	50	–	200	ns

**Notes**

1. Outputs OPL and OPR are measured with external components as recommended in Fig.11.
2. Total analog performance is limited by dynamic range of the NICAM 728 system. Due to compansion the quantization noise is never lower than approximately -62 dB with respect to the input level.
3. Measured with a -30 dB, 1 kHz NICAM 728 input signal.
4. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.
5. If a fast I<sup>2</sup>C-bus device is used in an up to 100 kbit/s I<sup>2</sup>C-bus system, then the requirement t<sub>SU;DAT</sub> ≥ 250 ns is always fulfilled if this device cannot stretch the LOW level of the SCL signal. If a device stretches the LOW level of the SCL signal, then data to SD9A must be asserted (t<sub>RD(max)</sub> + t<sub>SU;DAT</sub>) = 1000 + 250 = 1250 ns before the SCL signal is released to be compatible with the up to 100 kbit/s I<sup>2</sup>C-bus specification.
6. The output fall time is measured between 3.0 V and 1.5 V for a bus capacitance of 400 pF and an active pull-up.

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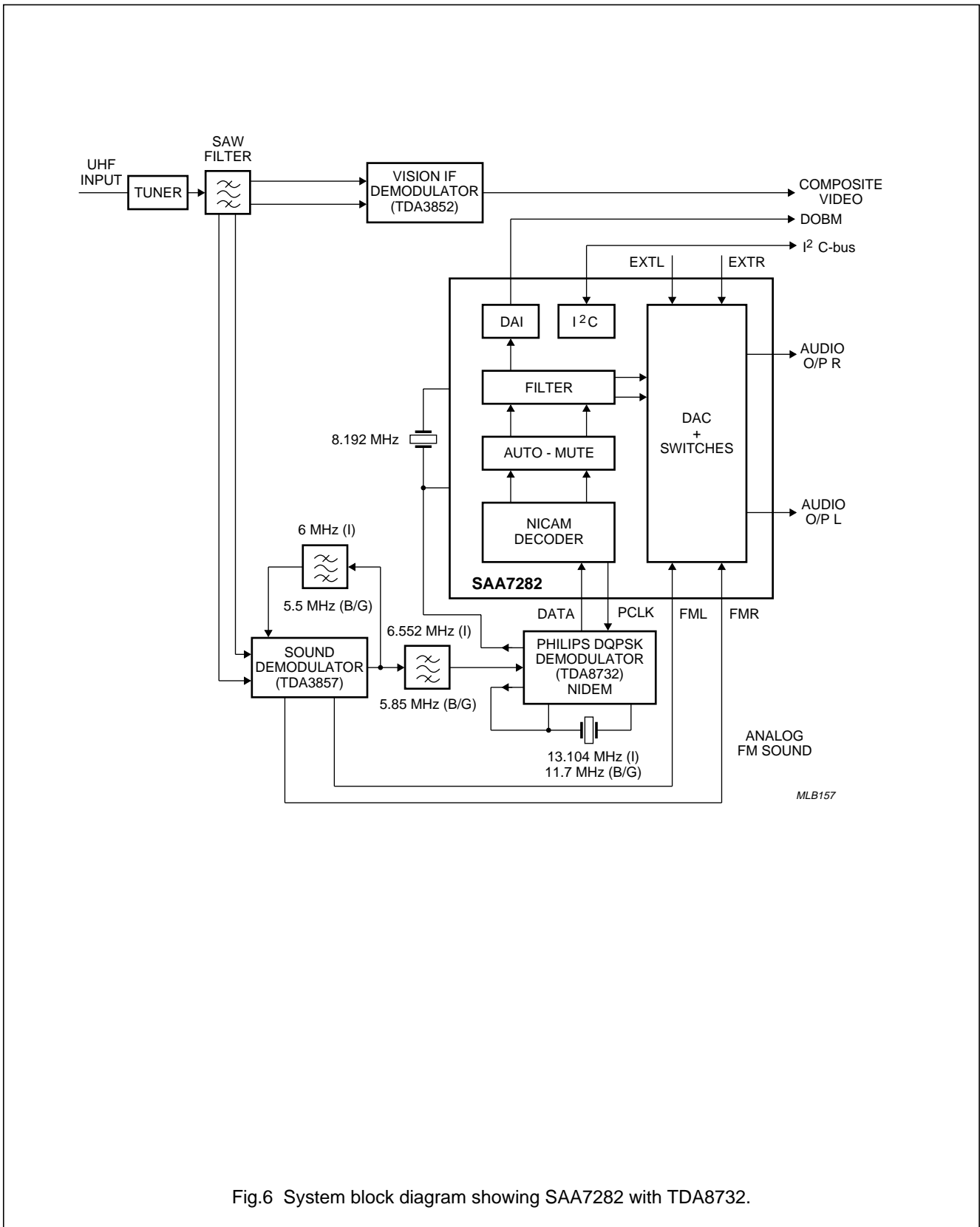


Fig.6 System block diagram showing SAA7282 with TDA8732.

# Terrestrial Digital Sound Decoder (TDSD2)

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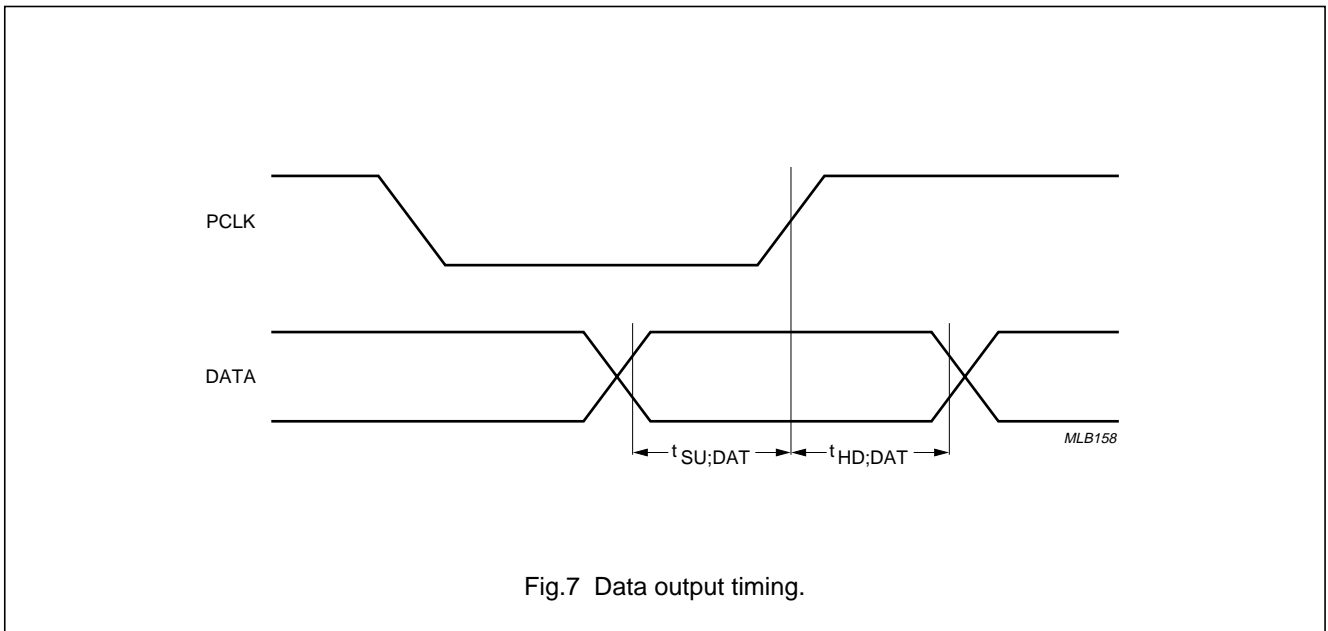


Fig.7 Data output timing.

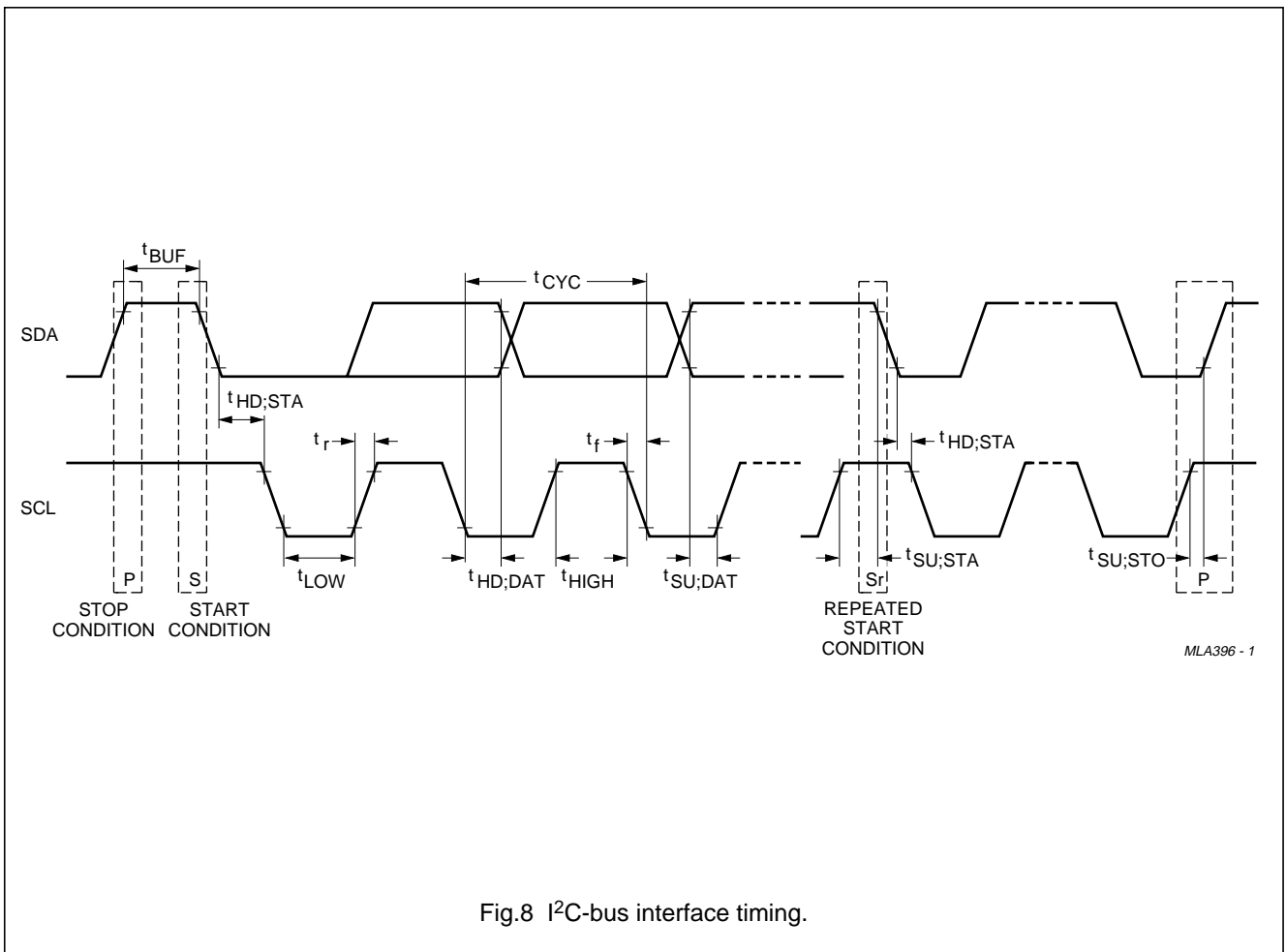


Fig.8 I<sup>2</sup>C-bus interface timing.

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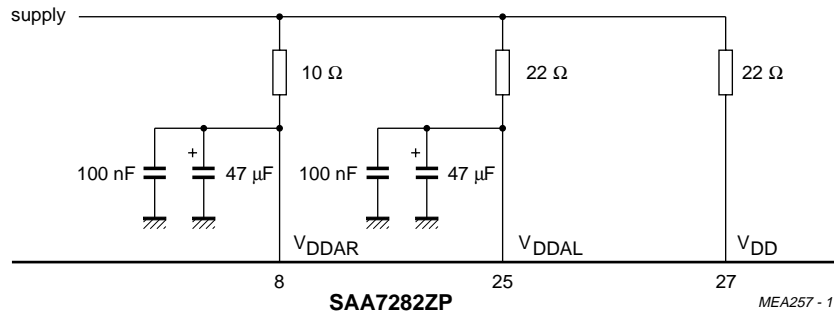


Fig.9 V<sub>DD</sub> external circuitry.

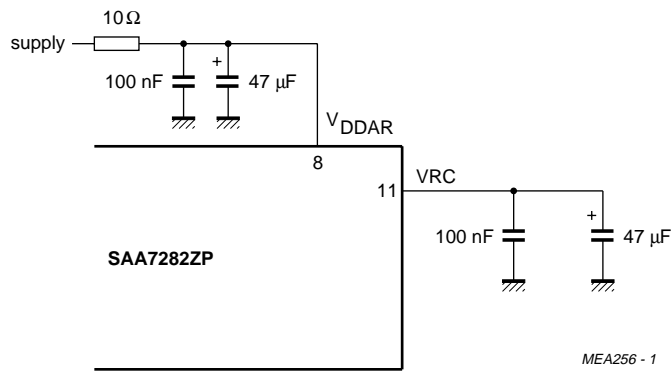


Fig.10 VRC external circuitry (same external circuit values also required for VRO).

# Terrestrial Digital Sound Decoder (TDSD2)

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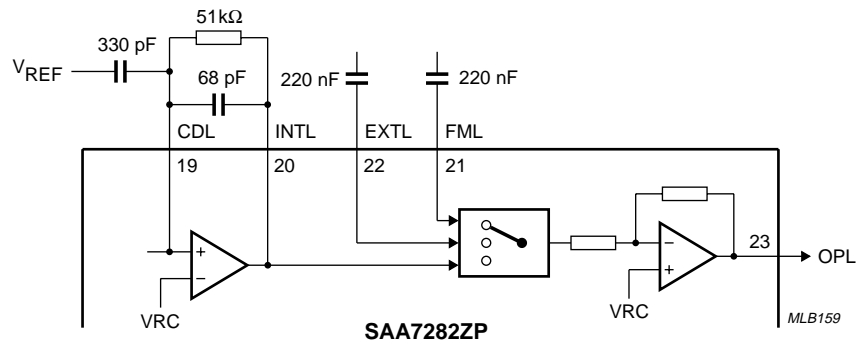


Fig.11 External circuitry for left channel DAC (same external circuit values also required for right channel DAC).

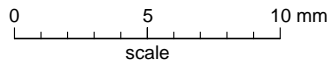
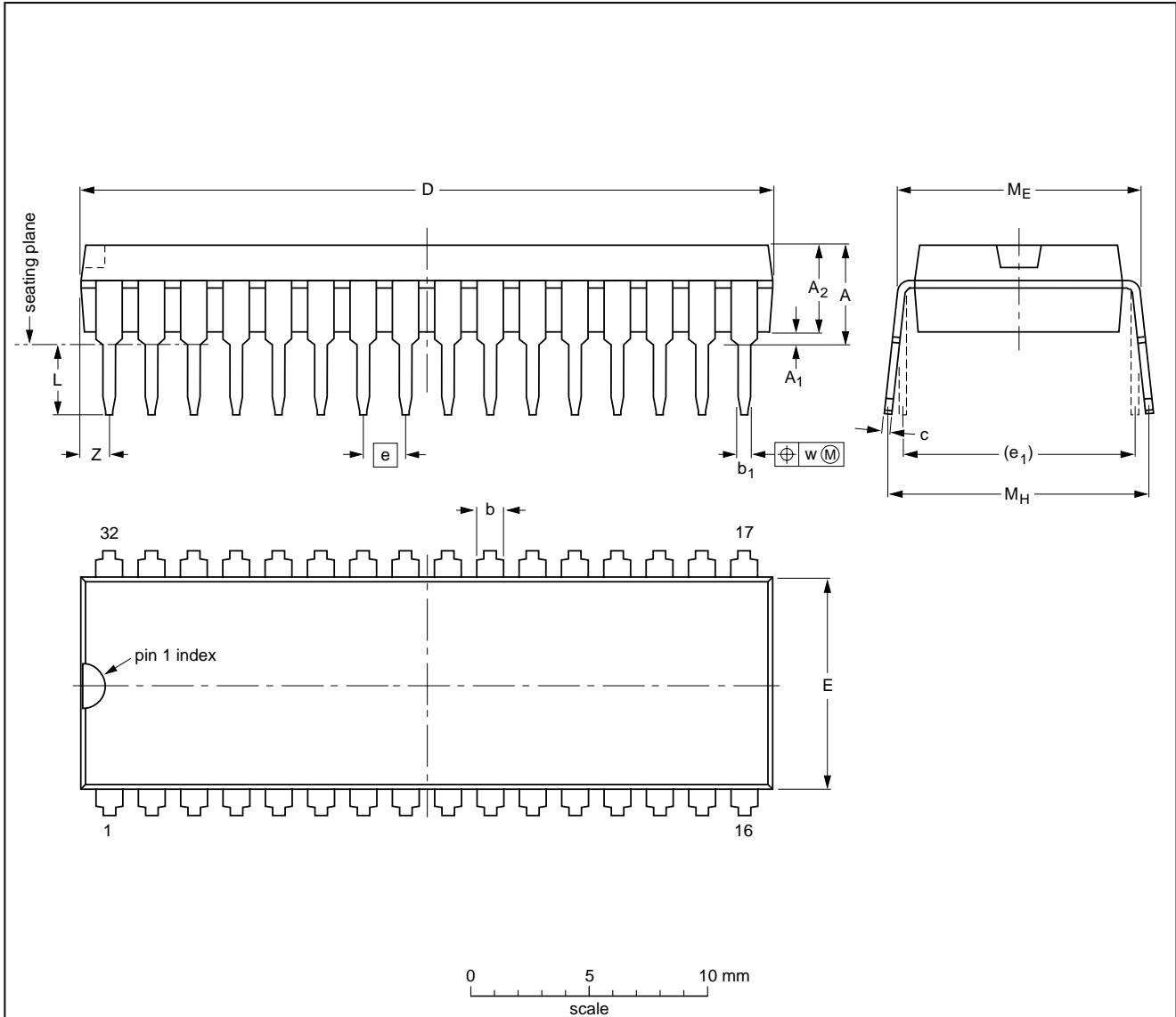
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PACKAGE OUTLINES

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil)

SOT232-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

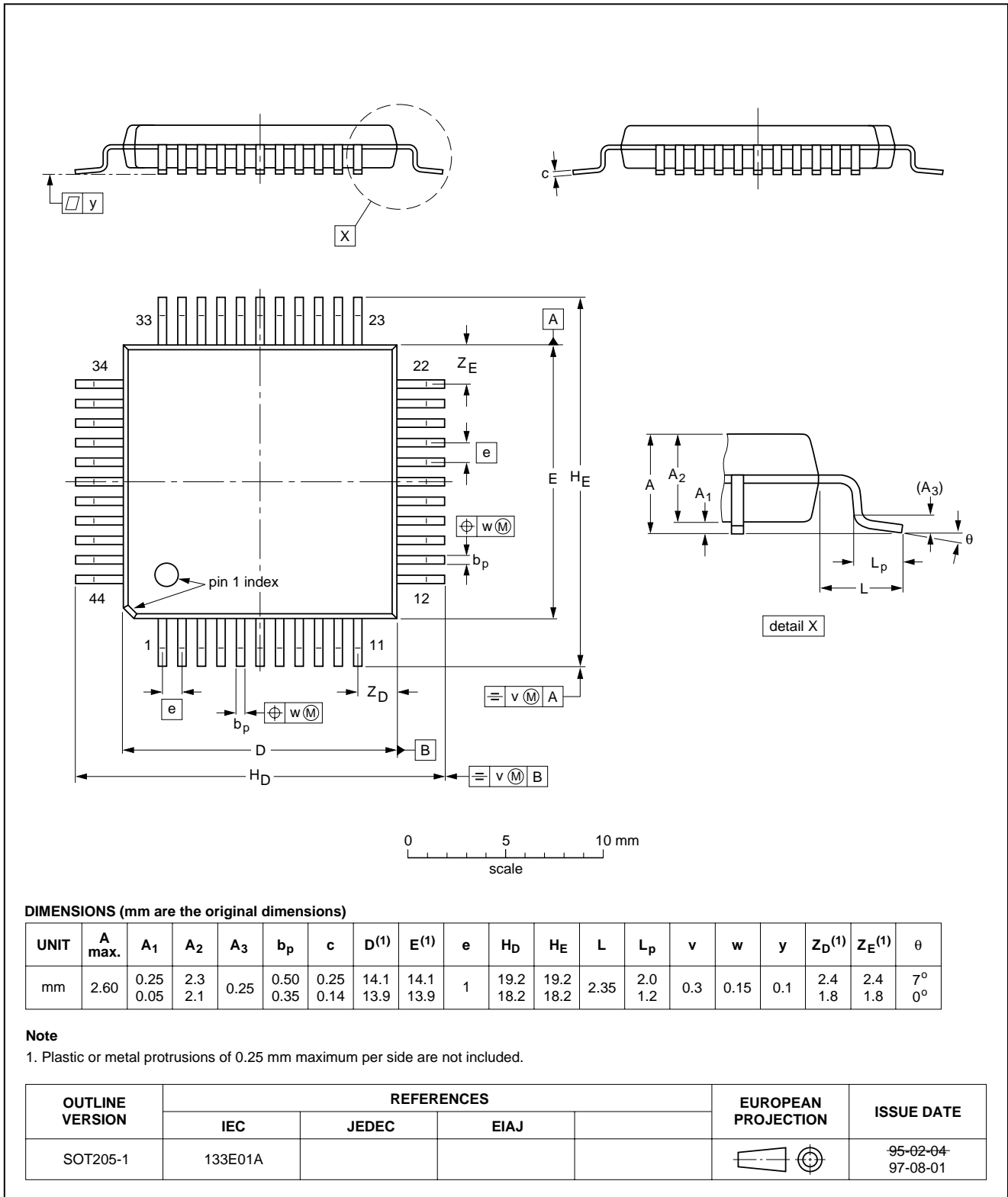
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						92-11-17 95-02-04

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QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm

SOT205-1



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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

#### SDIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### QFP

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

#### **If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

**Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

**PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS**

Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.