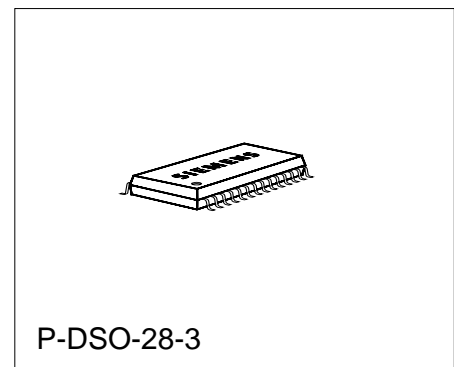


Preliminary Data

MOS IC

### Features

- On-chip PLL
- Full frame display for 50/60 Hz in order to increase the vertical resolution and to suppress moving artifacts.
- Compatibility to the 16:9 display format by means of independent setting of the vertical and horizontal decimation factors and the width of the border frame
- Decimation of the Y, U, V data for pictures sizes 1/9 and 1/16 with 6 bits width of the input word without rounding error
- Intermediate storage of the inset picture (on-chip-memory)
- RGB- or Y-, U-, V-signal generation
- 100% pin- and software compatible with SDA 9188X if external PLL is used
- Increased bandwidth of analog outputs due to higher output currents
- New select function for multi-PIP feature



| Type        | Ordering Code | Package                    |
|-------------|---------------|----------------------------|
| SDA 9188-3X | Q67100-H5142  | P-DSO-28-3 (350 mil) (SMD) |

### Functional Description

The SDA 9188-3X Picture-in-Picture (PIP) processor with on-chip PLL combines two asynchronous picture sources so that a small moving picture (the inset picture) can be superimposed in a moving picture of normal size (the parent picture).

The components of the video signal of the inset source have to be fed in a digitized form to the SDA 9188-3X (**figure 1**). Amplitude resolution of the signal components is 6 bit at a sampling rate of 13.5 MHz for the luminance signal and 3.375 MHz for the chrominance signals.

The PIP processor SDA 9188-3X handles picture reduction (decimation with horizontally and vertically acting filters), intermediate data storage in an integrated image memory (169.812 bits) as well as the output of the decimated picture.

The picture can be set 1/9 or 1/16 of its original size. In order to indicate the border between parent picture and inset picture the inset picture can be surrounded with a frame: its width is adjustable in 2 stages and its brightness in 16 stages. Different signal sources can be identified by using different framing colors. The four corners of the parent picture are possible positions for the inset picture. The inset picture can also be inserted as a still picture, independently of the parent picture.

The output signals of the SDA 9188-3X are analog. Either RGB or Y, U, V signals can be output, whereby a 6-bit broadband conversion is obtained for all components. Clamping for RGB output signal is performed in an RGB processor (e.g. TDA 4685).

Only a few additional devices are required for a complete picture-in-picture system. **Application circuits 1a and 1b** illustrate the use of the PIP device.

If the CVBS input signal is to be decoded using an analog color decoder for the PIP, the analog/digital interface for the inset picture (3 A/D Converter, SDA 9187-2X) performs the conversion of the Y, U, V components into digital signals as well as the generation of the inset clocks BLNI and LL3I.

The SDA 9188-3X processes both 50 Hz/625 and 60 Hz/525 line signals. The field frequency can be 50/60 Hz or 100/120 Hz. For systems with Siemens Dig TV Featurebox a field frequency of 100 Hz or 120 Hz is also possible by doubling the clock frequency LL3P (LL1.5P). Frame mode display with 50 Hz or 60 Hz can also be set via the I<sup>2</sup>C bus. Adaptation to the number of lines occurs automatically. If the field frequency in the parent and inset channels are different, artifacts may result in the picture.

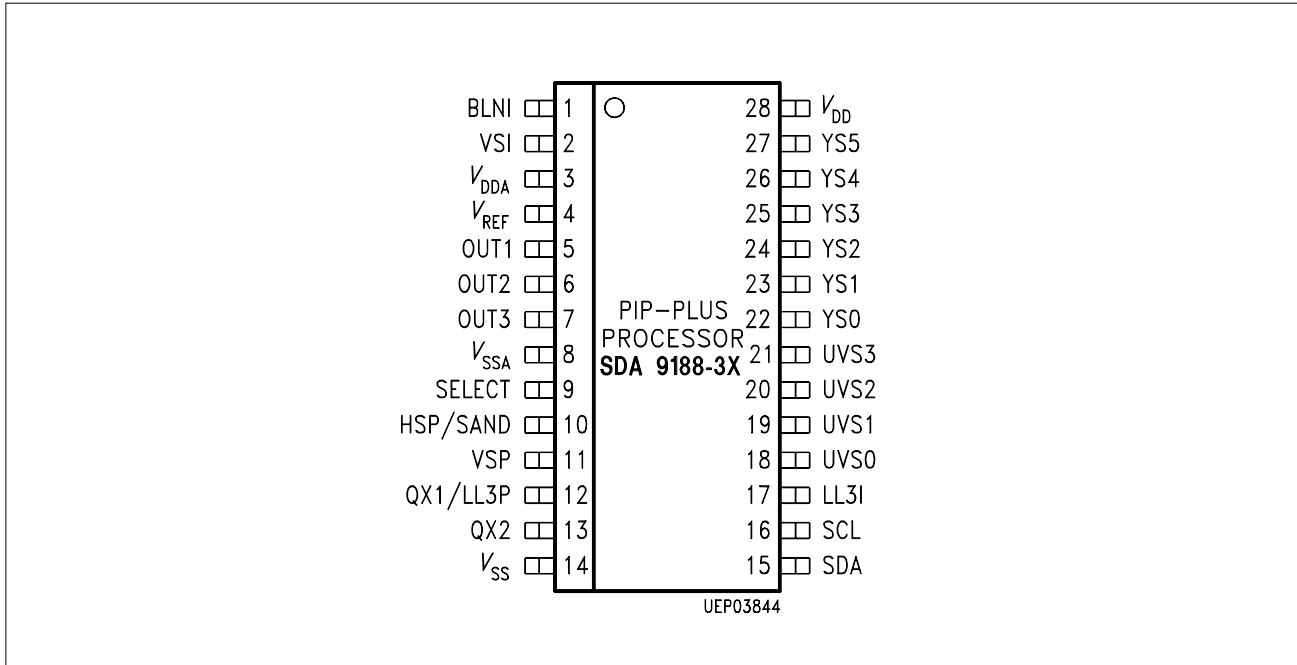
Synchronization with the parent channel is performed via the horizontal and vertical sync signals HSP/SAND and VSP. The clock frequency is 13.5 MHz (LL3P) without standard conversion and 27 MHz (LL1.5P) with standard conversion (100/120 Hz). The display clock is generated on chip. Optionally the external clock generator SDA 9086-3 can be used in the same way as with the SDA 9188X.

The horizontal and vertical sync signals BLNI and VSI plus the LL3I clock (13.5 MHz) are used for synchronization with the inset source.

The interface between inset and parent channel is done by the on-chip memory. The memory write access is controlled by the inset clock and the read access is controlled by the parent clock.

The SELECT output signal inserts the inset picture into the parent picture driving an external analog switch, e.g. the TDA 4685. All operation modes of the SDA 9188-3X can be controlled via the I<sup>2</sup>C bus. Nine registers can be used.

## Pin Configuration (top view)



## Pin Definitions and Functions

| Pin No. | Symbol         | Function  | Descriptions   |
|---------|----------------|---|--|
| 1       | BLNI           | Blanking inset                                    | Inset line synchronization   |
| 2       | VSI            | Vertical synchronous inset                        | Inset field synchronization  |
| 3       | $V_{DDA}$      | Analog supply                                     | $V_{DD}$ -power supply for D/A converter and PLL                               |
| 4       | $V_{REF}$      | Reference voltage                                 | External resistor can be used for generation of the internal reference voltage |
| 5-7     | OUT1-OUT3      | Analog R, G, B, Y, -U, -V-outputs                 | Analog RGB or YUV outputs  |
| 8       | $V_{SSA}$      | Analog ground                                     | Ground for D/A converter and PLL   |
| 9       | SELECT         | SELECT  | Valid signals at OUT1-OUT3   |
| 10      | HSP/SAND       | Horizontal synchronous/Sandcastle parent          | Parent line synchronization  |
| 11      | VSP            | Vertical synchronous parent                       | Parent field synchronization   |
| 12      | LL3P/QX1       | Line locked clock parent/Output of the oscillator | Parent system clock or to be connected to the crystal                          |
| 13      | QX2            | Input of the oscillator                           | To be connected to the crystal   |
| 14      | $V_{SS}$       | Digital ground                                    | Ground   |
| 15      | SDA            | Serial Data                                       | I <sup>2</sup> C Data  |
| 16      | SCL            | Serial Clock                                      | I <sup>2</sup> C Clock   |
| 17      | LL3I           | Line locked clock inset                           | Inset system clock   |
| 18-27   | UV0-UV3, Y0-Y5 | UV, Y-Data  | Digital YUV input data   |
| 28      | $V_{DD}$       | Digital supply                                    | $V_{DD}$ supply  |



**Circuit Description**

**Data Transfer**

The digital data are transferred under the control of LL3I, BLNI and VSI on pins YS0-YS5 and UVS0-UVS3. The decimated data are stored automatically. Either R, G, B, or Y, -U, -V analog signals are available at the outputs OUT1-OUT3. The validity of the signals is identified by SELECT = 1. In a digital system environment the input is controlled by LL3P, HSP and VSP.

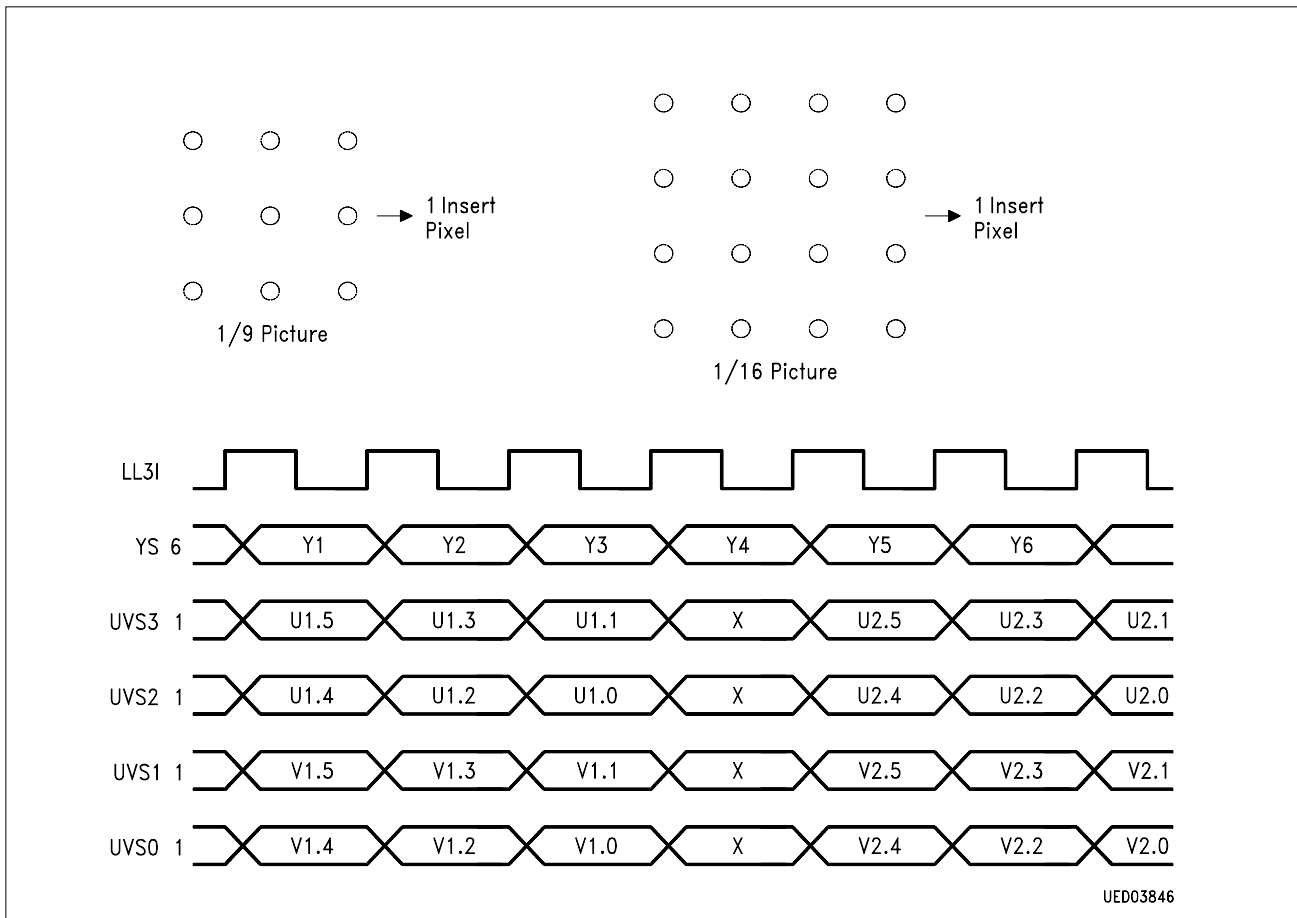
**Inset Data Reduction**

The data rate at the inputs YS0-YS5, UVS0-UVS3 is 13.5 MHz in multiplexed format, **see figure 1**.

In order to reduce the quantity of data which have to be stored and to prevent artifacts in the inset picture, nine pixels are processed into one inset pixel for a 1/9 picture. For the 1/16 picture 16 pixels are processed into one inset pixel.

This is done by horizontal and vertical averaging of pixels:

The characteristic of decimation for the luminance signal is 1-1-1 for 1/9- and 1-1-1-1 for 1/16 picture. Chrominance signal: 1-2-1 for 1/9 and 1-1-1-1 for 1/16 picture.



**Figure 1**  
**Input Data Format**

During the decimation process the following parts of the original picture are processed:

- |    |                                |                                   |
|----|--------------------------------|-----------------------------------|
| 1. | DECHOR/DECVER = 0(1/9-Picture) |                                   |
|    | during 625 line mode:          | Line 36 ... 302; Pixel 13 ... 636 |
|    | during 525 line mode:          | Line 26 ... 256; Pixel 13 ... 636 |
| 2. | SIZE = 1(1/16-Picture):        |                                   |
|    | during 625 line mode:          | Line 36 ... 303; Pixel 17 ... 640 |
|    | during 525 line mode:          | Line 26 ... 257; Pixel 17 ... 640 |

### Temporary Storage of Inset Picture

The PIP memory has a capacity of 169.812 bits. The memory organisation is  $89 \times 212 \times 9$  bits.

Data are written in with the inset and read out with the parent clock frequency.

For standard video signals with 50 or 60 Hz a full frame display is possible. To assure a correct display of the two fields, the control of the memory is done dependently of the field and the phase relation of the Inset and Parent channel. Frame mode display is only possible for standard 50 Hz/60 Hz video signals. Certain VCR-functions (e.g. fast forward-mode), non interlaced signals and 50 Hz/60 Hz mixed-mode would cause unacceptable picture distortions. Under these conditions the SDA 9188-3X switches automatically into field mode display.

Also freezed pictures can only be displayed in the field-mode.

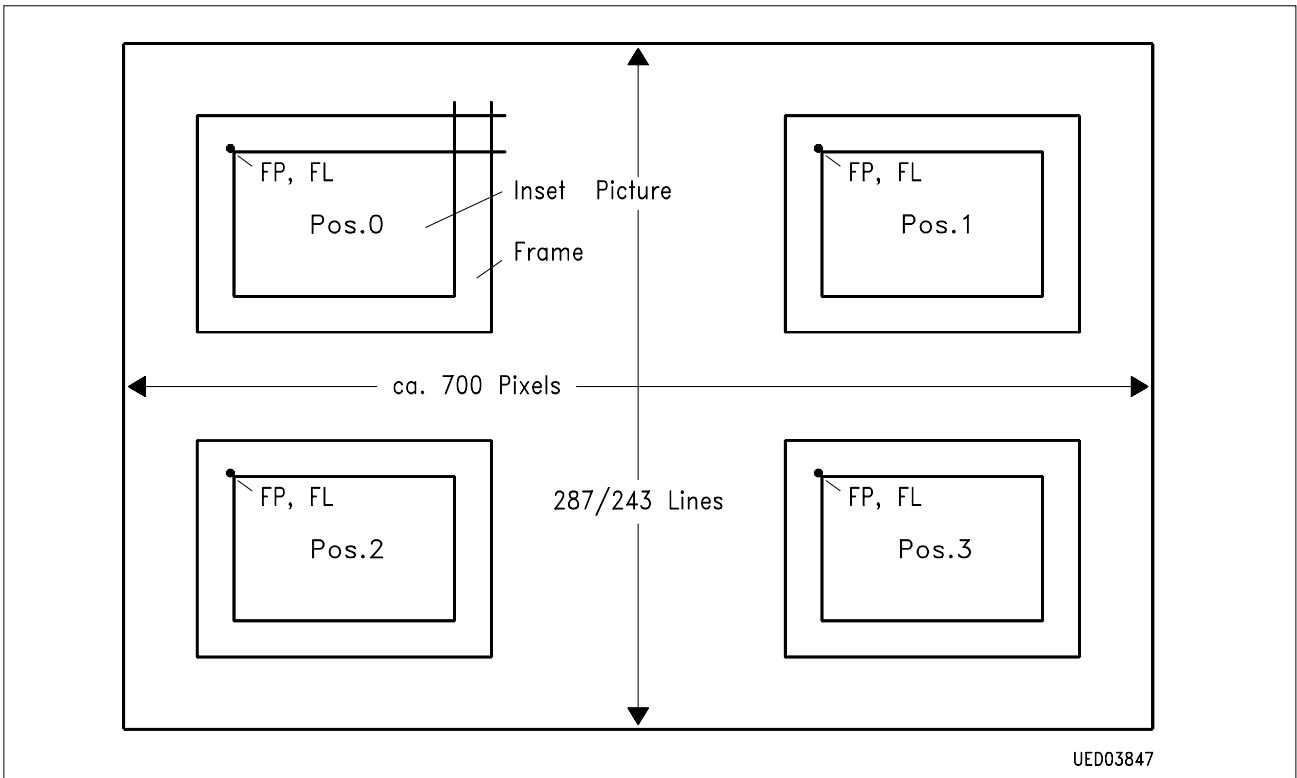
### Output of Data in Parent Window

The four corners of the parent picture are foreseen as positions for inserting the inset picture. To enable compatibility to different system configurations, readout from memory can be shifted horizontally in 63 steps by max. 252 LL3P cycles and vertically in 15 steps by max. 30 lines in the parent field setting the control bits RDH and RDV in control register 2 and 3.

The coordinates BRP, BRL of the normal location of all four insertion positions are given in **table 3** for RDH = RDV = 8.

The SELECT signal goes high during the display of the inset picture. Outside of the inset picture SELECT signal is low and the analog outputs OUT1-OUT3 provide the black level. The external wiring can produce a delay between the SELECT signal and the analog outputs. This delay can be compensated by bits SD0-SD2 in register 2 via the I<sup>2</sup>C bus.

A frame with one of eight colors can be inserted using control bits FRON, COL0-2. The width of the frame is fixed by FRWV at three or two lines and by FRWH at six or four pixels. The brightness can be adjusted in 16 stages.



**Figure 2**  
**Insertion Positions of Inset Picture**

**Table 3**  
**Display of Inset Picture**

| Position | TV Standard (Parent)<br>(Frame Line Number) | Picture<br>Size | Location of Top Left Corner Point<br>for FRWH = 1, FRWV = 1 |     |               |
|----------|---|-----------------|---|-----|---------------|
|          |   |                 | TV Line<br>(FL)   |     | Pixel<br>(FP) |
|          |   |                 | NINT  | INT |               |
| 0        | 625   | X               | 57  | 29  | 54            |
| 0        | 525   | X               | 41  | 21  | 54            |
| 1        | 625   | 1/9             | 57  | 29  | 448           |
| 1        | 525   | 1/9             | 41  | 21  | 448           |
| 1        | 625   | 1/16            | 57  | 29  | 502           |
| 1        | 525   | 1/16            | 41  | 21  | 502           |
| 2        | 625   | 1/9             | 365   | 183 | 54            |
| 2        | 525 *                                       | 1/9             | 293   | 147 | 54            |
| 2        | 625   | 1/16            | 409   | 205 | 54            |
| 2        | 525 *                                       | 1/16            | 333   | 167 | 54            |



| Position | TV Standard (Parent)<br>(Frame Line Number) | Picture Size | Location of Top Left Corner Point<br>for FRWH = 1, FRWV = 1 |     |            |
|----------|---|--------------|---|-----|------------|
|          |   |              | TV Line (FL)  |     | Pixel (FP) |
|          |   |              | NINT  | INT |            |
| 3        | 625   | 1/9          | 365   | 183 | 448        |
| 3        | 525 *                                       | 1/9          | 293   | 147 | 448        |
| 3        | 625   | 1/16         | 409   | 205 | 502        |
| 3        | 525 *                                       | 1/16         | 333   | 167 | 502        |

Pixel data related to positive HSP edge

Line data related to positive VSP edge

\* If the System is in the 50/60 Hz mixed mode RDV in Register 2 is forced to the logical "0" state.

If FRWV is set to "0" during the INT Mode the inset position will be shifted by one line.

The width of the borderframe is depending on the programming of the bits FRWV and FRWH (in Register 5) 3 or 2 lines and 6 or 4 pixels.

The pixels and line number of the inset picture depend on the standard of the inset channel and on the selected picture size.

**Table 1**  
**Inset Picture Size**

| Picture Size | TV Standard (Inset)<br>(Frame Line Number) | Pixel Number P |    |    | Line Number L |
|--------------|--|----------------|----|----|---------------|
|              |  | Y              | U  | V  |               |
| 1/9          | 625  | 212            | 53 | 53 | 88            |
| 1/9          | 525  | 212            | 53 | 53 | 76            |
| 1/16         | 625  | 160            | 40 | 40 | 66            |
| 1/16         | 525  | 160            | 40 | 40 | 57            |

### Interpolation of Chrominance Data Rate to Luminance Data Rate

To avoid chrominance artifacts after D/A conversion and for digital RGB conversion, the data rate of the chrominance signals is quadrupled in order to match the luminance data rate. This is done by repeating the chrominance data twice followed by low-pass filtering.

## RGB, Y, U, V Outputs

A digital RGB matrix converts the Y, U, V data in R, G, B data.

The equation of the implemented RGB Matrix are:

$$R = Y + 0.75 V$$

$$G = Y - 0.375 V - 0.1875 U$$

$$B = Y + U$$

For a signal with 100 % white and 75 % color saturation the amplitudes of the analog input signals have to be set according the following relation:

$$Y / U / V = 0.72 / 0.95 / 1$$

By means of an internal switch at the output of the RGB matrix it is possible to by-pass the matrix with the digital data for Y, U and V and feed them directly into the D/A converters. During this operation mode the chrominance data U and V will be inverted.

## D/A Conversion

SDA 9188-3X includes three 6-bits D/A converters. Each D/A converter delivers a current through an external resistor that is to be connected between OUT1-OUT3 and  $V_{SSA}$ . The resistor value determines the output voltages (**see application circuit**). The assignment of outputs OUT1-OUT3 to R, G, B and Y, U, V is shown in **table 5**. It is possible to change the output voltage via I<sup>2</sup>C bus **Register 4**.

The tolerances of the output voltages can be reduced significantly if the resistor at  $V_{REF}$  is replaced by means of a constant current source.

**Table 5**  
**Assignment of Output Signals to OUT1-OUT3**

| Output | RGB | YUV |
|--------|-----|-----|
| OUT1   | R   | - V |
| OUT2   | G   | Y   |
| OUT3   | B   | - U |

## Borderframe

The width of the border frame can be adjusted in two steps, the intensity of the frame can be set in 16 steps via the I<sup>2</sup>C bus.

**I<sup>2</sup>C BUS**

**Organization of I<sup>2</sup>C Bus Registers**

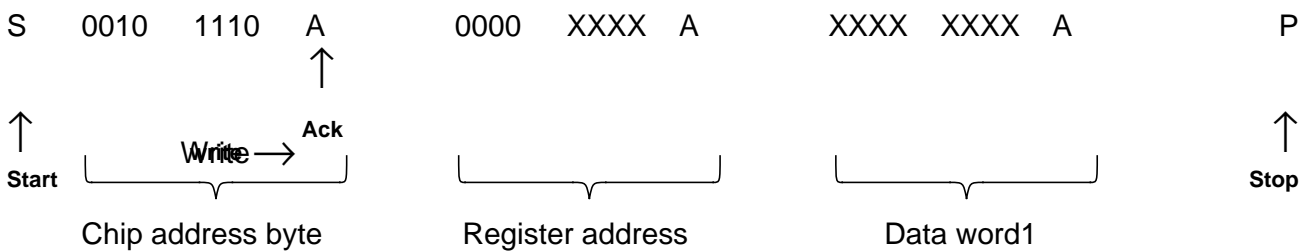
SDA 9188-3X has the device address

$$00101110 = 2E_H$$

Applying the supply voltage  $V_{DD}$  produces a power-up reset. The bus lines SDA and SCL are enabled. All bits in the registers except bit PL27 (D3 in Register 0) are set to 0. Bit PL27 is set to 1.

The I<sup>2</sup>C bus interface works as a slave receiver and only functions if the inset clock LL3I is available.

**Write Operation**



After writing a byte into any register, the register address is automatically incremented for the write access to the next register.

The following table shows the functions that can be set on the I<sup>2</sup>C bus and define the data bytes. Not used data bits have to be written with “0” . Before PON = 1 all other bits have to be defined in relation to the used hardware.

| Function  | SUB-address | D7        | D6     | D5    | D4       | D3       | D2       | D1       | D0      |
|-----------|-------------|-----------|--------|-------|----------|----------|----------|----------|---------|
|           |             | CONTROL 0 | 00     | 0     | 0        | STILL    | SIZE     | PL27     | NINT    |
| CONTROL 1 | 01          | 0         | 0      | 0     | FRY      | COL2     | COL1     | COL0     | FRON    |
| CONTROL 2 | 02          | 0         | SD2    | SD1   | SD0      | RDV 3    | RDV 2    | RDV 1    | RDV 0   |
| CONTROL 3 | 03          | POS 1     | POS 0  | RDH 5 | RDH 4    | RDH 3    | RDH 2    | RDH 1    | RDH 0   |
| CONTROL 4 | 04          | CON0      | CON1   | CON2  | CON3     | 0        | SOP      | PLLOFF   | HSP5    |
| CONTROL 5 | 05          | DECVER    | DECHOR | FRWV  | FRWH     | PMOD1    | PMOD0    | IMOD1    | IMOD0   |
| CONTROL 6 | 06          | FRAME     | STATI  | VSIIS | VSIDEL4  | VSIDEL3  | VSIDEL2  | VSIDEL1  | VSIDEL0 |
| CONTROL 7 | 07          | AMSEC     | STATP  | VSPIS | VSPDEL4  | VSPDEL3  | VSPDEL2  | VSPDEL1  | VSPDEL0 |
| CONTROL 8 | 08          | 0         | 0      | 0     | FRYEN    | FRY5     | FRY4     | FRY3     | FRY2    |
| CONTROL 9 | 09          | 0         | PLLTC  | SOS   | VCOSSEL3 | VCOSSEL2 | VCOSSEL1 | VCOSSEL0 | 0       |

**Table 6: I<sup>2</sup>C Bus Register**

The bits are numbered in the reverse order to the data stream of the I<sup>2</sup>C bus.

If the control software addresses the internal register number 8 or 9 there is no longer any software compatibility to the devices SDA 9088-2 and SDA 9089X. This is caused by the fact that in these devices register 0 and 1 can also be accessed via the subaddress 08 and 09.

## Register 0 (Address 00<sub>H</sub>)

| Bit    | Function                                | Name  | Remarks  |
|--------|---|-------|--|
| d0     | 0 = PIP OFF<br>1 = PIP ON               | PON   | If d0 = 0, no SELECT generated<br>PON = 1 should be set after the initialization         |
| d1     | 0 = Y, -U, -V<br>1 = RGB                | OUT   | Output format  |
| d2     | 0 = Normal picture<br>1 = Double scan   | NINT  | Reproduction mode  |
| d3     | 0 = 13.5 MHz PLL<br>1 = 27 MHz PLL      | PL27  | Switching of the clock prescaler of the PLL for<br>50/60 Hz or 100/120 Hz operation mode |
| d4     | 0 = 1/9<br>1 = 1/16                     | SIZE  | Picture size; if d4 = 0 the picture size depends on<br>DECHOR, DECVAR in Register 5      |
| d5     | 0 = normal picture<br>1 = still picture | STILL | Still/moving picture   |
| d6, d7 | not assigned                            |       |  |

## Register 1 (Address 01<sub>H</sub>)

| Bit   | Function   | Name          | Remarks                 |
|-------|--|---------------|-------------------------|
| d0    | 0 = without frame<br>1 = with frame  | FRON          | FRON                    |
| d1-d3 | frame color<br><br>d3 d2 d1<br>0 0 0 = blue<br>0 0 1 = violet<br>0 1 0 = green<br>0 1 1 = white<br>1 0 0 = red<br>1 0 1 = yellow<br>1 1 0 = orange<br>1 1 1 = cyan   | COL0-<br>COL2 |                         |
| d4-d7 | Intensity of the border frame<br><br>1 = dark frame for white, yellow, orange and cyan<br>bright frame for blue, violet, green and red<br>0 = bright frame for white, yellow, orange and<br>cyan<br>dark frame for blue, violet, green and red | FRY           | Only valid if FRYEN = 0 |
| d7-d5 | without function   |               |                         |

## Register 2 (Address 02<sub>H</sub>)

| Bit   | Function  | Name          | Remarks   |
|-------|---|---------------|---|
| d0-d3 | Vertical read delay<br>in HSP period<br><br>d3 d2 d1 d0<br>0 0 0 0 = 0<br>0 0 0 1 = 2<br>0 0 1 0 = 4<br>:<br>1 1 0 1 = 26<br>1 1 1 0 = 28<br>1 1 1 1 = 30 | RDV0-<br>RDV3 | Increment in two HSP<br>periods.<br>If POS1 = 1 is selected, i.e.<br>525-lines parent picture and<br>625-lines inset picture are displayed,<br>then RDV bits are not evaluated. |
| d4-d6 | SELECT delay<br>in<br>LL3P period<br><br>d6 d5 d4<br>0 0 0 = 0<br>0 0 1 = 1<br>0 1 0 = 2<br>0 1 1 = 3<br>1 0 0 = 4<br>1 0 1 = 5<br>1 1 0 = 6<br>1 1 1 = 7 | SD0-<br>SD2   |   |
| d7    | without function  |               |   |

### Register 3 (Address 03<sub>H</sub>)

| Bit    | Function  | Name          | Remarks                        |
|--------|---|---------------|--------------------------------|
| d0-d5  | Horizontal read delay<br>in LL3P period<br><br>d5 d4 d3 d2 d1 d0<br>0 0 0 0 0 0 = 0<br>0 0 0 0 0 1 = 4<br>0 0 0 0 1 0 = 8<br>:<br>1 1 1 1 0 1 = 244<br>1 1 1 1 1 0 = 248<br>1 1 1 1 1 1 = 252 | RDH0-<br>RDH5 | Increment in four LL3P periods |
| d6, d7 | Inset picture location<br><br>d7 d6<br>0 0 top left<br>0 1 top right<br>1 0 down left<br>1 1 down right   | POS0-<br>POS1 |                                |



## Register 5 (Address 05<sub>H</sub>)

| Bit    | Function   | Name     | Remarks  |
|--------|--|----------|--|
| d1, d0 | 00 = Automatic TV standard recognition<br>01 = 50 Hz<br>10 = 60 Hz<br>11 = Freeze the current mode | IMOD0, 1 | For multistandard applicat.<br>Fixed setting<br>Fixed setting<br>Undisturbed switching during the change of the received station |
| d3, d2 | same like d1, d0   | PMOD0, 1 | as above but for the parent channel  |
| d4     | 0 = Frame width horizontal: 6 Pixel<br>1 = Frame width horizontal: 4 Pixel                         | FRWH     | Separated setting of the frame width and height is possible i.e. for 16:9 operation  |
| d5     | 0 = Frame width vertical: 3 lines<br>1 = Frame width vertical: 2 lines                             | FRWV     | Separated setting of the frame width and height is possible i.e. for 16:9 operation  |
| d6     | 0 = Horizontal decimation 3:1<br>1 = Horizontal decimation 4:1                                     | DECHOR   | Separated setting of the picture width and height is possible i.e. for 16:9 operation, but only if Size = 0 in Register 0        |
| d7     | 0 = Vertical decimation 3:1<br>1 = Vertical decimation 4:1   | DECVER   | Separated setting of the picture width and height is possible i.e. for 16:9 operation, but only if Size = 0 in Register 0        |



## Register 6 (Address 06<sub>H</sub>)

| Bit   | Function   | Name   | Remarks  |
|-------|--|--------|--|
| d4:d0 | Setting the delay of VSI<br>(see test circuit 6)                                       | VSIDEL | Setting is possible in steps of 2,37 $\mu$ s (see measurement circuit 6)   |
| d5    | 0 = Vertical noise reduction inactive<br>1 = Vertical noise reduction active           | VSIS   | Noise reduction of the VSI pulse (should be set to '1' under normal conditions.)   |
| d6    | 0 = Check for correct TV standard inactive<br>1 = Check for correct TV standard active | STATI  | If the check is active a full frame display is only possible if the number of lines is exactly according the TV standard:<br>312.5 (50 Hz)<br>262.5 (60 Hz)                      |
| d7    | 0 = Field display<br>1 = Frame display   | FRAME  | Only active if the line number and the interlace mode are equal for both inset and parent signal.<br>If the display mode is 100/120 Hz or progressive scan d7 has to be set to 0 |

### Register 7 (Address 07<sub>H</sub>)

| Bit   | Function   | Name   | Remarks   |
|-------|--|--------|---|
| d4:d0 | Delay of the VSP pulse   | VSPDEL | Setting is possible in steps of 2,37 $\mu$ s (50 Hz or 1,185 $\mu$ s 100 Hz) (see measuring circuit 6)  |
| d5    | 0 = Vertical noise reduction OFF<br>1 = Vertical noise reduction ON                    | VSPIS  | Noise reduction for the vertical pulse of the parent channel (should be set to '1' under normal conditions).  |
| d6    | 0 = Check for correct TV standard inactive<br>1 = Check for correct TV standard active | STATP  | If the check for the correct TV standard is active a full frame display is only possible if the number of lines is exactly according the TV standard:<br>312.5 (50 Hz)<br>262.5 (60 Hz) |
| d7    | 0 = PAL/NTSC<br>1 = SECAM  | AMSEC  | Doubling of the gain if a sufficient SECAM decoder without delay line is used   |

### Register 8 (Address 08<sub>H</sub>)

| Bit   | Function  | Name   | Remarks  |
|-------|---|--------|--|
| d3:d0 | 0000 = min. brightness of the border frame<br>1111 = max. brightness of the border frame                                      | FRY5:2 | Setting only valid if the bit d4 is set to '1' |
| d4    | 0 = brightness of the border frame can be selected by FRY<br><br>1 = brightness of the border frame can be selected by FRY5:2 | FRYEN  |  |
| d7:d5 | not used to be set to "0".  |        |  |

## Register 9 (Address 09<sub>H</sub>)

| Bit       | Function              | Name              | Remarks  |
|-----------|-----------------------|-------------------|--|
| d0        | –                     |                   | Set to '0'   |
| d1 ... d4 | VCO Nominal Frequency | VCOSEL<br>0 ... 3 | Set to '0' under nominal conditions  |
| d5        | Select open Source    | SOS               | If d5 = 1<br>Pulldown-transistor of select output is switched OFF<br>Resistor to ground required |
| d6        | PLL-Time constant     | PLLTC             | 0 = fast time constant<br>1 = slow time constant   |
| d7        | –                     |                   | Set to '0'   |

## Absolute Maximum Ratings

$T_A = 0 \dots 70 \text{ }^\circ\text{C}$  (all voltages are referred to  $V_{SS}$ )

| Parameter           | Symbol           | Limit Values |                | Unit             | Test Condition |
|---------------------|------------------|--------------|----------------|------------------|----------------|
|                     |                  | min.         | max.           |                  |                |
| Supply voltage      | $V_{DD}$         | - 1          | 6              | V                |                |
| Pin voltages        | $V_{IN}$         | - 1          | $V_{DD} + 0.5$ | V                |                |
| Difference between  | $V_{DD}/V_{DDA}$ | - 0.25       | 0.25           | V                |                |
| Ambient temperature | $T_A$            | - 20         | 70             | $^\circ\text{C}$ |                |
| Storage temperature | $T_{stg}$        | - 20         | 125            | $^\circ\text{C}$ |                |
| Power dissipation   | $P_{tot}$        |              | 1              | W                |                |
| Thermal resistance  | $R_{th\ SU}$     |              | 55             | K/W              |                |

## Operating Range

$T_A = 0 \dots 70 \text{ }^\circ\text{C}$

|                     |          |     |     |                  |  |
|---------------------|----------|-----|-----|------------------|--|
| Supply voltage      | $V_{DD}$ | 4.5 | 5.5 | V                |  |
| Ambient temperature | $T_A$    | 0   | 70  | $^\circ\text{C}$ |  |

## Characteristics

$T_A = 0 \dots 70 \text{ }^\circ\text{C}$  (all voltages are referred to  $V_{SS}$ )

| Parameter           | Symbol                | Limit Values |      |      | Unit | Test Condition                                   |
|---------------------|-----------------------|--------------|------|------|------|--|
|                     |                       | min.         | typ. | max. |      |  |
| Supply voltage      | $V_{DD}/V_{DDA}$      | 4.5          | 5    | 5.5  | V    |  |
| Current consumption | digital<br>$I_{DD}$   | 13           | 40   | 120  | mA   | without load<br>LL3I = 13.5 MHz<br>LL3P = 27 MHz |
|                     | analog<br>$I_{DD\ A}$ | 5            | 10   | 18   | mA   |  |

## Inputs

YS0-YS5, UVS0-UVS3

LL3I, BLNI, VSI, LL3P, VSP

|   |              |       |  |          |               |                          |
|---|--------------|-------|--|----------|---------------|--------------------------|
| H-input voltage                               | $V_{IH}$     | 2.3   |  | $V_{DD}$ | V             |                          |
| L-input voltage                               | $V_{IL}$     | - 1.0 |  | 0.8      | V             |                          |
| Input capacitance                             | $C_i$        |       |  | 7        | pF            |                          |
| Input leakage current<br>(not valid for LL3P) | $I_L$        |       |  | 10       | $\mu\text{A}$ | $V_{IH} = 5.5 \text{ V}$ |
| Input leakage current                         | LL3P/<br>QX2 |       |  | 200      | $\mu\text{A}$ | $V_{IH} = V_{DD}$        |

## Characteristics (cont'd)

| Parameter            | Symbol     | Limit Values |      |          | Unit | Test Condition   |
|----------------------|------------|--------------|------|----------|------|--|
|                      |            | min.         | typ. | max.     |      |  |
| <b>Output Select</b> |            |              |      |          |      |  |
| H-output voltage     | $V_{QH}$   | 2.4          |      | $V_{DD}$ | V    | $-I_{QH} = 0.2 \text{ mA}$ ,<br>SOP = 0                        |
|                      | $V_{QH}$   | 1.5          |      | $V_{DD}$ | V    | $-I_{QH} = 4.5 \text{ mA}$ , <sup>2)</sup><br>SOS = 1, SOP = 0 |
| L-output voltage     | $V_{QL}$   | 0            |      | 0.4      | V    | $I_{QH} = 1.6 \text{ mA}$<br>SOP = 0, SOS = 0                  |
| H-output voltage     | $V_{QH}$   |              |      | $V_{DD}$ | V    | SOP = 1  |
| L-output voltage     | $V_{QL}$   | 0            |      | 1        | V    | $I_{QL} = 5 \text{ mA}$ <sup>1)</sup><br>SOP = 1, SOS = 0      |
| Transition period    | $t_r, t_f$ |              |      | 15       | ns   | SOP = 0, SOS = 0<br>$C_1 = 30 \text{ pF}$                      |

<sup>1)</sup> Measuring Circuit 9a

<sup>2)</sup> Measuring Circuit 9b

## Input HSP / SAND

|                       |          |       |  |          |               |  |
|-----------------------|----------|-------|--|----------|---------------|--|
| H-input voltage       | $V_{IH}$ | 2.3   |  | $V_{DD}$ | V             | HSP5 = 1                               |
| L-input voltage       | $V_{IL}$ | - 1.0 |  | 0.8      | V             | HSP5 = 1                               |
| Input capacitance     | $C_1$    |       |  | 7        | pF            |  |
| Input leakage current | $I_L$    | - 10  |  | 10       | $\mu\text{A}$ | $0 \leq V \leq V_{DD} + 0.5 \text{ V}$ |

## Characteristics (cont'd)

| Parameter                       | Symbol     | Limit Values |      |          | Unit    | Test Condition   | Measuring Circuit |
|---------------------------------|------------|--------------|------|----------|---------|------------------|-------------------|
|                                 |            | min.         | nom. | max.     |         |                  |                   |
| <b>Input SCL, In/Output SDA</b> |            |              |      |          |         |                  |                   |
| L-input voltage                 | $V_{IL}$   | - 1          |      | 1.5      | V       |                  |                   |
| H-input voltage                 | $V_{IH}$   | 3            |      | $V_{DD}$ | V       |                  |                   |
| Input leakage current           | $I_L$      |              |      | 10       | $\mu$ A | $V_{IH} = 5,5$ V |                   |
| Input capacitance               | $C_I$      |              |      | 7        | pF      |                  |                   |
| Input frequency                 | $f_{SCL}$  |              |      | 100      | kHz     |                  |                   |
| Transition period               | $t_r, t_f$ |              |      | 2        | $\mu$ s |                  |                   |
| Max. capacitance at bus         | $C_{max}$  |              |      | 400      | pF      |                  |                   |
| Fall time                       | $t_f$      |              |      | 0.2      | $\mu$ s | from 3 V to 1 V  |                   |
| SDA by acknowledge              | $V_{AL}$   | 0            |      | 0.4      | V       | $I_{AL} = 3$ mA  |                   |

## Output OUT1 ... 3 \*

|  |                       |        |        |        |            |                                 |   |
|--|-----------------------|--------|--------|--------|------------|---------------------------------|---|
| Output current   | $I_O$                 | - 1.61 | - 1.79 | - 1.97 | mA         | $V_{DDA} = 5$ V                 | 1 |
| Output voltage Range   | $V_{OH}$              | 0      | 1.0    | 2      | Vpp        | Bits D4 ... D7 of Reg. 4 = 0000 | 1 |
|  |                       |        |        |        |            | $I_{REF} = \text{nom.}$         | 1 |
| Resolution   | $I_{O \text{ quant}}$ |        | 28.4   |        | $\mu$ A    | $V_{DDA} = 5$ V                 | 1 |
| Load resistance  | $R_L$                 | 0      | 560    | 1000   | $\Omega$   |                                 | 1 |
| Output capacitance   | $C_O$                 |        |        | 7      | pF         |                                 | 1 |
| Coupling capacitance   | $C_C$                 |        | 47     |        | nF         |                                 | 1 |
| Reference current  | $I_{REF}$             | - 0.3  | - 0.58 | - 0.8  | mA         |                                 | 1 |
| Time constant  | $t_{const}$           |        |        | 35     | ns         | BW = 4.5 MHz                    | 1 |
| Differential non-linearity **  |                       | - 0.5  |        | 0.5    | LSB        | Range 0 ... 1 V                 |   |
| Maximum difference of output current at the RGB outputs for the same full modulation |                       | - 3    |        | 3      | %          | Bit d1 of Reg. 0 = 1            |   |
| Change of the output currents by changing of bits CON 0-3 in Register 4              | $\Delta I_O$          | 20     |        |        | %          | $R_{REF} = 10$ k $\Omega$       |   |
| Reference resistance   | $R_{REF}$             | 2.7    | 3.9    | 4.7    | k $\Omega$ | Bits D4 ... D7 of Reg. 4 = 0000 |   |

\* The nominal color saturation is achieved in RGB mode by an amplitude ratio of 0.72/0.95/1 for Y/U/V at the inputs.

\*\* of D/A converter

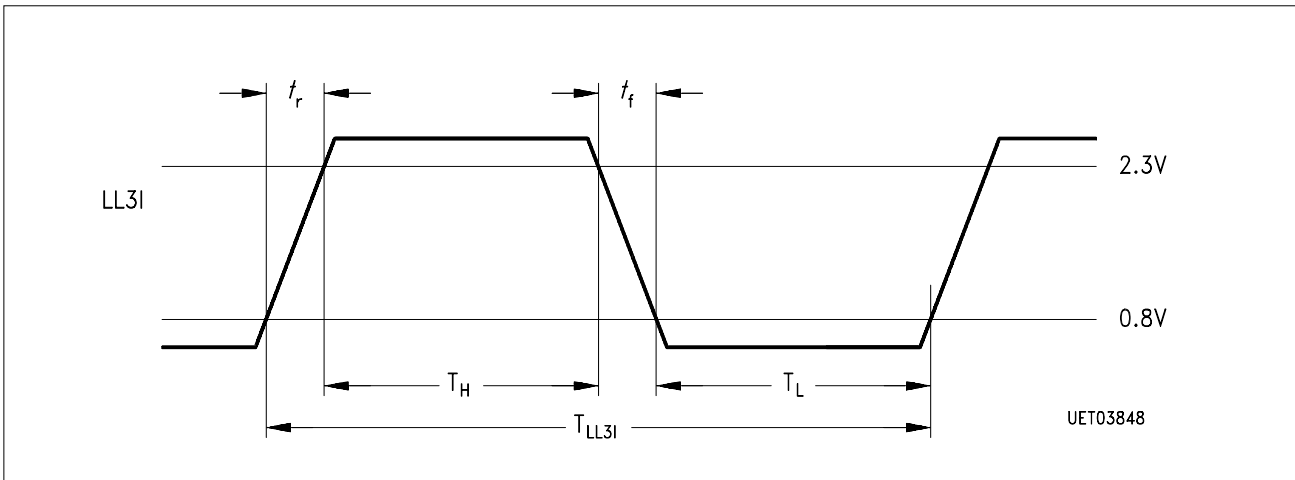
### Internal PLL

Maximum frequency tolerance  $\pm 7\%$   
 (includes variation of horizontal-frequency and resonator tolerance).  
 Attention: Voltage at pins QX1, QX2 must be below the limit values of  
 absolute maximum ratings under all conditions.  
 Minimum input amplitude at pin QX2 =  $1 V_{PP}$ .

### Maximum series resistor of quartz or ceramic resonator.

| Load capacitance<br>at pin 12, 13 | $R_s$       |
|-----------------------------------|-------------|
| 33 pF                             | 10 $\Omega$ |
| 22 pF                             | 20 $\Omega$ |
| 15 pF                             | 30 $\Omega$ |
| 10 pF                             | 40 $\Omega$ |

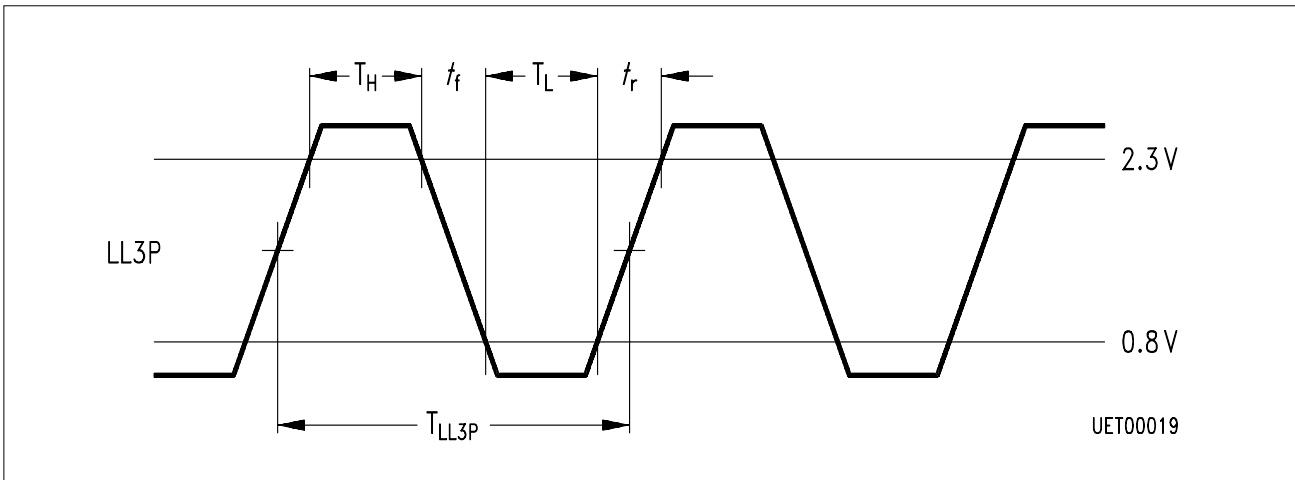
| Horizontal Frequency | min   |            | Conditions   |
|----------------------|-------|------------|--|
|                      |       | max.       |  |
|                      | 14.53 | 16.72 kHz  | Quartz Frequency 20.48 MHz<br>Bit d3 of Reg. 0 = 0 |
|                      | 29.06 | 33.47 kHz  | Bit d3 of Reg. 0 = 1                               |
|                      | 30    | 34.375 kHz | Bit d3 of Reg. 0 = 1<br>Quartz Frequency 21.09 MHz |



Timing Diagram 1

| Parameter   | Symbol     | Limit Values |      |      | Unit |
|-------------|------------|--------------|------|------|------|
|             |            | min.         | typ. | max. |      |
| <b>LL31</b> |            |              |      |      |      |
| Period time | $T_{LL31}$ | 68           | 74   | 80   | ns   |
| Rise time   | $t_r$      |              |      | 5    | ns   |
| Fall time   | $t_f$      |              |      | 4    | ns   |
| Low time    | $T_L$      | 30           |      |      | ns   |
| High time   | $T_H$      | 28           |      |      | ns   |



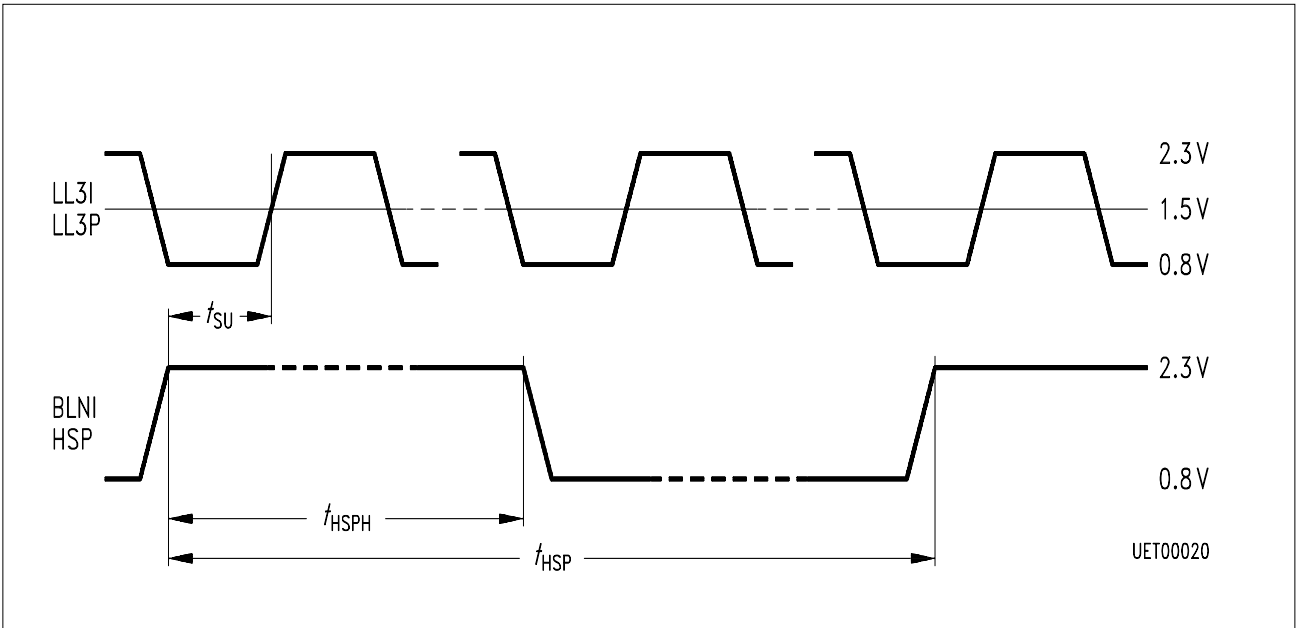


Timing Diagram 2

| Parameter | Symbol | Limit Values |      |      | Unit |
|-----------|--------|--------------|------|------|------|
|           |        | min.         | typ. | max. |      |

**LL3P**

|             |             |    |    |    |    |
|-------------|-------------|----|----|----|----|
| Period time | $T_{LL1.5}$ | 34 | 37 | 40 | ns |
| Rise time   | $t_r$       |    |    | 4  | ns |
| Fall time   | $t_f$       |    |    | 4  | ns |
| Low time    | $T_L$       | 14 |    |    | ns |
| High time   | $T_H$       | 12 |    |    | ns |



Timing Diagram 3

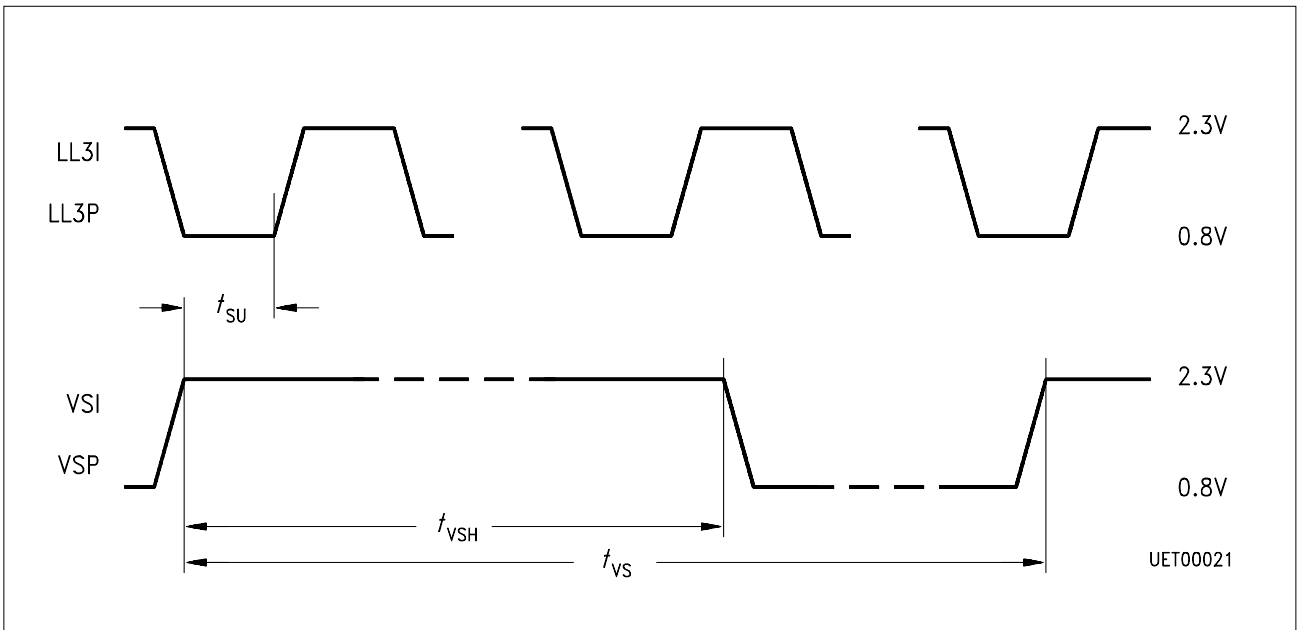
| Parameter | Symbol | Limit Values |      |      | Unit |
|-----------|--------|--------------|------|------|------|
|           |        | min.         | typ. | max. |      |

**BLNI**

|                       |             |     |     |     |            |
|-----------------------|-------------|-----|-----|-----|------------|
| Period time 625 lines | $t_{BLN}$   | 864 | 864 | 864 | $T_{LL3I}$ |
| Period time 525 lines | $t_{BLN}$   | 858 | 864 | 864 | $T_{LL3I}$ |
| High time             | $t_{BLN H}$ | 1   |     | 857 | $T_{LL3I}$ |
| Set-up time           | $t_{SU}$    | 12  |     |     | ns         |

**HSP**

|                       |             |     |     |     |                         |
|-----------------------|-------------|-----|-----|-----|-------------------------|
| Period time 625 lines | $t_{HSP}$   | 864 | 864 | 864 | $T_{LL3P} / T_{LL1.5P}$ |
| Period time 525 lines | $t_{HSP}$   | 858 | 864 | 864 | $T_{LL3P} / T_{LL1.5P}$ |
| High time             | $t_{HSP H}$ | 4   |     | 854 | $T_{LL3P} / T_{LL1.5P}$ |
| Set-up time           | $t_{SU}$    | 12  |     |     | ns                      |



Timing Diagram 4

| Parameter | Symbol | Limit Values |      |      | Unit |
|-----------|--------|--------------|------|------|------|
|           |        | min.         | typ. | max. |      |

**VSI**

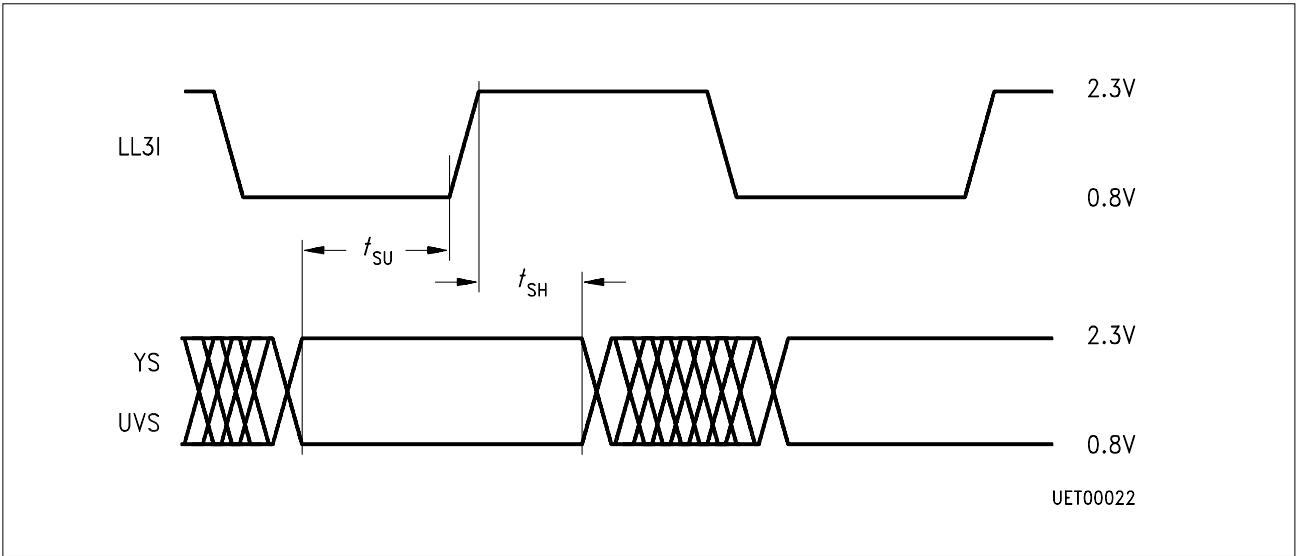
|                       |           |    |       |  |            |
|-----------------------|-----------|----|-------|--|------------|
| Period time 625 lines | $t_{VS}$  |    | 312.5 |  | $T_{BLNI}$ |
| Period time 525 lines | $t_{VS}$  |    | 262.5 |  | $T_{BLNI}$ |
| High time             | $t_{VSH}$ | 1  |       |  | $T_{LL3I}$ |
| Set-up time           | $t_{SU}$  | 15 |       |  | ns         |

**VSP**

|                       |           |    |       |  |            |
|-----------------------|-----------|----|-------|--|------------|
| Period time 625 lines | $t_{VS}$  |    | 312.5 |  | $T_{HSP}$  |
| Period time 525 lines | $t_{VS}$  |    | 262.5 |  | $T_{HSP}$  |
| High time             | $t_{VSH}$ | 1  |       |  | $T_{LL3P}$ |
| Set-up time           | $t_{SU}$  | 15 |       |  | ns         |

Full frame display is possible if the input signal is fully according the TV standard.

The phase relation of the VSI/BLNI or the VSP/HSP signals has to be programmed in a way that the rising edge is neither close to the rising edge of the HS pulse nor in the middle of the TV line. (Test circuit 6).

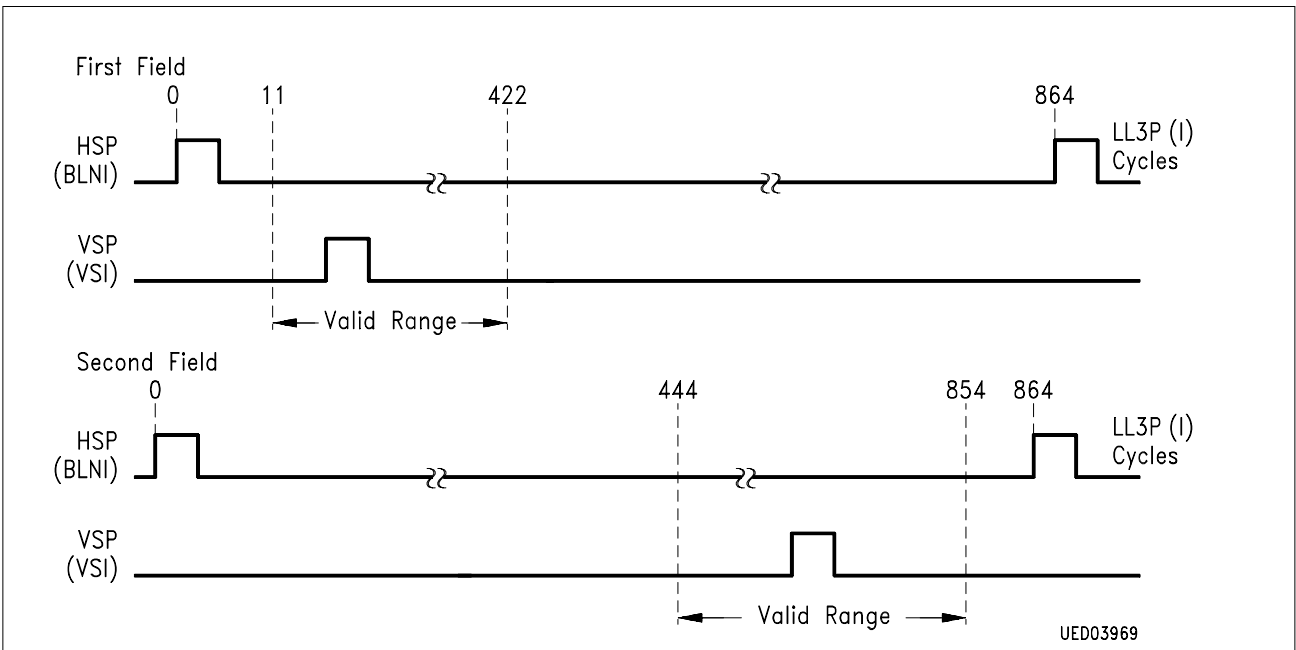


Timing Diagram 5

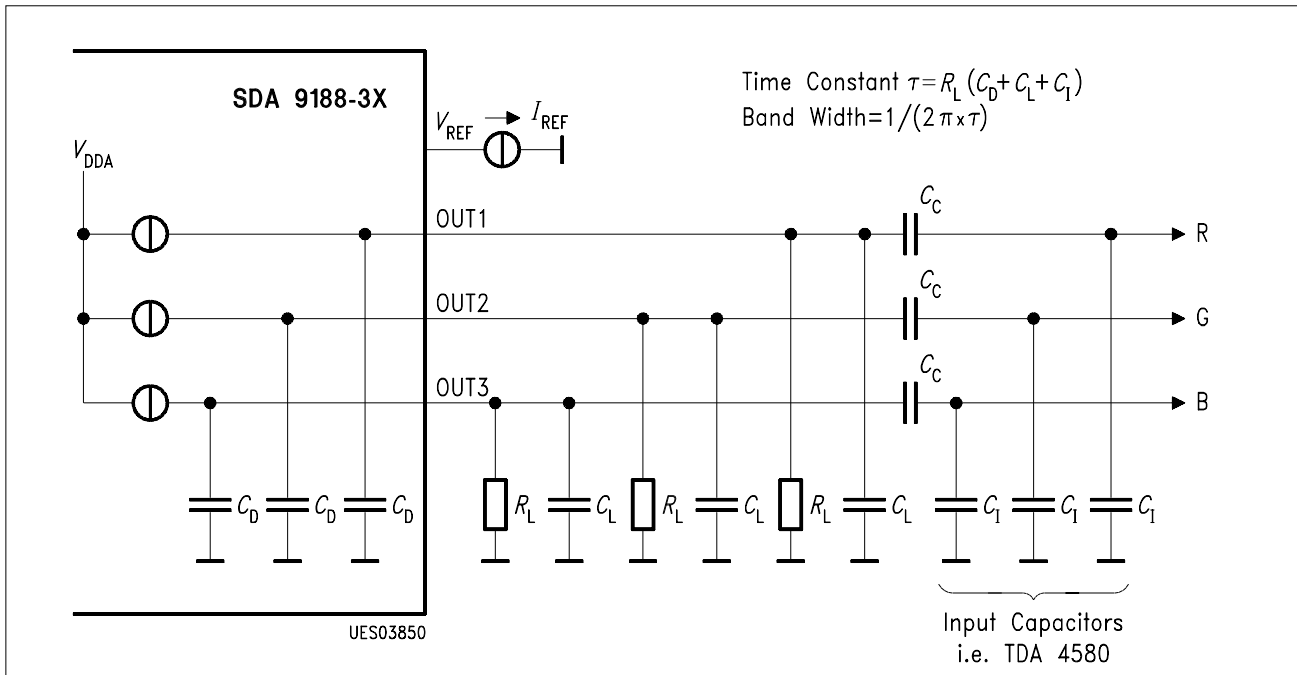
| Parameter | Symbol | Limit Values |      | Unit |
|-----------|--------|--------------|------|------|
|           |        | min.         | max. |      |

**YS, UVS**

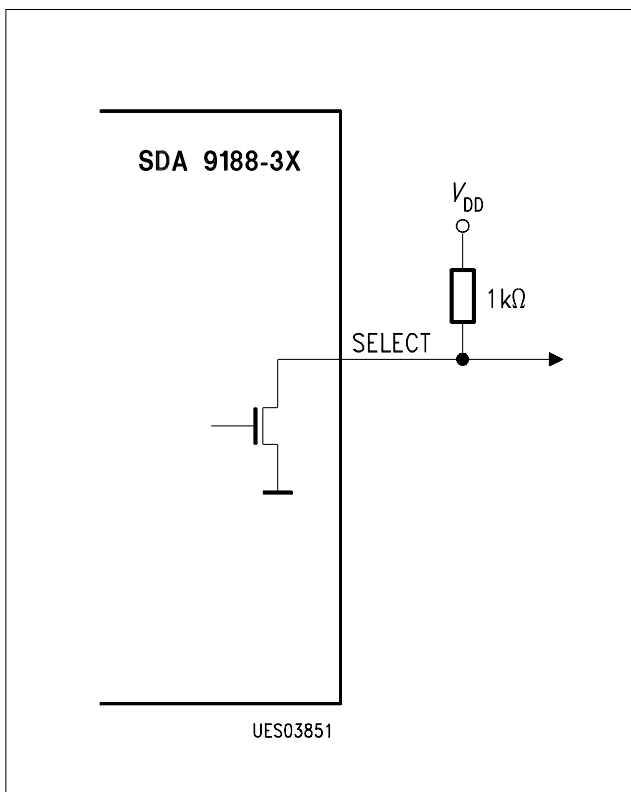
|             |          |    |  |    |
|-------------|----------|----|--|----|
| Set-up time | $t_{SU}$ | 15 |  | ns |
| Hold time   | $t_{SH}$ | 5  |  | ns |



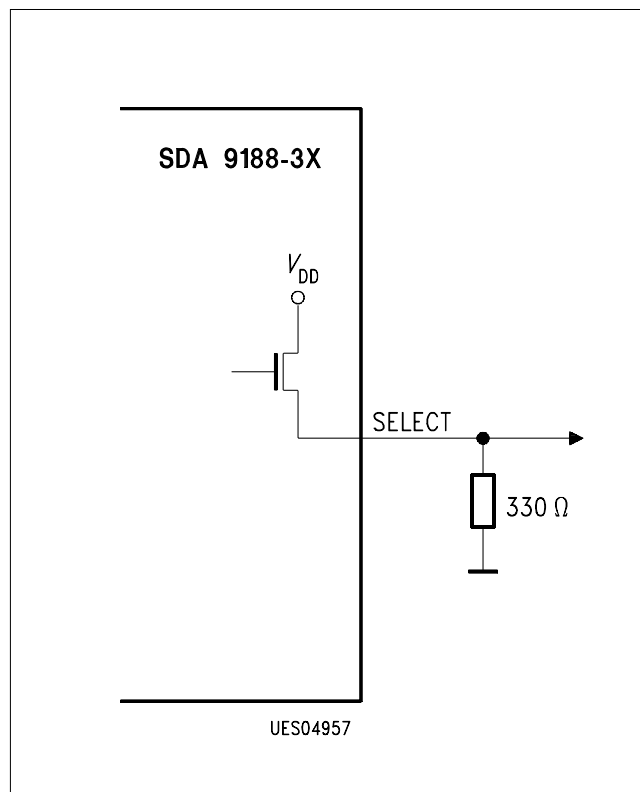
Timing Diagram 6: Allowed phase relation of the VSP/HSP or the VSI/BLNI pulse if the VSPDEL 0:4 or VSIDEL 0:4 = 00000.



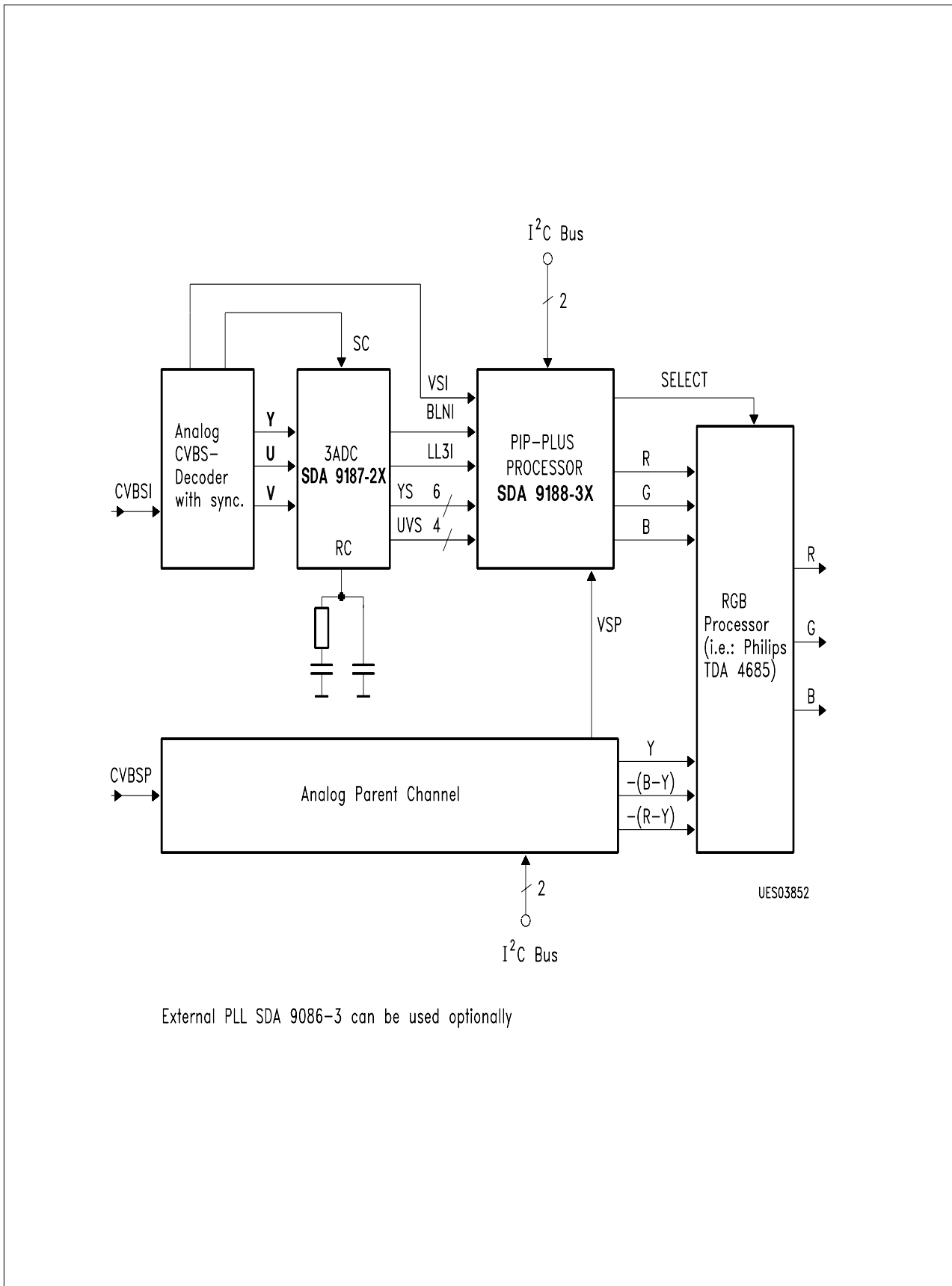
**Measuring Circuit 1**  
**Wiring of D/A Converter Outputs**



**Measuring Circuit 2 a**  
**Wiring of SELECT Output Circuit, if**  
**register 4, bit d2 = 1**  
**register 9, bit d5 = 0**



**Measuring Circuit 2 b**  
**Wiring of SELECT Output, if**  
**register 4, bit d2 = 0**  
**register 9, bit d5 = 1**



External PLL SDA 9086-3 can be used optionally

Application Circuit 1a

