

74ABT125 Quad Buffer with 3-STATE Outputs

General Description

The ABT125 contains four independent non-inverting buffers with 3-STATE outputs.

Features

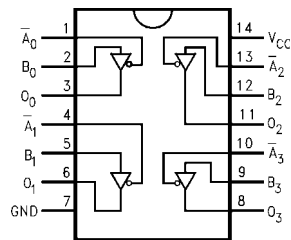
- Non-inverting buffers
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Disable time less than enable time to avoid bus contention

Ordering Code:

Order Number	Package Number	Package Description
74ABT125CSC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ABT125CSJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT125CMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Descriptions
\bar{A}_n, B_n	Inputs
O_n	Outputs

Function Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V _{CC}
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current (Across Comm Operating Range)	-300 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage				V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.5			V	Min	I _{OH} = -3 mA
		2.0			V	Min	I _{OH} = -32 mA
V _{OL}	Output LOW Voltage			0.55	V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current			1	μA	Max	V _{IN} = 2.7V (Note 3)
				1	μA	Max	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-1	μA	Max	V _{IN} = 0.5V (Note 3)
				-1	μA	Max	V _{IN} = 0.0V
I _{ID}	Input Leakage Test				V	0.0	I _{ID} = 1.9 μA, All Other Pin Grounded
I _{OZH}	Output Leakage Current			10	μA	0-5.5V	V _{OUT} = 2.7V; $\overline{OE}_n = 2.0V$
I _{OZL}	Output Leakage Current			-10	μA	0-5.5V	V _{OUT} = 0.5V; $\overline{OE}_n = 2.0V$
I _{OS}	Output Short-Circuit Current			-275	mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			15	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μA	Max	$\overline{OE}_n = V_{CC}$; All Others at V _{CC} or Ground
I _{CC1}	Additional I _{CC} /Input Outputs Enabled Outputs 3-STATE Outputs 3-STATE			1.5	mA	Max	V _I = V _{CC} - 2.1V
				1.5	mA		Enable Input V _I = V _{CC} - 2.1V
				50	μA		Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or Ground
I _{CCD}	Dynamic I _{CC} No Load (Note 3)			0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n = GND$, (Note 4) One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

Note 4: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

AC Electrical Characteristics

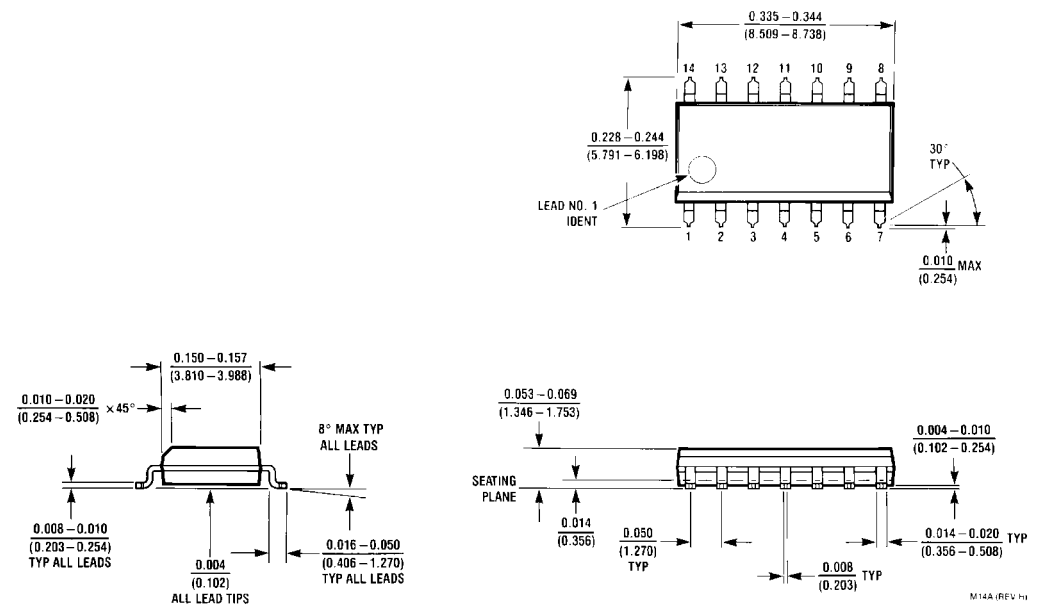
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5\text{V}$ $C_L = 50\text{ pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V} - 5.5\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.0		4.6	1.0	4.6	ns
t_{PHL}	Data to Outputs	1.0		4.9	1.0	4.9	
t_{PZH}	Output Enable	1.0		5.1	1.0	5.1	ns
t_{PZL}	Time	1.0		6.8	1.0	6.8	
t_{PHZ}	Output Disable	1.0		6.2	1.0	6.2	ns
t_{PLZ}	Time	1.0		5.5	1.0	5.5	

Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$
C_{OUT} (Note 5)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$

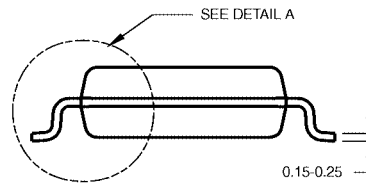
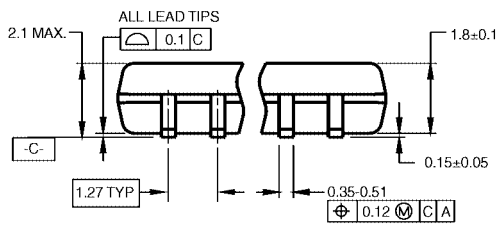
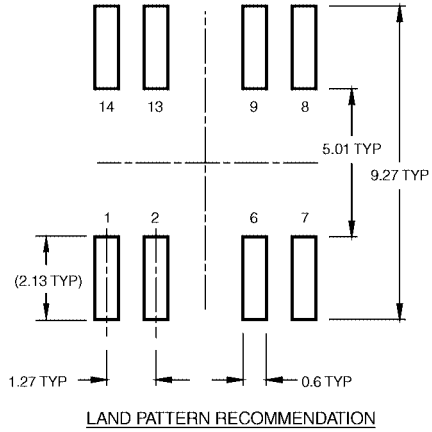
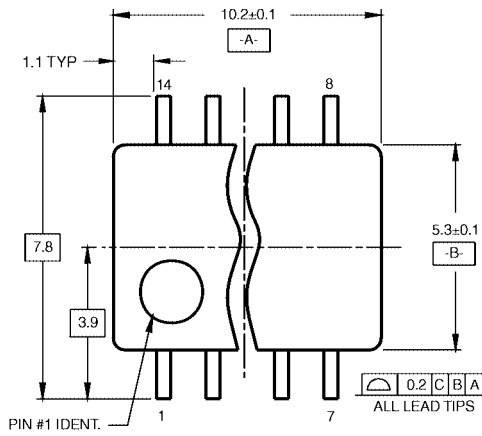
Note 5: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M14A**

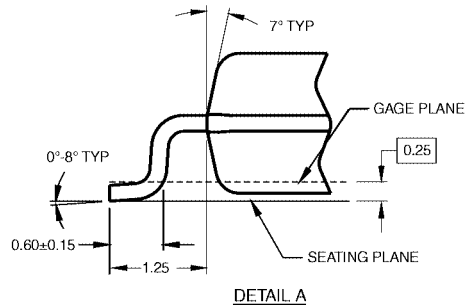
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

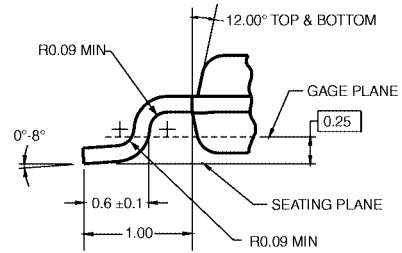
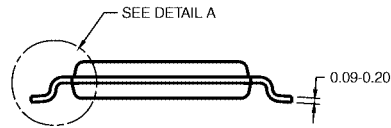
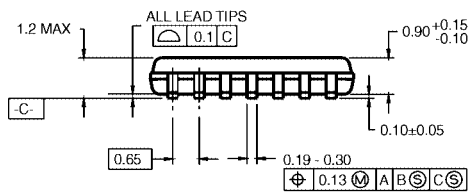
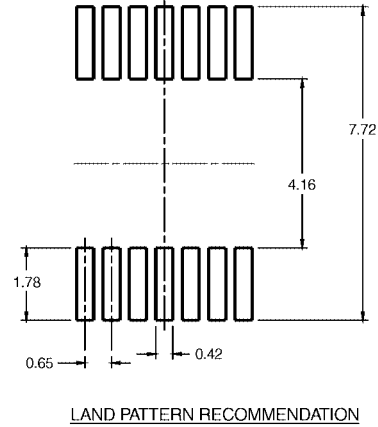
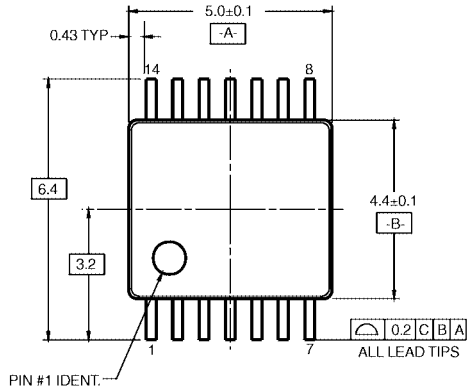
- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



- NOTES:
- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
 - DIMENSIONS ARE IN MILLIMETERS.
 - DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

DETAIL A

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

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