BC846BPDW1T1, BC847BPDW1T1, BC847CPDW1T1, BC848BPDW1T1, BC848CPDW1T1

ON Semiconductor

Formerly a Division of Motorola

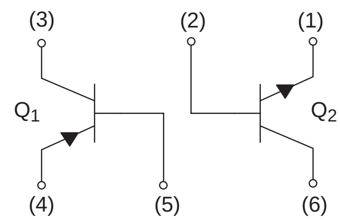
http://onsemi.com

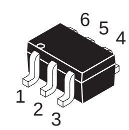
Dual General Purpose Transistors

NPN/PNP Duals

These transistors are designed for general purpose amplifier applications. They are housed in the SOT–363/SC–88 which is designed for low power surface mount applications.

- Device Marking:
  BC846BPDW1T1 = BB
  BC847BPDW1T1 = 13F
  BC847CPDW1T1 = 13G
  BC848BPDW1T1 = 13K
  BC848CPDW1T1 = 13L





SOT–363/SC–88
CASE 419B
STYLE 1

MAXIMUM RATINGS – NPN

Rating	Symbol	BC846	BC847	BC848	Unit
Collector–Emitter Voltage	V_{CEO}	65	45	30	V
Collector–Base Voltage	V_{CBO}	80	50	30	V
Emitter–Base Voltage	V_{EBO}	6.0	6.0	5.0	V
Collector Current — Continuous	I_C	100	100	100	mAdc

MAXIMUM RATINGS – PNP

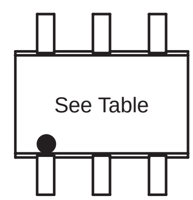
Rating	Symbol	BC846	BC847	BC848	Unit
Collector–Emitter Voltage	V_{CEO}	–65	–45	–30	V
Collector–Base Voltage	V_{CBO}	–80	–50	–30	V
Emitter–Base Voltage	V_{EBO}	–5.0	–5.0	–5.0	V
Collector Current — Continuous	I_C	–100	–100	–100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation Per Device FR–5 Board (1) $T_A = 25°C$ Derate Above 25°C	P_D	380 250 3.0	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	328	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C

1. FR–5 = 1.0 x 0.75 x 0.062 in

DEVICE MARKING



ORDERING INFORMATION

Device	Package	Shipping
BC846BPDW1T1	SOT–363	3000 Units/Reel
BC847BPDW1T1	SOT–363	3000 Units/Reel
BC847CPDW1T1	SOT–363	3000 Units/Reel
BC848BPDW1T1	SOT–363	3000 Units/Reel
BC848CPDW1T1	SOT–363	3000 Units/Reel

ELECTRICAL CHARACTERISTICS (NPN) (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = 10 mA)	BC846 Series BC847 Series BC848 Series	$V_{(BR)CEO}$	65 45 30	— — —	— — —	V
Collector–Emitter Breakdown Voltage (I_C = 10 μA, V_{EB} = 0)	BC846 Series BC847 Series BC848 Series	$V_{(BR)CES}$	80 50 30	— — —	— — —	V
Collector–Base Breakdown Voltage (I_C = 10 μA)	BC846 Series BC847 Series BC848 Series	$V_{(BR)CBO}$	80 50 30	— — —	— — —	V
Emitter–Base Breakdown Voltage (I_E = 1.0 μA)	BC846 Series BC847 Series BC848 Series	$V_{(BR)EBO}$	6.0 6.0 5.0	— — —	— — —	V
Collector Cutoff Current (V_{CB} = 30 V) (V_{CB} = 30 V, T_A = 150°C)		I_{CBO}	— —	— —	15 5.0	nA μA
ON CHARACTERISTICS						
DC Current Gain (I_C = 10 μA, V_{CE} = 5.0 V)	BC846B, BC847B, BC848B BC847C, BC848C	h_{FE}	— —	150 270	— —	—
(I_C = 2.0 mA, V_{CE} = 5.0 V)	BC846B, BC847B, BC848B BC847C, BC848C		200 420	290 520	475 800	
Collector–Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.5 mA) (I_C = 100 mA, I_B = 5.0 mA)		$V_{CE(sat)}$	— —	— —	0.25 0.6	V
Base–Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.5 mA) (I_C = 100 mA, I_B = 5.0 mA)		$V_{BE(sat)}$	— —	0.7 0.9	— —	V
Base–Emitter Voltage (I_C = 2.0 mA, V_{CE} = 5.0 V) (I_C = 10 mA, V_{CE} = 5.0 V)		$V_{BE(on)}$	580 —	660 —	700 770	mV
SMALL–SIGNAL CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = 10 mA, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	100	—	—	MHz
Output Capacitance (V_{CB} = 10 V, f = 1.0 MHz)		C_{obo}	—	—	4.5	pF
Noise Figure (I_C = 0.2 mA, V_{CE} = 5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)	BC846B, BC847B, BC848B BC847C, BC848C	NF	— —	— —	10 4.0	dB

ELECTRICAL CHARACTERISTICS (PNP) (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage		$V_{(BR)CEO}$				V
(I_C = –10 mA)	BC846 Series		–65	—	—	
	BC847 Series		–45	—	—	
	BC848 Series		–30	—	—	
Collector–Emitter Breakdown Voltage		$V_{(BR)CES}$				V
(I_C = –10 μA, V_{EB} = 0)	BC846 Series		–80	—	—	
	BC847 Series		–50	—	—	
	BC848 Series		–30	—	—	
Collector–Base Breakdown Voltage		$V_{(BR)CBO}$				V
(I_C = –10 μA)	BC846 Series		–80	—	—	
	BC847 Series		–50	—	—	
	BC848 Series		–30	—	—	
Emitter–Base Breakdown Voltage		$V_{(BR)EBO}$				V
(I_E = –1.0 μA)	BC846 Series		–5.0	—	—	
	BC847 Series		–5.0	—	—	
	BC848 Series		–5.0	—	—	
Collector Cutoff Current (V_{CB} = –30 V)		I_{CBO}	—	—	–15	nA
(V_{CB} = –30 V, T_A = 150°C)			—	—	–4.0	μA
ON CHARACTERISTICS						
DC Current Gain		h_{FE}				—
(I_C = –10 μA, V_{CE} = –5.0 V)	BC846B, BC847B, BC848B		—	150	—	
	BC847C, BC848C		—	270	—	
(I_C = –2.0 mA, V_{CE} = –5.0 V)	BC846B, BC847B, BC848B		200	290	475	
	BC847C, BC848C		420	520	800	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = –10 mA, I_B = –0.5 mA)			—	—	–0.3	
(I_C = –100 mA, I_B = –5.0 mA)			—	—	–0.65	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				V
(I_C = –10 mA, I_B = –0.5 mA)			—	–0.7	—	
(I_C = –100 mA, I_B = –5.0 mA)			—	–0.9	—	
Base–Emitter On Voltage		$V_{BE(on)}$				V
(I_C = –2.0 mA, V_{CE} = –5.0 V)			–0.6	—	–0.75	
(I_C = –10 mA, V_{CE} = –5.0 V)			—	—	–0.82	
SMALL–SIGNAL CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = –10 mA, V_{CE} = –5.0 Vdc, f = 100 MHz)		f_T	100	—	—	MHz
Output Capacitance (V_{CB} = –10 V, f = 1.0 MHz)		C_{ob}	—	—	4.5	pF
Noise Figure (I_C = –0.2 mA, V_{CE} = –5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)		NF	—	—	10	dB

TYPICAL NPN CHARACTERISTICS

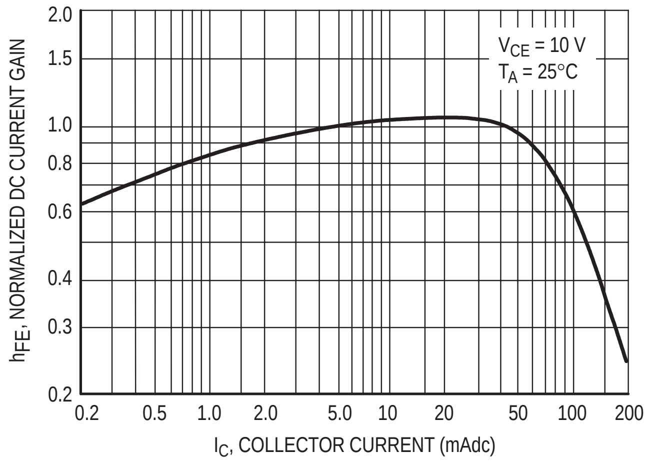


Figure 1. Normalized DC Current Gain

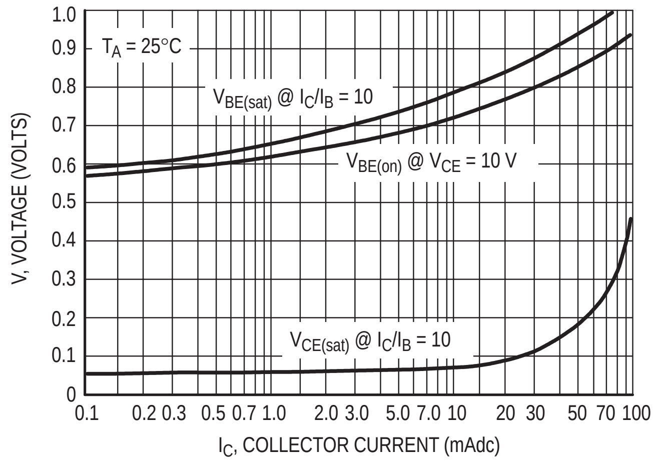


Figure 2. "Saturation" and "On" Voltages

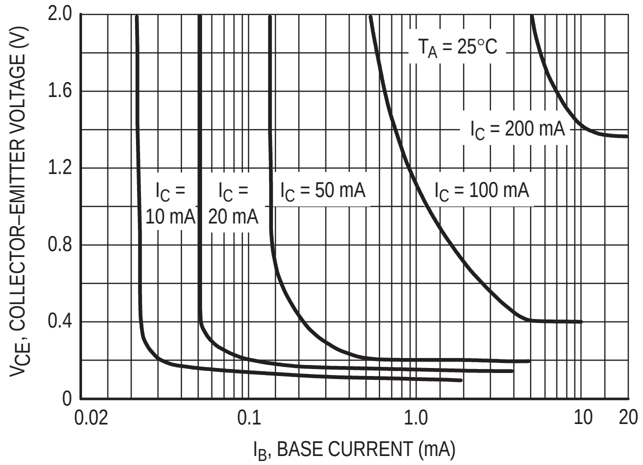


Figure 3. Collector Saturation Region

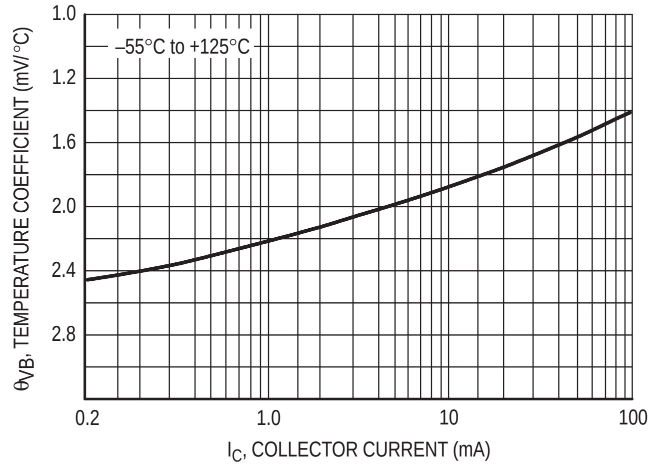


Figure 4. Base–Emitter Temperature Coefficient

TYPICAL NPN CHARACTERISTICS

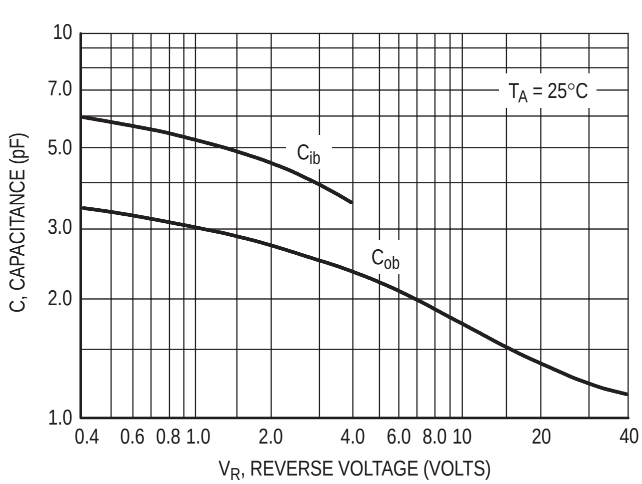


Figure 5. Capacitances

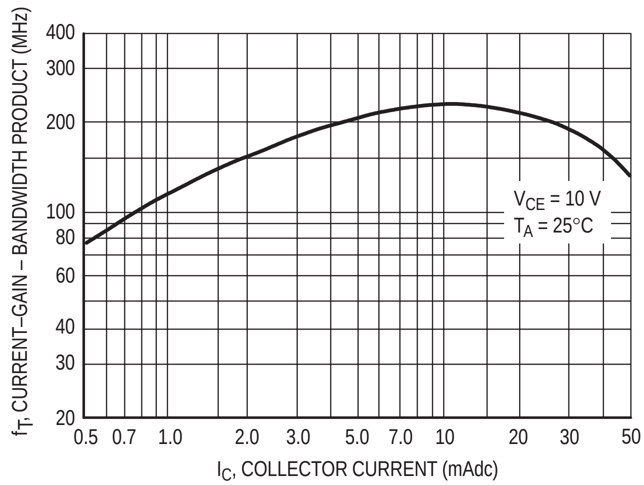


Figure 6. Current−Gain − Bandwidth Product

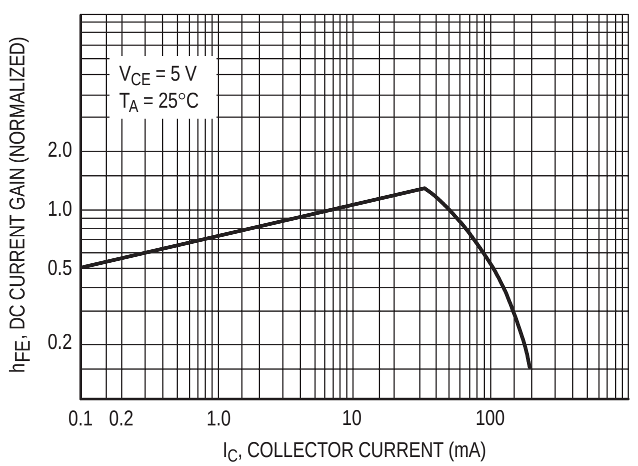


Figure 7. DC Current Gain

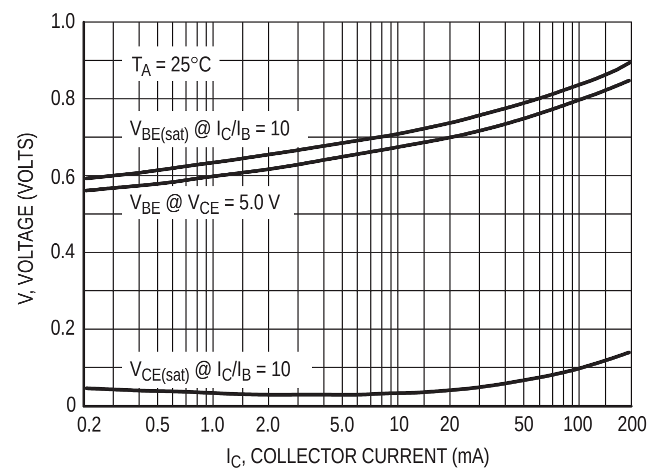


Figure 8. "On" Voltage

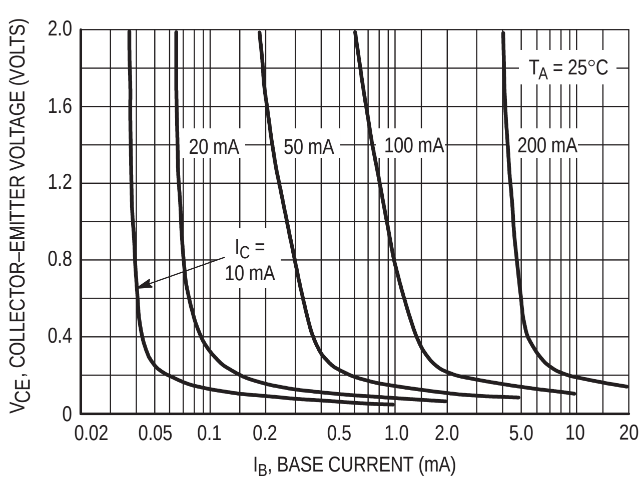


Figure 9. Collector Saturation Region

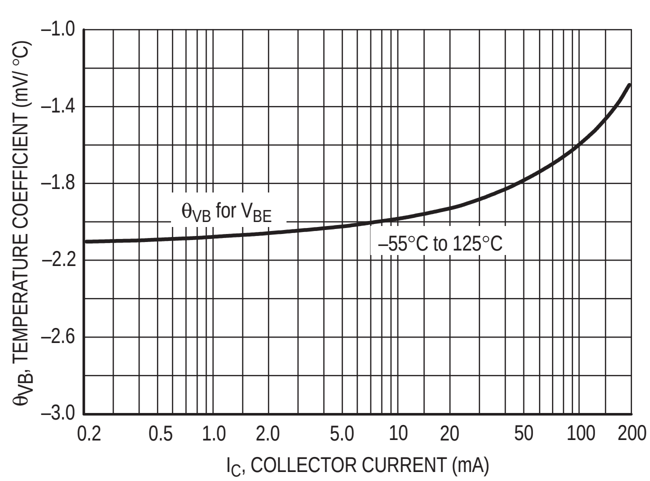


Figure 10. Base−Emitter Temperature Coefficient

TYPICAL PNP CHARACTERISTICS — BC846

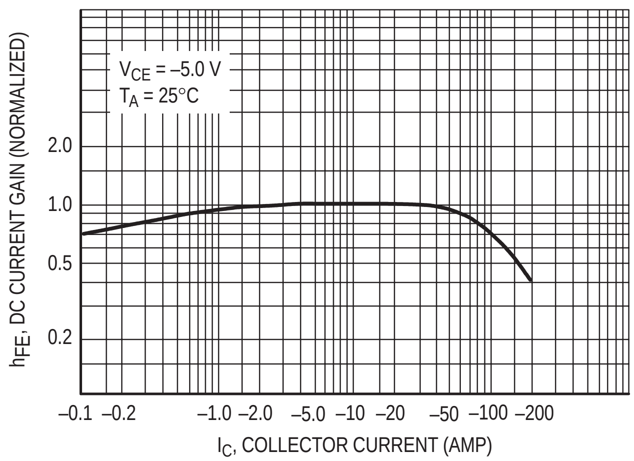


Figure 11. DC Current Gain

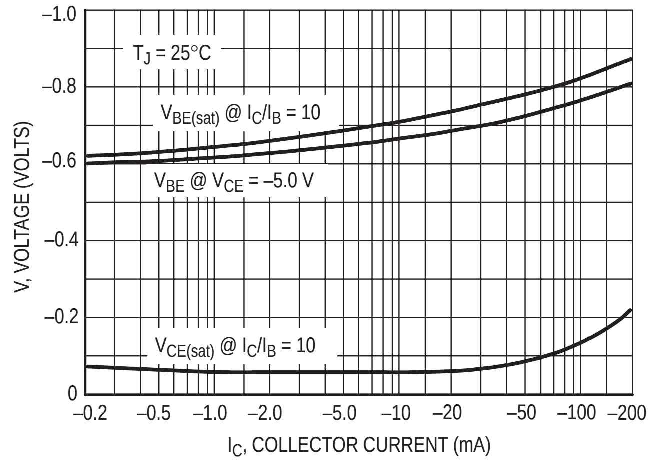


Figure 12. "On" Voltage

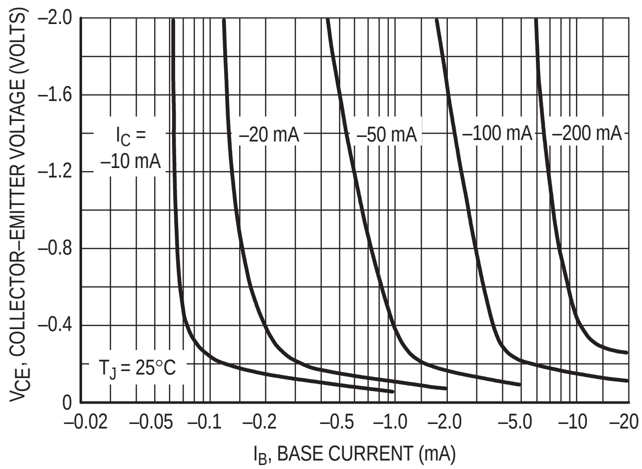


Figure 13. Collector Saturation Region

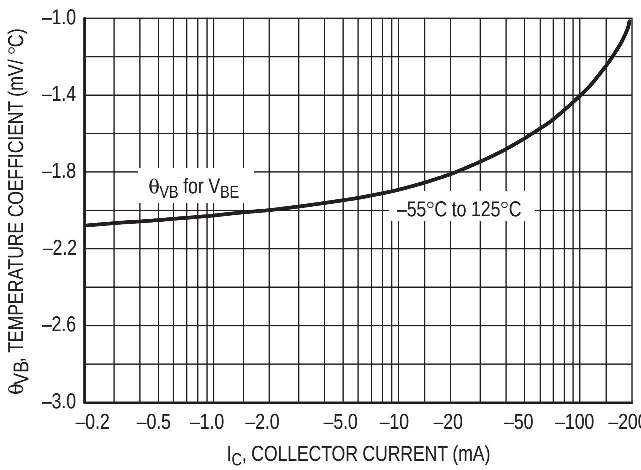


Figure 14. Base–Emitter Temperature Coefficient

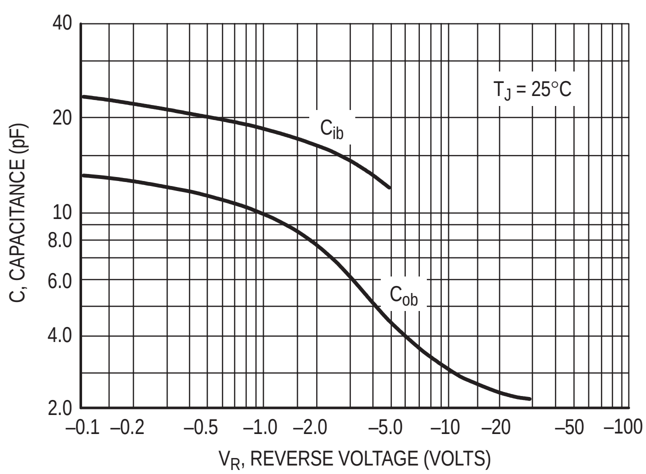


Figure 15. Capacitance

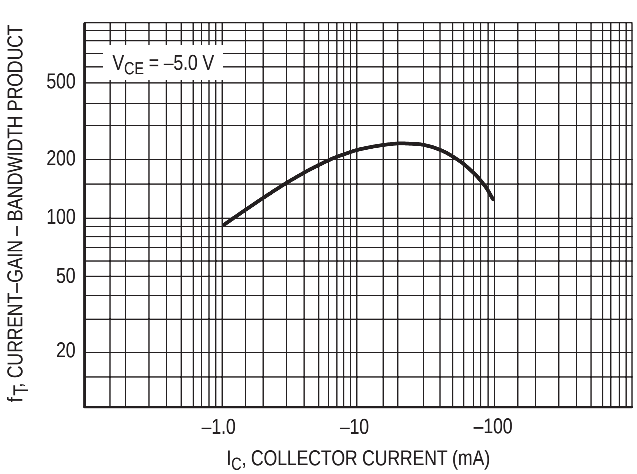


Figure 16. Current–Gain – Bandwidth Product

TYPICAL PNP CHARACTERISTICS — BC847/BC848

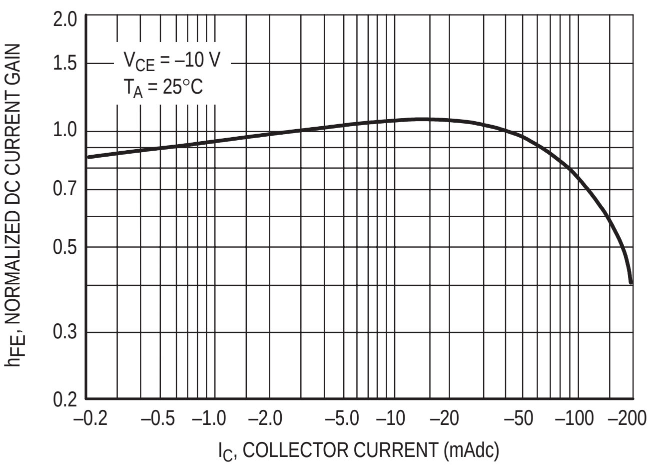


Figure 17. Normalized DC Current Gain

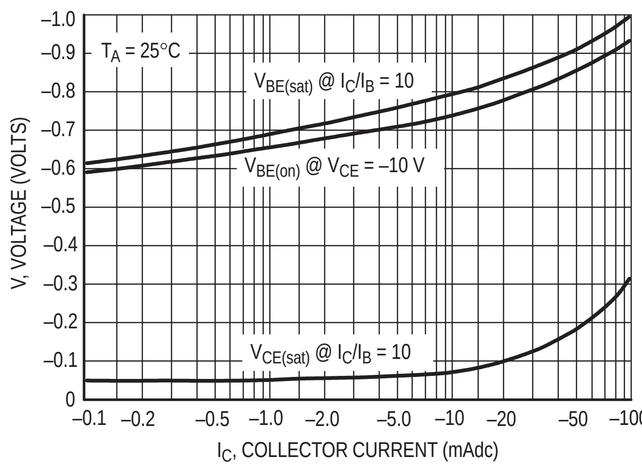


Figure 18. “Saturation” and “On” Voltages

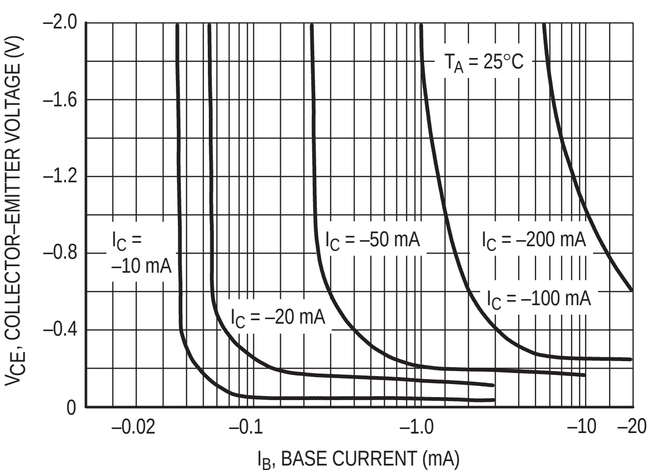


Figure 19. Collector Saturation Region

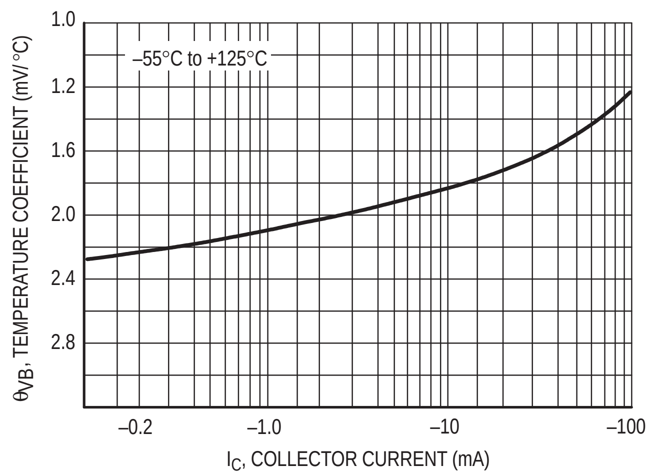


Figure 20. Base–Emitter Temperature Coefficient

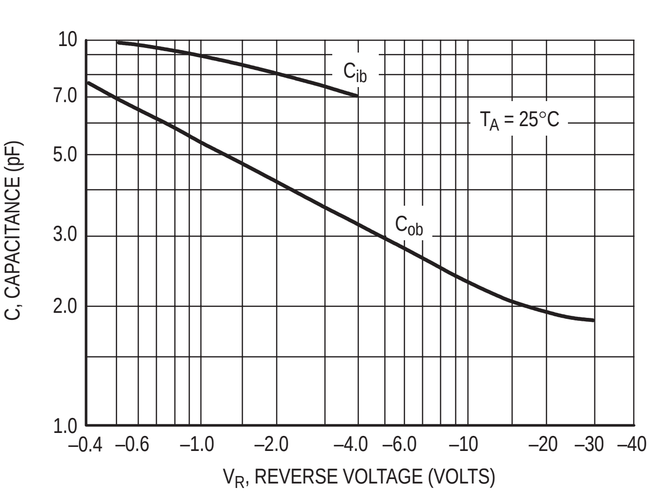


Figure 21. Capacitances

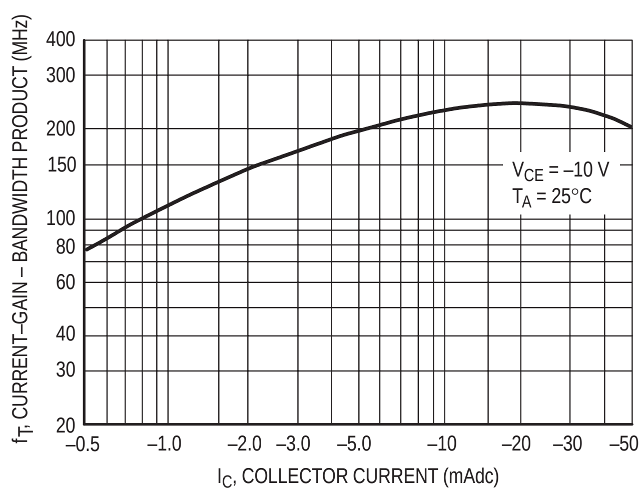


Figure 22. Current–Gain – Bandwidth Product

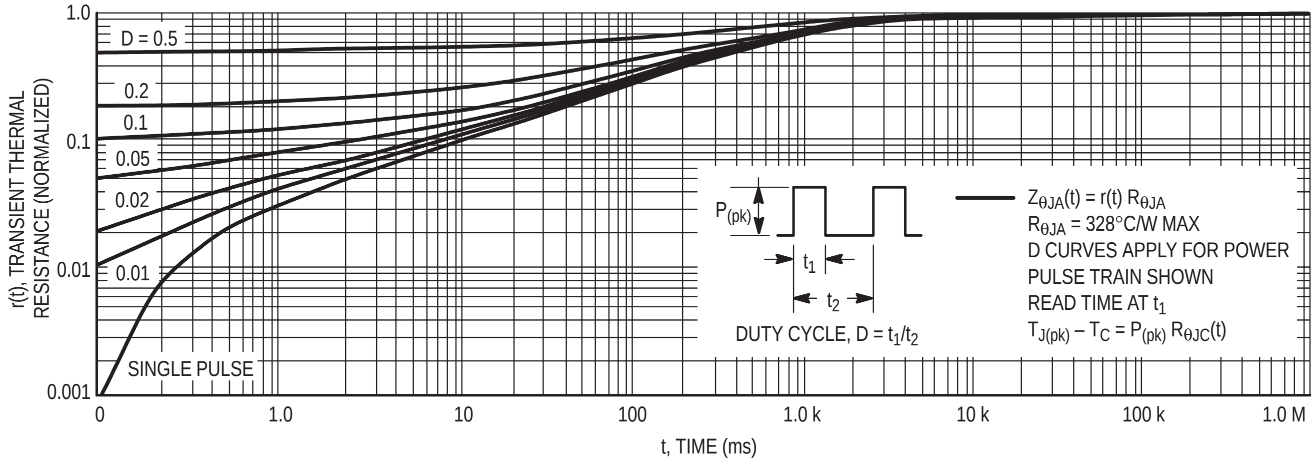


Figure 23. Thermal Response

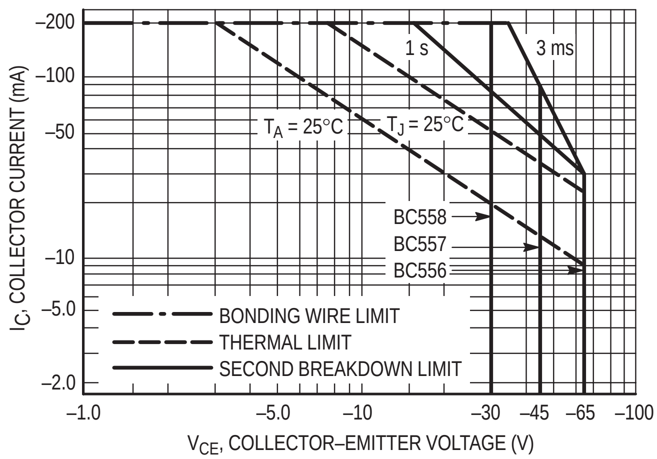


Figure 24. Active Region Safe Operating Area

The safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

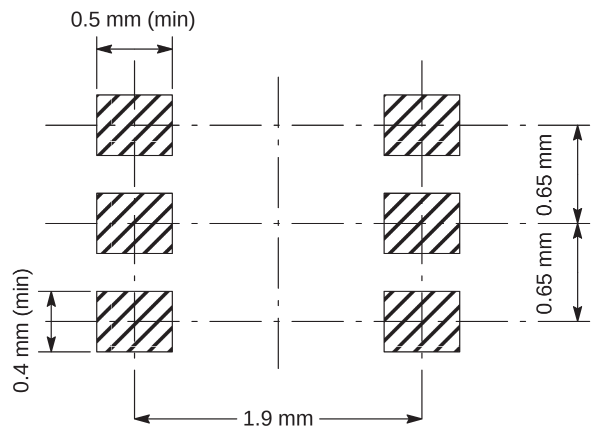
The data of Figure 14 is based upon $T_{J(pk)} = 150°C$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown.

INFORMATION FOR USING THE SOT–363 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

SOT–363



SOT–363 POWER DISSIPATION

The power dissipation of the SOT–363 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–363 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT–363 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–363 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

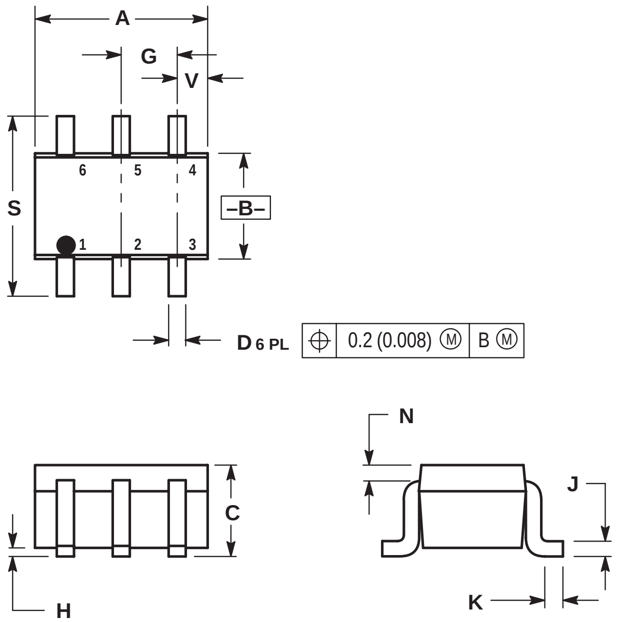
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

Notes

PACKAGE DIMENSIONS

SOT–363/SC–88
CASE 419B–01
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

Thermal Clad is a trademark of the Bergquist Company.

PUBLICATION ORDERING INFORMATION

North America Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

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Email: ONlit–french@hibbertco.com
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Email: r14153@onsemi.com

Fax Response Line: 303–675–2167
800–344–3810 Toll Free USA/Canada

ON Semiconductor Website: http://onsemi.com

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Sales Representative.