CRYSTAL®

CS5460A

Single Phase Bi-Directional Power/Energy IC

Features

- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range
- On-Chip Functions: Energy, I $*$ V, I_{RMS} and V_{RMS}, Energy-to-Pulse Conversion
- Smart "Auto-Boot" Mode from Serial EEPROM with no microcontroller.
- AC or DC System Calibration
- Mechanical Counter/Stepper Motor Driver
- Meets Accuracy Spec for IEC 687/1036, JIS
- Power Consumption <12 mW
- Interface Optimized for Shunt Sensor
- Phase Compensation
- Ground-Referenced Signals with Single Supply
- On-chip 2.5 V Reference (MAX 60 ppm/°C drift)
- Simple Three-Wire Digital Serial Interface
- Watch Dog Timer
- Power Supply Monitor
- Power Supply Configurations
  VA+ = +5 V; VA- = 0 V; VD+ = +3 V to +5 V
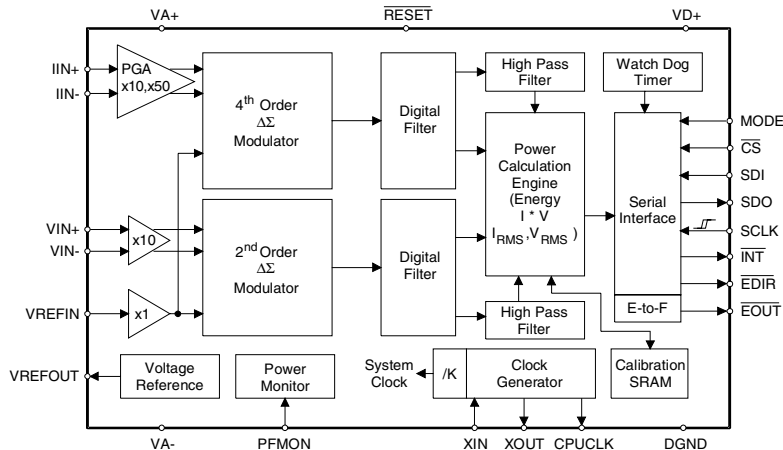 VA+ = +2.5 V; VA- = -2.5 V; VD+ = +3 V

Description

The CS5460A is a highly integrated $\Delta\Sigma$ Analog-to-Digital Converter (ADC) which combines two $\Delta\Sigma$ ADCs, high speed power calculation functions, and a serial interface on a single chip. It is designed to accurately measure and calculate: Energy, Instantaneous Power, I_{RMS}, and V_{RMS} for single phase 2- or 3-wire power metering applications. The CS5460A interfaces to a low-cost shunt resistor or transformer to measure current, and resistive divider or potential transformer to measure voltage. The CS5460A features a bi-directional serial interface for communication with a micro-controller and a programmable frequency output that is proportional to energy. CS5460A has on-chip functionality to facilitate AC or DC system-level calibration.

The "Auto-Boot" feature allows the CS5460A to function 'stand-alone' and to initialize itself on system power up. In Auto-Boot Mode, the CS5460A reads the calibration data and start-up instructions from an external EEPROM. In this mode, the CS5460A can work without the need for a microprocessor, for low-cost metering applications.

ORDERING INFORMATION:
    CS5460A-BS   -40°C to +85°C   24-pin SSOP

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Contacting Cirrus Logic Support

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http://www.cirrus.com/corporate/contacts/sales/cfm

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ANALOG CHARACTERISTICS (T$_A$ = -40° C to +85° C; VA+, VD+ = +5 V ±10%; VREFIN = 2.5 V; VA- = AGND; MCLK = 4.096 MHz, K = 1; N = 4000, OWR = 4.0 kHz.)(See Notes 1, 2, and 3)

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (Both Channels)						
Total Harmonic Distortion		THD	74	-	-	dB
Common Mode Rejection (DC, 50, 60 Hz)		CMRR	80	-	-	dB
Offset Drift (Without the High Pass Filter)			-	5	-	nV/°C
Analog Inputs (Current Channel)						
Differential Input Voltage Range {(IIN+) - (IIN-)} (Gain = 10)		IIN	0	-	±250	mV(dc)
(Gain = 50)			0	-	±50	mV(dc)
Common Mode + Signal on IIN+ or IIN- (Gain = 10 or 50)			-0.25	-	VA+	V
Crosstalk with Voltage Channel at Full Scale (50, 60 Hz)			-	-	-115	dB
Input Capacitance (Gain = 10)		IC	-	25	-	pF
(Gain = 50)			-	25	-	pF
Effective Input Impedance (Note 4)		EII				
(Gain = 10)			30	-	-	kΩ
(Gain = 50)			30	-	-	kΩ
Noise (Referred to Input) (Gain = 10)			-	-	20	µV$_{rms}$
(Gain = 50)			-	-	4	µV$_{rms}$
Accuracy (Current Channel)						
Bipolar Offset Error (Note 1)		VOS	-	-	±0.001	%F.S.
Full-Scale Error (Note 1)		FSE	-	-	±0.001	%F.S.
Analog Inputs (Voltage Channel)						
Differential Input Voltage Range {(VIN+) - (VIN-)}		VIN	0	-	±250	mV(dc)
Common Mode + Signal on VIN+ or VIN-			-0.25	-	VA+	V
Crosstalk with Current Channel at Full Scale (50, 60 Hz)			-	-	-70	dB
Input Capacitance		IC	-	0.2	-	pF
Effective Input Impedance (Note 4)		EII	5	-	-	MΩ
Noise (Referred to Input)			-	-	250	µV$_{rms}$
Accuracy (Voltage Channel)						
Bipolar Offset Error (Note 1)		VOS	-	-	±0.01	%F.S.
Full-Scale Error (Note 1)		FSE	-	-	±0.01	%F.S.

Notes: 1. Applies after system calibration

2. Specifications guaranteed by design, characterization, and/or test.

3. Analog signals are relative to VA- and digital signals to DGND unless otherwise noted.

4. Effective Input Impedance (EII) is determined by clock frequency (DCLK) and Input Capacitance (IC). EII = 1/(IC*DCLK/4). Note that DCLK = MCLK / K.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Phase Compensation Range (Voltage Channel, 60 Hz)		-2.4	-	+2.5	°
High Rate Filter Output Word Rate (Both Channels)	OWR	-	DCLK/1024	-	Hz
Input Sampling Rate DCLK = MCLK/K		-	DCLK/4	-	Hz
Full Scale DC Calibration Range (Note 5)	FSCR	25	-	100	%F.S.
Channel-to-Channel Time-Shift Error (when PC[6:0] bits are set to "0000000")			1.0		μs
High Pass Filter Pole Frequency -3 dB		-	0.5	-	Hz
Reference Output					
Output Voltage	REFOUT	2.4	-	2.6	V
Temperature Coefficient		-	25	60	ppm/°C
Load Regulation (Output Current 1 μA Source or Sink)	ΔV_R	-	6	10	mV
Output Noise Voltage (0.1 Hz to 512 kHz)	eN	-	100	-	μV$_{rms}$
Reference Input					
Input Voltage Range	VREFIN	2.4	2.5	2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	25	-	nA
Power Supplies					
Power Supply Currents (Active State) I$_{A+}$	PSCA	-	1.3	-	mA
I$_{D+}$ (VD+ = 5 V)	PSCD	-	2.9	-	mA
I$_{D+}$ (VD+ = 3 V)	PSCD	-	1.7	-	mA
Power Consumption Active State (VD+ = 5 V)	PC	-	21	25	mW
(Note 6) Active State (VD+ = 3 V)		-	11.6	-	mW
Stand-By State		-	6.75	-	mW
Sleep State		-	10	-	μW
Power Supply Rejection Ratio (50, 60 Hz)		-	-		
(Note 7) (Gain = 10)	PSRR	56			dB
(Gain = 50)	PSRR	70			dB
PFMON Low-Voltage Trigger Threshold (Note 8)	PMLO	2.3	2.45	-	V
PFMON High-Voltage Power-On Trip Point (Note 9)	PMHI	-	2.55	2.7	V

Notes: 5. The minimum FSCR is limited by the maximum allowed gain register value.

6. All outputs unloaded. All inputs CMOS level.

7. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5V, a 150mV rms (60 Hz) sinewave is imposed onto the +5V supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to VA-. Then the CS5460A is commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The rms value of the digital sinusoidal output signal is determined, and this rms value is converted into the rms value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as V$_{eq}$. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{150}{V_{eq}}\right\}$$

8. When voltage level on PFMON is sagging, and LSD bit is at 0, the voltage at which LSD bit is set to 1.

9. If the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), if the PFMON voltage starts to rise again, this is the voltage level on PFMON at which the LSD bit can be permanently reset back to 0 (without instantaneously changing back to 1). This indicates that power has been restored. Typically, for a given sample, the PMHI voltage will be ~100mV above the PMLO voltage.

5 V DIGITAL CHARACTERISTICS (T_A = -40° C to +85° C; VA+, VD+ = 5 V ±10% VA-, DGND = 0 V) (See Notes 2 and 10)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		-	-	0.8	V
XIN		-	-	1.5	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

3 V DIGITAL CHARACTERISTICS (T$_A$ = -40° C to +85° C; VA+ = 5 V ±10%, VD+ = 3 V ±10%; VA-, DGND = 0 V) (See Notes 2 and 10)

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V$_{IH}$				
All Pins Except XIN and SCLK and $\overline{RESET}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{RESET}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V$_{IL}$				
All Pins Except XIN and SCLK and $\overline{RESET}$		-	-	0.48	V
XIN		-	-	0.3	V
SCLK and $\overline{RESET}$		-	-	0.2 VD+	V
High-Level Output Voltage I$_{out}$ = +5 mA	V$_{OH}$	(VD+) - 1.0	-	-	V
Low-Level Output Voltage I$_{out}$ = -5 mA	V$_{OL}$	-	-	0.4	V
Input Leakage Current	I$_{in}$	-	±1	±10	µA
3-State Leakage Current	I$_{OZ}$	-	-	±10	µA
Digital Output Pin Capacitance	C$_{out}$	-	5	-	pF

Notes: 10.   All measurements performed under static conditions.

ABSOLUTE MAXIMUM RATINGS (DGND = 0 V; See Note 11)

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supplies (Notes 12 and 13)					
Positive Digital	VD+	-0.3	-	+6.0	V
Positive Analog	VA+	-0.3	-	+6.0	V
Negative Analog	VA-	+0.3	-	-6.0	V
Input Current, Any Pin Except Supplies (Note 14 and 15)	I$_{IN}$	-	-	±10	mA
Output Current	I$_{OUT}$	-	-	±25	mA
Power Dissipation (Note 16)	PDN	-	-	500	mW
Analog Input Voltage All Analog Pins	V$_{INA}$	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage All Digital Pins	V$_{IND}$	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature	T$_A$	-40	-	85	°C
Storage Temperature	T$_{stg}$	-65	-	150	°C

Notes: 11.   All voltages with respect to ground.

12.   VA+ and VA- must satisfy {(VA+) - (VA-)} ≤ +6.0 V.

13.   VD+ and VA- must satisfy {(VD+) - (VA-)} ≤ +6.0 V.

14.   Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.

15.   Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

16.   Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
        Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = -40° C to +85 °C; VA+ = 5.0 V ±10%; VD+ = 3.0 V ±10% or 5.0 V ±10%; VA- = 0.0 V; Logic Levels: Logic 0 = 0.0 V, Logic 1 = VD+; CL = 50 pF))

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency Internal Gate Oscillator (Note 17)		MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle			40	-	60	%
CPUCLK Duty Cycle	(Note 18)		40		60	%
Rise Times Any Digital Input Except SCLK (Note 19)		t_{rise}	-	-	1.0	µs
	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Fall Times Any Digital Input Except SCLK (Note 19)		t_{fall}	-	-	1.0	µs
	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Start-up						
Oscillator Start-Up Time XTAL = 4.096 MHz (Note 20)		t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock Pulse Width High		t_1	200	-	-	ns
Pulse Width Low		t_2	200	-	-	ns
SDI Timing						
CS Falling to SCLK Rising		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SCLK Falling Prior to CS Disable		t_6	100	-	-	ns
SDO Timing						
CS Falling to SDO Driving		t_7	-	20	50	ns
SCLK Falling to New Data Bit (hold time)		t_8	-	20	50	ns
CS Rising to SDO Hi-Z		t_9	-	20	50	ns
Auto-Boot Timing						
Serial Clock Pulse Width High		t_{10}		8		MCLK
Pulse Width Low		t_{11}		8		MCLK
MODE setup time to RESET Rising		t_{12}	50			ns
RESET rising to CS falling		t_{13}	48			MCLK
CS falling to SCLK rising		t_{14}	100	8		MCLK
SCLK falling to CS rising		t_{15}		16		MCLK
CS rising to driving MODE low (to end auto-boot sequence).		t_{16}	50			ns
SDO guaranteed setup time to SCLK rising		t_{17}	100			ns

Notes: 17. Device parameters are specified with a 4.096 MHz clock, however, clocks between 3 MHz to 20 MHz can be used.

18. If external MCLK is used, then its duty cycle must be between 45% and 55% to maintain this spec.

19. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

20. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.
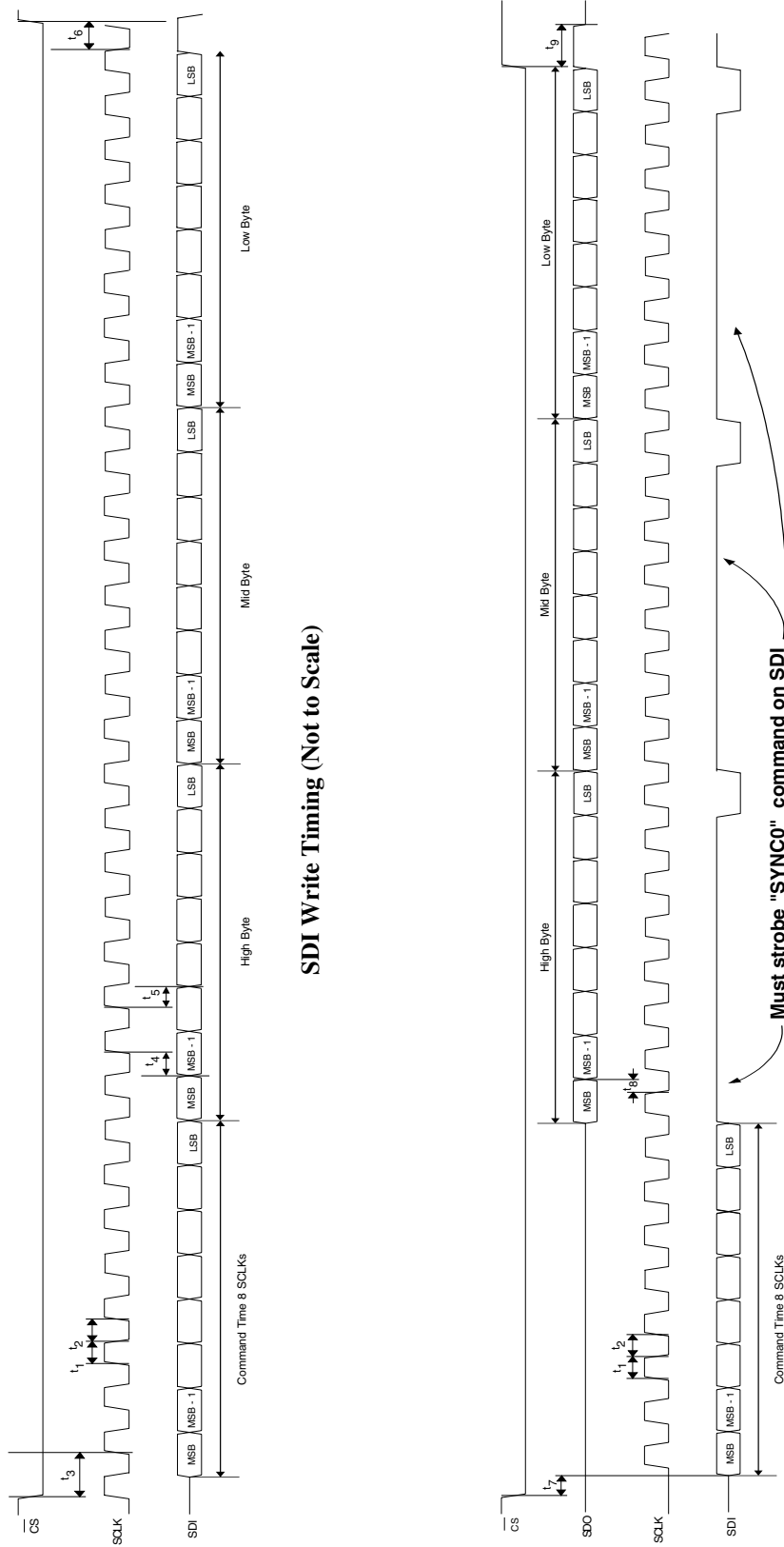
Figure 1. CS5460A Read and Write Timing Diagrams
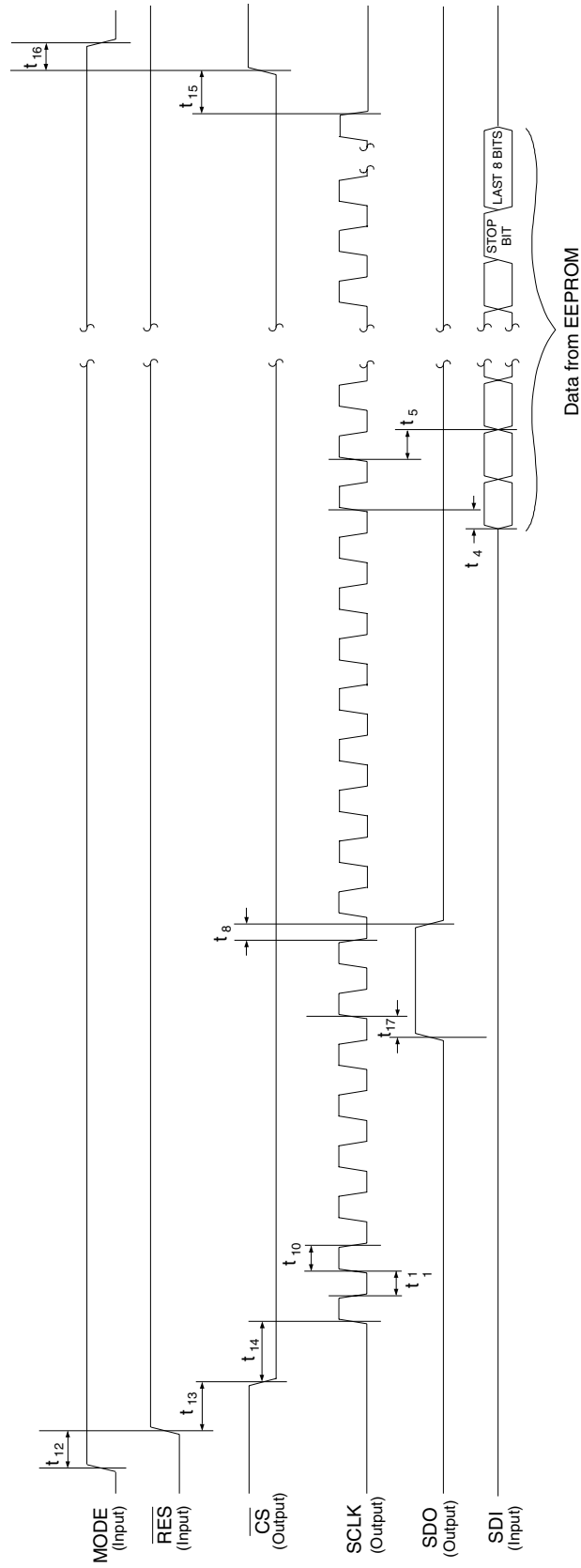
Figure 2. CS5460A Auto-Boot Sequence Timing

2. GENERAL DESCRIPTION

The CS5460A is a CMOS monolithic power measurement device with an energy computation engine. The CS5460A combines a programmable gain amplifier, two $\Delta\Sigma$ modulators, two high rate filters, system calibration, and power calculation functions to compute Energy, V_{RMS}, I_{RMS}, and Instantaneous Power.

The CS5460A is designed for power measurement applications and is optimized to interface to a shunt or current transformer to measure current, and a resistive divider or transformer to measure voltage. To accommodate various input voltage levels, the current channel includes a programmable gain amplifier (PGA) which provides either ±250 mV or ±50 mV as the full-scale input level. The voltage channel's PGA has only one gain setting (10x) which allows an input range of ±250 mV. With single +5 V supply on VA+/-, both of the CS5460A's input channels accommodate common mode + signal levels between -0.25 V and VA+.

The CS5460A includes two high-rate digital filters, which decimate the output from the 2 $\Delta\Sigma$ modulators. These filters yield 24-bit output data at a (MCLK/K)/1024 output word rate (OWR). The OWR can be thought of as the effective sampling rate of the voltage channel and the current channel.

To facilitate communication to a microcontroller, the CS5460A includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The serial port has a Schmitt Trigger input on its SCLK (serial clock) and $\overline{RESET}$ pins to allow for slow rise time signals.

2.1 Theory of Operation

A computational flow diagram for the two data paths is shown in Fig. 3. The analog waveforms at the voltage/current channel inputs are subject to the gains of the input PGAs (not shown in Figure 3). These waveforms are then sampled by the delta-sigma modulators at a rate of (MCLK/K) / 8.

2.1.1 High-Rate Digital Low-Pass Filters

The data is then low-pass filtered, to remove high-frequency noise from the modulator output. Referring to Figure 3, the high rate filter on the voltage channel is implemented as a fixed Sinc^2 filter.

Also note from Figure 3 that the digital data on the voltage channel is subjected to a variable time-delay filter. The amount of delay depends on the value of the seven phase compensation bits (see *Phase Compensation*), which can be set by the user. Note that when the phase compensation bits PC[6:0] are set to their default setting of "0000000" (and if MCLK/K = 4.096MHz) then the nominal time delay that is imposed on the original analog voltage input signal, with respect to the original analog current input signal, is ~1.0 μs. This translates into a delay of ~0.0216 degrees at 60Hz.

2.1.2 Digital Compensation Filters

The data from both channels is then passed through two FIR compensation filters, whose purpose is to compensate for the magnitude roll-off of the low-pass filtering operation (mentioned earlier).

2.1.3 Digital High-Pass Filters

Both channels provide an optional high-pass filter (denoted as "HPF" in Figure 3) which can be engaged into the signal path to remove the DC content from the current/voltage signal before the RMS/energy calculations are made. These filters are activated by enabling certain bits in the Configuration Register.

If the user wants to use the high-pass filter on only one of the two channels, then the user should engage the all-pass filter (see "APF" in Figure 3) on the other channel, in order to preserve the relative phase relationship between the voltage-sense and current-sense input signals. For example, if the HPF is needed for voltage channel, but not the current channel, then the APF should be engaged in the
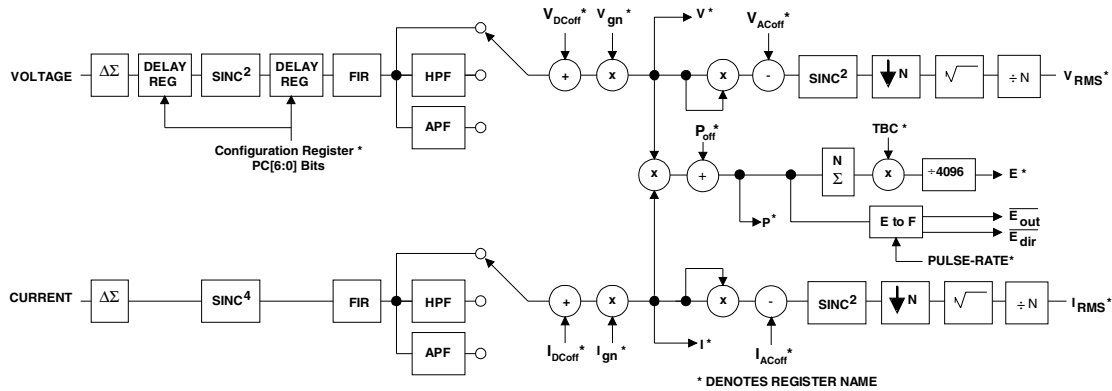
Figure 3. Data Flow.

voltage channel, to match the phase delay that is introduced by the high-pass filter.

2.1.4 Overall Filter Response

When the CS5460A is driven with a 4.096 MHz clock (K=1), the composite magnitude response (over frequency) of the voltage channel's input filter network is shown in Figure 4, while the composite magnitude response of the current channel's input filter network is given in Figure 5. Note that the composite filter response of both channels scales with MCLK frequency and K.

2.1.5 Gain and DC Offset Adjustment

After the filtering, the instantaneous voltage and current digital codes are both subjected to value adjustments, based on the values in the DC Offset Registers (additive) and the Gain Registers (multiplicative). These registers are used for calibration of the device (see *Section 4.8, Calibration*). After offset and gain, the instantaneous data is available to the user by reading the Instantaneous Voltage and Current Registers.

2.1.6 Power/Energy, and RMS Computations

The digital instantaneous voltage and current data is then processed further. Referring to Figure 3, the

instantaneous voltage/current data samples are multiplied together (one multiplication for each pair of voltage/current samples) to form instantaneous power data, which is available to the user by reading the Instantaneous Power Register. The instantaneous power data is summed over N instantaneous conversions (N = value in Cycle Count Register) to form a result in the Energy Register. The bits in this running energy sum are left-shifted 12 times (divided by 4096) to avoid overflow in the Energy Register. RMS calculations are performed on the data and can be read from the RMS Voltage Register and the RMS Current Register.

2.2 Performing Measurements

The CS5460A performs measurements of instantaneous current, instantaneous voltage, instantaneous power, energy, RMS current, and RMS voltage. These measurements are output as 24-bit signed and unsigned data formats as a percentage of full scale. Note that the 24-bit *signed* output format is a two's complement format. The 24-bit data words in the CS5460A output registers represent values between 0 and 1 (for unsigned output registers) or between -1 and +1 (for signed output registers). A

register value of 1 represents the maximum possible value. Note that a value of 1.0 is never actually obtained in the registers of the CS5460A. As an illustration, in any of the signed output registers, the maximum register value is $[(2^{23} - 1) / (2^{23})] = 0.999999880791$. After each A/D conversion, the CRDY bit will be asserted in the Status Register, and the $\overline{INT}$ pin will also become active if the CRDY bit is unmasked (in the Mask Register). The assertion of the CRDY bit indicates that new instantaneous voltage and current samples have been collected, and these two samples have also been multiplied together to provide a corresponding instantaneous power sample.
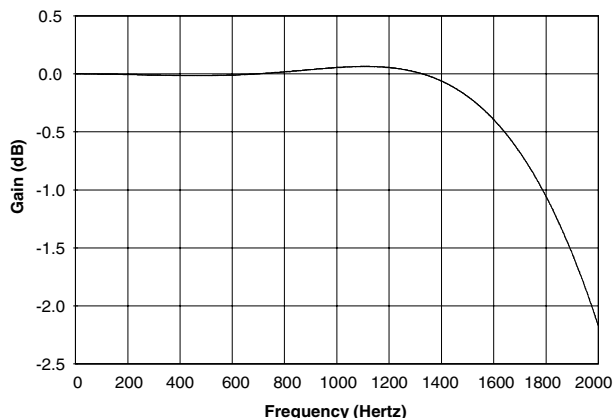
Figure 4. Voltage Input Filter Characteristics
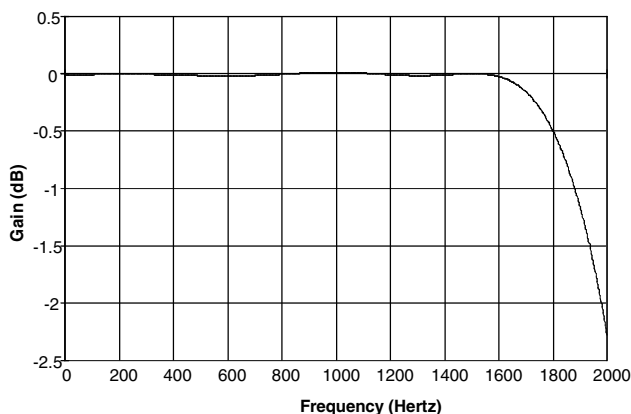
Figure 5. Current Input Filter Characteristics

The V_{RMS}, I_{RMS}, and energy calculations are updated every N conversions (which is known as 1 "*computation cycle*") where N is the value in the Cycle Count Register. At the end of each computation cycle, the DRDY bit in the Mask Register will be set, and the $\overline{INT}$ pin will become active if the DRDY bit is unmasked.

DRDY is set only after each computation cycle has completed, whereas the CRDY bit is asserted after each individual A/D conversion. When these bits are asserted, they must be cleared by the user before they can be asserted again. If the Cycle Count Register value (N) is set to 1, all output calculations are instantaneous, and DRDY will indicate when instantaneous calculations are finished, just like the CRDY bit. For the RMS results to be valid, the Cycle-Count Register must be set to a value greater than 10.

A computation cycle is derived from the master clock and its frequency is (MCLK/K)/(1024*N). Under default conditions with a 4.096 Mhz clock at XIN, instantaneous A/D conversions for voltage, current, and power are performed at a 4000 Hz rate, whereas I_{RMS}, V_{RMS}, and energy calculations are performed at a 1 Hz rate.

2.3 CS5460A Linearity Performance

Table 1 lists the range of input levels (as a percentage of full-scale registration in the Energy, Irms, and Vrms Registers) over which the output linearity of the Vrms, Irms and Energy Register measure-

	Energy	**Vrms**	**Irms**
Range (% of FS)	0.1% - 100%	50% - 100%	0.2% - 100%
Max Input (dc volts)	*not applicable*	V-channel: ±250mV	I-channel: ±250mV 10x ±50mV 50x
Linearity	0.1% of reading	0.1% of reading	0.1% of reading

Table 1. Available range of ±0.1% output linearity, with default settings in the gain/offset registers.

ments are guaranteed to be within ±0.1%. Note that until the CS5460A is calibrated (see Calibration) the *accuracy* of the CS5460A (with respect to a reference line-voltage and line-current level on the power mains) is not guaranteed to within ±0.1%. But the *linearity* of any given sample of CS5460A, before calibration, will be within ±0.1% of reading over the ranges specified, with respect to the input voltage levels required (on the voltage and current channels) to cause full-scale readings in the Irms/Vrms Registers. Note that the ±0.1% of reading specs in Table 1 imply linearity + variation, after the completion of each successive computation cycle. Finally, observe that the maximum (full-scale) differential input voltage for the voltage channel (and current channel, in 10x PGA gain setting) is 250mV (nominal). **If the gain registers of both channels are set to 1 (default) and the two dc offset registers are set to zero (default), then a 250mV dc signal applied to the voltage/current inputs will measure at (or near) the maximum value of 0.9999... in the RMS Current/Voltage Registers.** Remember that the RMS value of a 250mV (dc) signal is also 250mV. However, for either input channel, it would not be practical to inject a sinusoidal voltage with RMS value of 250mV. This is because when such a sine wave enters the positive crest region of each cycle, the voltage level of this signal would exceed the maximum differential input voltage range of the input channels. The largest sine wave voltage signal that can be presented across the inputs, with no saturation of the inputs, is 250mV / sqrt(2) = ~176.78 mV (RMS), which is at ~70.7% of full-scale. This would imply that for the current channel, the linearity + variation tolerance of the RMS measurements for a purely sinusoidal 60 Hz input could be measured to within ±0.1% of reading over a magnitude range of 0.2% - 70.7% (of the maximum full-scale differential input voltage level). The linearity range can often be improved by selecting a value for the Cycle-Count Register that will cause the

time duration of one computation cycle to be equal (or very close to) a whole-number of power-line cycles (and N must be greater than or equal to 4000). For example, with the cycle count set to 4200, the ±0.1% of reading linearity range for measurement of a 60 Hz sinusoidal current-sense voltage signal (created by sensing the current on a power line) can be increased beyond the range of 0.2% - 70.7%. The linearity range can be increased because (4200 samples / 60 Hz) is a whole number of cycles (70). Increasing the accuracy range is attractive, because this enables accurate measurement of even smaller power-line current levels.

2.3.1 Single Computation Cycle (C=0)

Note that 'C' refers to the value of the C bit, contained in the Start Conversions command (see Section 3.1). Based on the value in the Cycle Count Register, a single computation cycle is performed after the user transmits the Start Conversions command. After the computations are complete, DRDY is set. Thirty-two SCLKs are then needed to acquire a calculation result from one of several result registers. The first 8 SCLKs are used to clock in the command to determine which register is to be read. The last 24 SCLKs are used to read the desired register. After reading the data, the serial port remains in the *active state*, and waits for a new command to be issued. (See Section 3 for more details on reading register data from the CS5460A).

2.3.2 Continuous Computation Cycles (C=1)

Based on the information provided in the Cycle Count Register, computation cycles are repeatedly performed on the voltage and current channels (after every N conversions). Computation cycles cannot be started/stopped on a per channel basis. After each computation cycle is completed, DRDY is set. Thirty-two SCLKs are then needed to read a register. The first 8 SCLKs are used to clock in the command to determine which results register is to be read. The last 24 SCLKs are used to read the calculation result. While in this acquisition mode, the

user may choose to acquire only the calculations required for the application as DRDY rises and falls to indicate the availability of a new data.

Referring again to Figure 3, note that for the Irms and Vrms data paths, prior to the square-root operation, the instantaneous voltage/current data is low-pass filtered by a $Sinc^2$ filter. Then the data is decimated to every Nth sample. Because of the filter operation, the first output for each channel will be invalid (i.e. all RMS calculations are invalid in the single computation cycle routine and the first RMS calculations will be invalid in the continuous computation cycle). However, all energy calculations will be valid since energy calculations do not require this $Sinc^2$ operation.

After the user issues the continuous conversion command to the CS5460A (see *Section 3.1, Commands (Write Only)*), the device will remain in its *active state*, and it will be ready to accept other commands through the serial interface. But now, the CS5460A is continuously sampling data on the voltage/current channels.

2.4 Basic Application Circuit Configurations

Figure 6 shows the CS5460A connected to a service to measure power in a single-phase 2-wire system while operating in a single supply configuration. Note that in this diagram the shunt resistor used to monitor the line current is connected on the "Line" (hot) side of the power mains. In most residential power metering applications, the power meter's current-sense shunt resistor is intentionally placed on the hot side of the power mains in order to detect a subscriber's attempt to steal power. In this type of shunt-resistor configuration, note that the common-mode level of the CS5460A

must be referenced to the hot side of the power line. This means that the common-mode potential of the CS5460A will typically oscillate to very high voltage levels, as well as very low voltage levels, with respect to earth ground potential. *The designer must therefore be careful* when attempting to interface the CS5460A's digital output lines to an external digital interface (such as a LAN connection or other communication network). Such digital communication networks may require that the CMOS-level digital interface to the meter is referenced to an earth ground. Because of this requirement, note in Figure 6 that the digital serial interface pins on the CS5460A *must be isolated* from the external digital interface, so that there is no conflict between the ground references of the meter and the external interface.

Figure 7 shows how the same single-phase two-wire system can be metered while achieving complete isolation from the power lines. The isolation is achieved using three transformers. One transformer is a general purpose transformer to supply the on-board DC power to the CS5460A. A second transformer is a high-precision, low impedance voltage transformer with very little roll-off/phase delay, even at the higher harmonics. A current transformer is then used to sense the line current. Because the CS5460A is not directly connected to the power mains, no isolation is necessary on the CS5460A's digital interface.

Figure 8 shows the CS5460A configured to measure power in a single-phase 3-wire system. In many 3-wire residential power systems within the United States, only the two line terminals are available (neutral is not available). Figure 9 shows how the CS5460A can be configured to meter a three-wire system when no neutral is available.
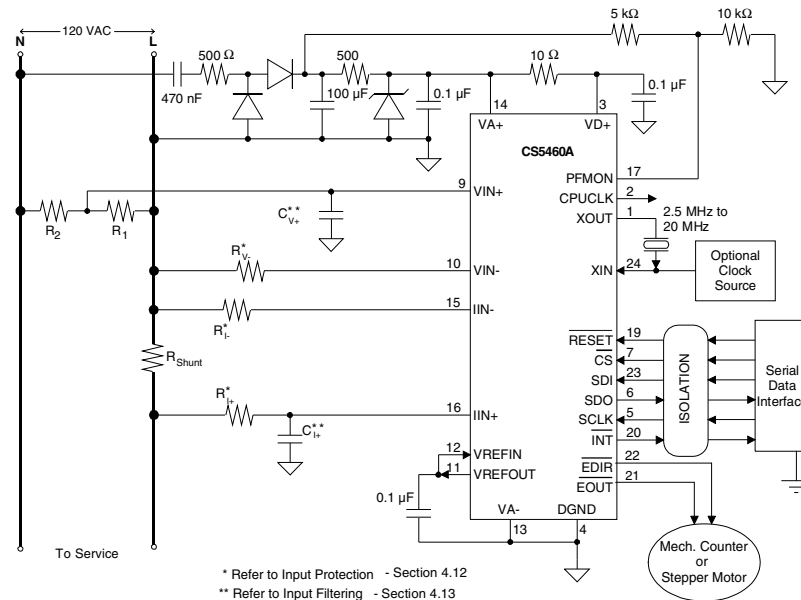
Figure 6. Typical Connection Diagram (One-Phase 2-Wire, Direct Connect to Power Line)
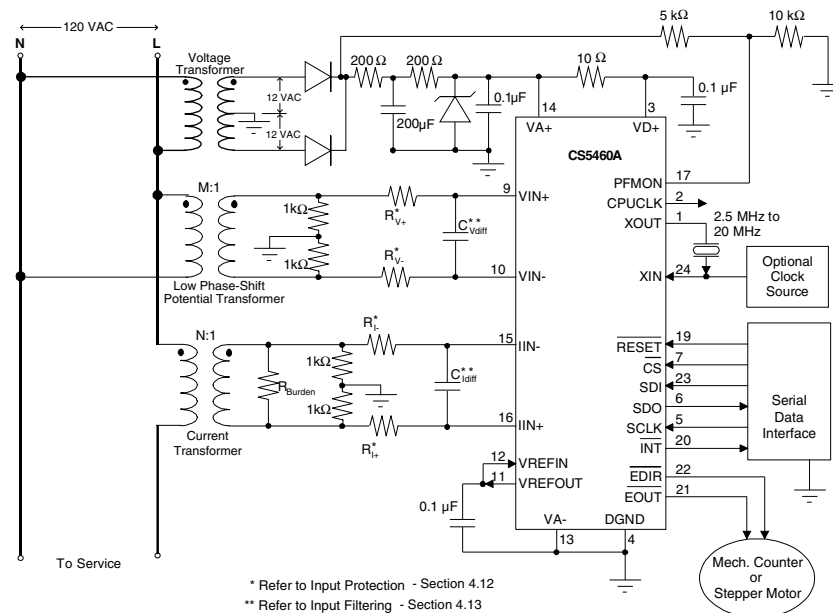
Figure 7. Typical Connection Diagram (One-Phase 2-Wire, Isolated from Power Line)

3. SERIAL PORT OVERVIEW

The CS5460A's serial port incorporates a state machine with transmit/receive buffers. The state machine interprets 8 bit command words on the rising edge of SCLK. Upon decoding of the command word, the state machine performs the requested command or prepares for a data transfer of the addressed register. Request for a read requires an internal register transfer to the transmit buffer, while a write waits until the completion of 24 SCLKs before performing a transfer. The internal registers
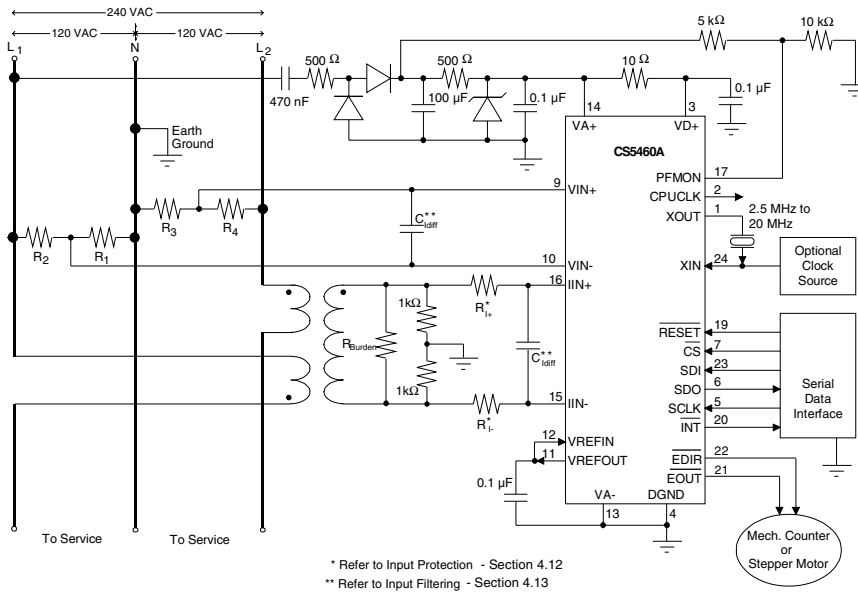
Figure 8. Typical Connection Diagram (One-Phase 3-Wire)
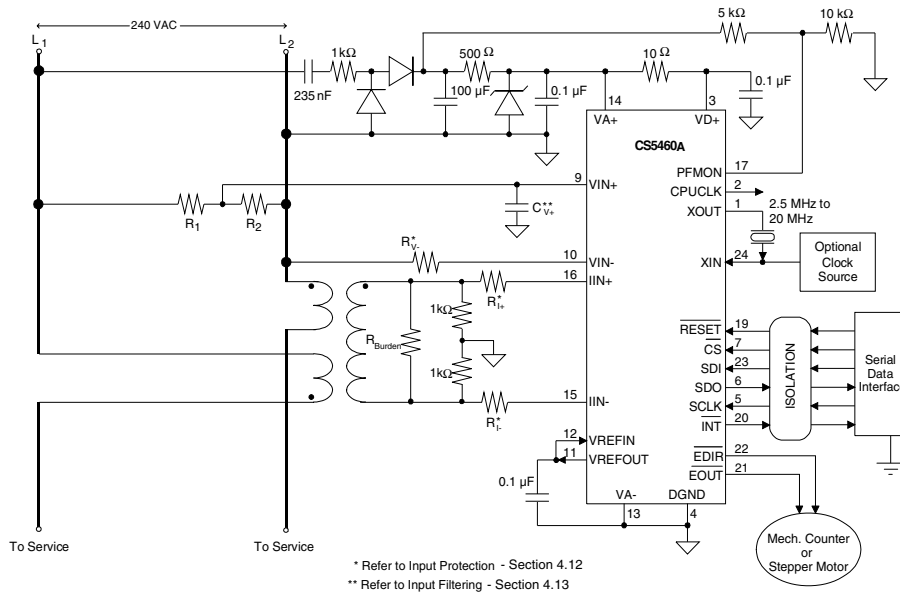
Figure 9. Typical Connection Diagram (One-Phase 3-Wire - No Neutral Available)

are used to control the ADC's functions. All registers are 24-bits in length. Figure 24 summarizes the internal registers available to the user.

The CS5460A is initialized and fully operational in its *active* state upon power-on. After a power-on, the device will wait to receive a valid command

(the first 8-bits clocked into the serial port). Upon receiving and decoding a valid command word, the state machine instructs the converter to either perform a system operation, or transfer data to or from an internal register. The user should refer to the "Commands" section to decode all valid commands.

3.1 Commands (Write Only)

All command words are 1 byte in length. Commands that write to a register must be followed by 1, 2, or 3 bytes of register data. Commands that read from registers initiate 3 bytes of register data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent to SDI which can execute before the original read is completed). This allows for "chaining" commands.

3.1.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C	0	0	0

This command indicates to the state machine to begin acquiring measurements and calculating results. The device has two modes of acquisition.

C = Modes of acquisition/measurement
 0 = Perform a single computation cycle
 1 = Perform continuous computation cycles

3.1.2 SYNC0 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	0

This command is the end of the serial port re-initialization sequence. The command can also be used as a NOP command. The serial port is resynchronized to byte boundaries by sending three or more consecutive SYNC1 commands followed by a SYNC0 command.

3.1.3 SYNC1 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	1

This command is part of the serial port re-initialization sequence. The command can also serve as a NOP command.

3.1.4 Power-Up/Halt

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down, this command will power-up the device. When powered-on, no computations will be running. If the part is already powered-on, all computations will be halted.

3.1.5 Power-Down

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

The device has two power-down states to conserve power. If the chip is put in stand-by state, all circuitry except the analog/digital clock generators is turned off. In the sleep state, all circuitry except the digital clock generator and the instruction decoder is turned off. Waking up the CS5460A out of sleep state requires more time than out of stand-by state, because of the extra time needed to re-start and re-stabilize the analog clock signal.

> S1,S0   Power-down state
> 00 = Reserved
> 01 = Halt and enter stand-by power saving state. This state allows quick power-on time
> 10 = Halt and enter sleep power saving state. This state requires a slow power-on time
> 11 = Reserved

3.1.6 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	V	I	R	G	O

The device has the capability of performing a system AC offset calibration, DC offset calibration, AC gain calibration, and DC gain calibration. The user can calibrate the voltage channel, the current channel, or both channels at the same time. Offset and gain calibrations should NOT be performed at the same time (must do one after the other). For a given application, if DC gain calibrations are performed, then AC gain calibration should not be performed (and vice-versa). The user must supply the proper inputs to the device before initiating calibration.

> V,I   Designates calibration channel
> 00 = Not allowed
> 01 = Calibrate the current channel
> 10 = Calibrate the voltage channel
> 11 = Calibrate voltage and current channel simultaneously
>
> R   Specifies AC calibration (R=1) or DC calibration (R=0)
>
> G   Designates gain calibration
> 0 = Normal operation
> 1 = Perform gain calibration
>
> O   Designates offset calibration
> 0 = Normal operation
> 1 = Perform offset calibration

3.1.7 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/$\overline{R}$	RA4	RA3	RA2	RA1	RA0	0

This command informs the state machine that a register access is required. On reads the addressed register is loaded into the output buffer and clocked out by SCLK. On writes the data is clocked into the input buffer and transferred to the addressed register on the 24th SCLK.

W/$\overline{R}$ Write/Read control
                         0 = Read register
                         1 = Write register

RA[4:0]   Register address bits. Binary encoded 0 to 31. All registers are 24 bits in length.

Address	Abbreviation	Name/Description
00000	Config	Configuration Register
00001	I_{DCoff}	Current Offset Register
00010	I_{gn}	Current Gain Register
00011	V_{DCoff}	Voltage Offset Register
00100	V_{gn}	Voltage Gain Register
00101	Cycle Count	Number of conversions to integrate over (N)
00110	Pulse-Rate	Used to set the $\overline{EOUT}$ energy-to-frequency output pulse ratio
00111	I	Instantaneous Current Register (last current value)
01000	V	Instantaneous Voltage Register (last voltage value)
01001	P	Instantaneous Power Register (Last Power value)
01010	E	Energy Register (total energy value over last computation cycle)
01011	I_{RMS}	RMS Current Register (RMS value over last computation cycle)
01100	V_{RMS}	RMS Voltage Register (RMS value over last computation cycle
01101	TBC	Timebase Calibration Register
01110	Poff	Power Offset Register
01111	Status	Status Register
10000	I_{ACoff}	AC Current Offset Register
10001	V_{ACoff}	AC Voltage Offset Register
10010	Res	Reserved †
.		
.		
10111	Res	Reserved †
11000	Res	Reserved †
11001	Test	Reserved †
11010	Mask	Mask Register
11011	Res	Reserved †
11100	Ctrl	Control Register
11101	Res	Reserved †
.		
.		
11111	Res	Reserved †

† These registers are for Internal Use only and should not be written to.

3.2 Serial Port Interface

The CS5460A's serial interface consists of four control lines, which have the following pin-names: $\overline{CS}$, SDI, SDO, and SCLK. Each control line is now described.

$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied to logic 0, the port can function as a three wire interface. SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held at logic 0 before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

3.3 Serial Read and Write

The state machine decodes the command word as it is received. Data is written to and read from the CS5460A by using the Register Read/Write command. Figure 1 illustrates the serial sequence necessary to write to, or read from the serial port's buffers. As shown in Figure 1, a transfer of data is always initiated by sending the appropriate 8-bit command (MSB first) to the serial port (SDI pin). It is important to note that some commands use information from the Cycle-Count Register and Configuration Register to perform the function. For those commands, it is important that the correct information is written to those registers first.

3.3.1 Register Write

When a command involves a write operation, the serial port will continue to clock in the data bits (MSB first) on the SDI pin for the next 24 SCLK cycles. Command words instructing a register write must be followed by 24 bits of data. For instance, to write the Configuration Register, the user would transmit the command (0x40) to initiate a write to the Configuration Register. The CS5460A will then acquire the serial data input from the (SDI) pin when the user pulses the serial clock (SCLK) 24 times. Once the data is received, the state machine writes the data to the Configuration Register and then waits to receive another valid command.

3.3.2 Register Read

When a read command is initiated, the serial port will start transferring register content bits serial (MSB first) on the SDO pin for the next 8, 16, or 24 SCLK cycles. Command words instructing a register read may be terminated at 8-bit boundaries (e.g., read transfers may be 8, 16, or 24 bits in length). Also data register reads allow "command chaining". This means that the micro-controller is allowed to send a new command while reading register data. The new command will be acted upon immediately and could possibly terminate the first register read. For example, if a command word is sent to the state machine to read one of the signed output registers, then after the user pulses SCLK for 16-bits of data, a second write command word (e.g., to clear the Status Register) may be pulsed on to the SDI line at the same time the last 8-bits of data (from the first read command) are pulsed from the SDO line. As another example, if the user is only interested in acquiring the 16 most significant bits of data from the first read, then the user can begin to strobe a second read command on SDI after the first 8 data bits have been read from SDO.

During the read cycle, the SYNC0 command (NOP) should be strobed on the SDI port while clocking the data from the SDO port.

3.4 System Initialization

A software or hardware reset can be initiated at any time. The software reset is initiated by writing a logic 1 to the RS (Reset System) bit in the Configuration Register, which automatically returns to logic 0 after reset. At the end of the 32nd SCLK (i.e., 8 bit command word and 24 bit data word) internal synchronization delays the loading of the Configuration Register by 3 or 4 DCLK cycles. Then the reset circuit initiates the reset routine on the 1st falling edge of MCLK.

A hardware reset is initiated when the $\overline{RESET}$ pin is forced low with a minimum pulse width of 50 ns. The $\overline{RESET}$ signal is asynchronous, requiring no MCLKs for the part to detect and store a reset event. The $\overline{RESET}$ pin is a Schmitt Trigger input, which allows it to accept slow rise times and/or noisy control signals. (This can often turn out to be the case, after a power failure or brown-out on the power line.) Once the $\overline{RESET}$ pin is inactive, the internal reset circuitry remains active for 5 MCLK cycles to insure resetting the synchronous circuitry in the device. The modulators are held in reset for

12 MCLK cycles after $\overline{RESET}$ becomes inactive. After a hardware or software reset, the internal registers (some of which drive output pins) will be reset to their default values on the first MCLK received after detecting a reset event (see Table 2). The CS5460A will then assume its *active* state. (The term *active state*, as well as the other possible power states of the CS5460A, are described in Section 3.6).

The reader should refer to Section 5 for a complete description of the registers listed in Table 2.

Configuration Register:	0x000001
Offset Register:	0x000000
Gain Registers	0x400000
Pulse-Rate Register:	0x0FA000
Cycle-Counter Register:	0x000FA0
Timebase Register:	0x800000
Status Register:	0x000000
Mask Register:	0x000000
Control Register:	0x000000
AC Current Offset Register:	0x000000
AC Voltage Offset Register:	0x000000
Power Offset Register:	0x000000
All Data Registers:	0x000000
All Unsigned Data Registers	0x000000

Table 2. Internal Registers Default Value

3.5 Serial Port Initialization

It is possible for the serial interface to become unsynchronized, with respect to the SCLK input. If this occurs, any attempt to clock valid CS5460A commands into the serial interface will result in either no operation or unexpected operation, because the CS5460A will not interpret the input command bits correctly. The CS5460A's serial port must then be re-initialized. To initialize the serial port, any of the following actions can be performed:

1) Power on the CS5460A. (Or if the device is already powered on, recycle the power.)

2) Hardware Reset

3) Issue the *Serial Port Initialization Sequence*, which is performed by clocking 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE).

3.6 CS5460A Power States

Active state denotes the operation of CS5460A when the device is fully powered on (not in *sleep* state or *stand-by* state). Performing any of the following actions will insure that the CS5460A is operating in the *active* state:

1) Power on the CS5460A. (Or if the device is already powered on, recycle the power.)

2) Hardware Reset

3) Software Reset

In addition to the three actions listed above, note that if the device is in *sleep* state or in *stand-by* state, the action of waking up the device out of *sleep* state or *stand-by* state (by issuing the Power-Up/Halt command) will also insure that the device is set into *active* state. But remember that in order to send the Power-Up/Halt command to the device, the user must be sure that the serial port has already been (or is still) initialized. Therefore, if there are situations in which the user wants to wake the CS5460A out of *sleep* state or *stand-by* state, successful wake-up of the device will be insured if the serial port initialization sequence is strobed to the device, prior to strobing the Power-Up/Halt Command.

For a description of the *sleep* power state and the *stand-by* power state, see the Power Down Command, located in Section 3.1.

4. FUNCTIONAL DESCRIPTION

4.1 Pulse-Rate Output

As an alternative to reading the energy through the serial port, the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins provide a simple interface with which signed energy can be accumulated. Each $\overline{\text{EOUT}}$ pulse represents a predetermined magnitude of energy. The magnitude of energy represented in one pulse can be varied by adjusting the value in the Pulse-Rate Register. Corresponding pulses on the $\overline{\text{EDIR}}$ output pin signify that the sign of the energy is negative. Note that these pulses are not influenced by the value of the Cycle-Count Register, and they have no reliance on the computation cycle, described earlier. With MCLK = 4.096 MHz, K = 1, the pulses will have an average frequency (in Hz) equal to the frequency setting in the Pulse Rate Register when the input signals into the voltage and current channels cause full-scale readings in the Instantaneous Voltage and Current Registers. When MCLK/K is not equal to 4.096 MHz, the user should scale the pulse-rate that one would expect to get with MCLK/K = 4.096 MHz by a factor of 4.096 MHz / (MCLK / K) to get the actual output pulse-rate.

EXAMPLE #1: Suppose that we want the pulse-frequency on the $\overline{\text{EOUT}}$ pin to be 'IR' = 100 pulses per second (100 Hz) when the RMS-voltage/RMS-current levels on the power line are 220 V and 15 A respectively, noting that the maximum rated levels on the power line are 250 V and 20 A. We also assume that we have calibrated the CS5460A voltage/current channel inputs such that a DC voltage level of 250 mV across the voltage/current channels will cause full-scale readings of 1.0 in the CS5460A Instantaneous Voltage and Current Registers as well as in the RMS-Voltage and RMS-Current Registers. We want to find out what frequency value we should put into the CS5460A's Pulse-Rate Register (call this value 'PR') in order to satisfy this requirement. Our first step is to set the voltage and current sensor gain

constants, K_V and K_I, such that there will be acceptable input voltage levels on the inputs when the power line voltage and current levels are at the maximum values of 250 V and 20 A, respectively. We need to calculate K_V and K_I in order to determine the appropriate ratios of the voltage/current transformers and/or shunt resistor values to use in the front-end voltage/current sensor networks.

We assume here that we are dealing with a sinusoidal AC power signal. For a sinewave, the largest RMS value that can be accurately measured (without over-driving the inputs) will register at ~0.7071 of the maximum DC input level. Since power signals are often not perfectly sinusoidal in real-world situations, and to provide for some over-range capability, we will set the RMS Voltage Register and RMS Current Register to measure at 0.6 when the RMS-values of the line-voltage and line-current levels are at 250 V and 20 A. Therefore, when the RMS registers measure 0.6, the voltage level at the inputs will be 0.6 x 250 mV = 150 mV. We now find our sensor gain constants, K_V and K_I, by demanding that the voltage and current channel inputs should be at 150 mV RMS when the power line voltage and current are at the maximum values of 250 V and 20 A.

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ohms

These sensor gain constants can help determine the ratios of the transformer or resistor-divider sensor networks. We now use these sensor gain constants to calculate what the input voltage levels will be on the CS5460A inputs when the line-voltage and line-current are at 220 V and 15 A. We call these values V_{Vnom} and V_{Inom}.

V_{Vnom} = K_V * 220 V = 132 mV

V_{Inom} = K_I * 15 A = 112.5 mV

The pulse rate on $\overline{\text{EOUT}}$ will be at 'PR' pulses per second (Hz) when the RMS-levels of voltage/current inputs are at 250 mV. When the voltage/cur-

rent inputs are set at V_{Vnom} and V_{Inom}, we want the pulse rate to be at 'IR' = 100 pulses per second. IR will be some percentage of PR. The percentage is defined by the ratios of $V_{Vnom}/250$ mV and $V_{Inom}/250$ mV with the following formula:

$$\text{PulseRate} = \text{IR} = \text{PR} \cdot \frac{V_{Vnom}}{250\text{mV}} \cdot \frac{V_{Inom}}{250\text{mV}}$$

We can rearrange the above equation and solve for PR. This is the value that we put into the Pulse-Rate Register.

$$\text{PR} = \frac{\text{IR}}{\dfrac{V_{Vnom}}{250\text{mV}} \times \dfrac{V_{Inom}}{250\text{mV}}} = \frac{100\text{Hz}}{\dfrac{132\text{mV}}{250\text{mV}} \times \dfrac{112.5\text{mV}}{250\text{mV}}}$$

Therefore we set the Pulse-Rate Register to ~420.875 Hz. Therefore, the Pulse-Rate Register would be set to 0x00349C.

The above equation is valid when current channel is set to x10 gain. If current channel gain is set to x50, then the equation becomes:

$$\text{PR} = \frac{\text{IR}}{\dfrac{V_{Vnom}}{250\text{mV}} \times \dfrac{V_{Inom}}{50\text{mV}}}$$

where it is assumed that the current channel has been calibrated such that the Instantaneous Current Register will read at full-scale when the input voltage across the IIN+ and IIN- inputs is 50 mV (DC).

EXAMPLE #2: Suppose that instead of being given a desired frequency of pulses per second to be issued at a specific voltage/current level, we are given a desired number of pulses per unit energy to be present at $\overline{\text{EOUT}}$, given that the maximum line-voltage is at 250 V (RMS) and the maximum line-current is at 20 A (RMS). For example, suppose that the required number of pulses per kW-hr is specified to be 500 pulses/kW-hr. In such a situ-

ation, the nominal line voltage and current do not determine the appropriate pulse-rate setting. Instead, the *maximum* line-voltage and line-current levels must be considered. We use the given maximum line-voltage and line-current levels to determine K_V and K_I as previously described to get:

K_V = 150 mV / 250 V = 0.0006

K_I = 150 mV / 20 A = 0.0075 Ohms

where we again have calculated our sensor gains such that the maximum line-voltage and line-current levels will measure as 0.6 in the RMS Voltage Register and RMS Current Register.

We can now calculate the required Pulse-Rate Register setting by using the following equation:

$$\text{PR} = 500\frac{\text{pulses}}{\text{kW} \cdot \text{hr}} \cdot \frac{1\text{hr}}{3600\text{s}} \cdot \frac{1\text{kW}}{1000\text{W}} \cdot \frac{250\text{mV}}{K_V} \cdot \frac{250\text{mV}}{K_I}$$

Therefore PR = ~1.929 Hz.

Note that the Pulse-Rate Register cannot be set to a frequency of exact 1.929 Hz. The closest setting that the Pulse-Rate Register can obtain is 0x00003E = 1.9375 Hz. To improve the accuracy, either gain register can be programmed to correct for the round-off error in PR. This value would be calculated as

$$\text{Ign or Vgn} = \frac{\text{PR}}{1.929} \cong 1.00441 = 0x404830$$

In the last example, suppose that the designer must use a value for MCLK/K of 3.05856MHz. When MCLK/K is not equal to 4.096MHz, the result for 'PR' that is calculated for the Pulse-Rate Register must be scaled by a correction factor of: 4.096MHz / (MCLK/K). In this case we would scale the result by 4.096/3.05856 to get a final PR result of ~2.583 Hz.

4.2 Pulse Output for Normal Format, Stepper Motor Format and Mechanical Counter Format

The duration and shape of the pulse outputs at the $\overline{EOUT}$ and $\overline{EDIR}$ pins can be set for three different output formats. The default setting is for *normal* output pulse format. When the pulse is set to either of the other two formats, the time duration and/or the relative timing of the $\overline{EOUT}$ and $\overline{EDIR}$ pulses is increased/varied such that the pulses can drive either an electro-mechanical counter or a stepper motor. The $\overline{EOUT}$ and $\overline{EDIR}$ output pins are capable of driving certain low-voltage/low-power counters/stepper motors directly. This depends on the drive current and voltage level requirements of the counter/motor. The ability to set the pulse output format to one of the three available formats is controlled by setting certain bits in the Control Register.

4.2.1 Normal Format

Referring to the description of the Control Register in *Section 5., REGISTER DESCRIPTION*, if both the MECH and STEP bits are set to '0', the $\overline{EOUT}$ and $\overline{EDIR}$ pulse output format at the $\overline{EOUT}$ and $\overline{EDIR}$ pins is illustrated in Figure 10. These are active-low pulses with very short duration. The pulse duration is an integer multiple of DCLK cycles, approximately equal to 1/16 of the period of the contents of the Pulse-Rate Register. However for Pulse-Rate Register settings less than the sampling rate (which is DCLK/1024), the pulse duration will remain at a constant duration, which is equal to the duration of the pulses when the Pulse-Rate Register is set to DCLK/1024. The maximum pulse frequency from the $\overline{EOUT}$ pin is therefore DCLK/16. When energy is positive, $\overline{EDIR}$ is always high. When energy is negative, $\overline{EDIR}$ has the same output as $\overline{EOUT}$. When MCLK/K = DCLK is not equal to 4.096 MHz, the user can predict the pulse-rate by first calculating what the pulse-rate would be if a 4.096MHz crystal is used (with K=1) and then scaling the result by a factor of (MCLK/K) / 4.096MHz.

In Normal pulse output format, the pulses may be sent out in "bursts" depending on the value of the Pulse-Rate Register, and also depending on the amount of energy that was registered by the CS5460 over the most recent A/D sampling period, which is 1 / [(MCLK/K) / 1024]. A running total of the energy accumulation is maintained in an internal register inside the CS5460A. If the amount of energy that has accumulated in this register over the most recent A/D sampling period is equal to or greater than the amount of energy that is represented by one pulse, the CS5460A will issue a "burst" of one or more pulses on $\overline{EOUT}$ (and also possibly on $\overline{EDIR}$). The CS5460A will issue as many pulses as are necessary to reduce the running energy accumulation value in this register to a value that is less than the energy represented in one pulse. If the amount of energy that has been registered over the most recent sampling period is large enough that it cannot be expressed with only one pulse, then a

$$t = \frac{\text{Pulse-Rate Register Period}}{16} = \frac{n}{2^x (MCLK / K)} \quad \text{for Integer } n$$
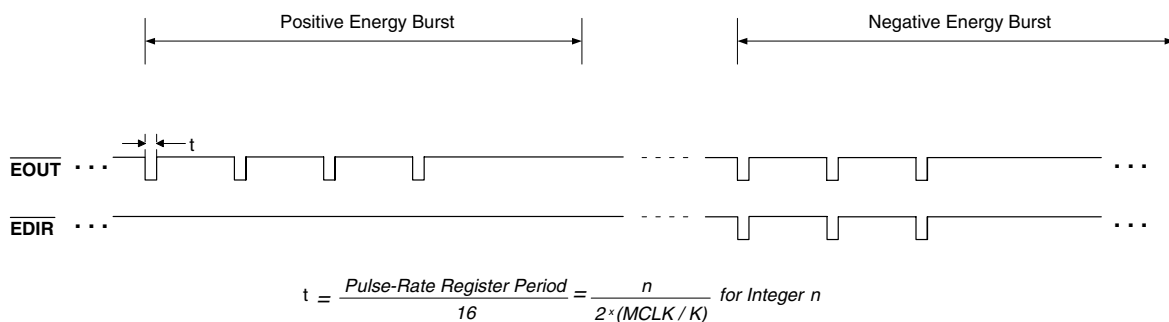
Figure 10. Time-plot representation of pulse output for a typical burst of pulses (Normal Format)
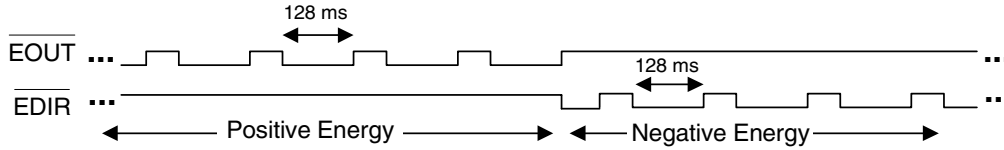
Figure 11. Mechanical Counter Format on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

burst of pulses will be issued, possibly followed by a period of time during which there will be no pulses, until the next A/D sampling period occurs. After the pulse or pulses are issued, a certain residual amount of energy may be left over in this internal energy accumulation register, which is always less (in magnitude) than the amount of energy represented by one pulse. In this situation, the residual energy is not lost or discarded, but rather it is maintained and added to the energy that is accumulated during the next update period. The amount of residual energy that can be left over becomes larger as the Pulse-Rate Register is set to lower and lower values, because lower Pulse-Rate Register values correspond to a higher amount of energy per pulse (for a given calibration).

4.2.2 Mechanical Counter Format

Setting the MECH bit in the Control Register to '1' and the STEP bit to '0' enables wide-stepping pulses for mechanical counters and similar discrete counter instruments. In this format, active-low pulses are 128 ms wide when using a 4.096 MHz crystal and K=1. When energy is positive, the pulses appear on $\overline{\text{EOUT}}$. When energy is negative, pulses appear on $\overline{\text{EDIR}}$. It is up to the user to insure that pulses will not occur at a rate faster than the 128 ms pulse duration, or faster than the mechani-

cal counter can accommodate. This is done by verifying that the Pulse-Rate Register is set to an appropriate value. Because the duration of each pulse is set to 128 ms, the maximum output pulse frequency is limited to ~7.8 Hz (for MCLK/K = 4.096 MHz). For values of MCLK / K different than 4.096 MHz, the duration of one pulse is (128 * 4.096 MHz)/(MCLK / K) milliseconds. See Figure 11 for a diagram of the typical pulse output.

4.2.3 Stepper Motor Format

Setting the STEP bit in the Control Register to '1' and the MECH bit to '0' transforms the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins into two stepper motor phase outputs. When an energy pulse occurs, one of the outputs changes state. When the next energy pulse occurs, the other output changes state. The direction the motor will rotate is determined by the order of the state changes. When energy is positive, $\overline{\text{EOUT}}$ will lead $\overline{\text{EDIR}}$. When energy is negative, $\overline{\text{EDIR}}$ will lead $\overline{\text{EOUT}}$. See Figure 12.

4.3 Auto-Boot Mode Using EEPROM

The CS5460A has a MODE pin. When the MODE pin is set to logic low, the CS5460A is in normal operating mode, called *host mode*. This mode denotes the normal operation of the part, that has been described so far. But when this pin is set to logic
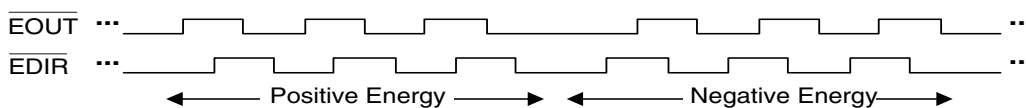
Figure 12. Stepper Motor Format on $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$

high, the CS5460A *auto-boot mode* is enabled. In auto-boot mode, the CS5460A is configured to request a memory download from an external serial EEPROM. The download sequence is initiated by driving the $\overline{\text{RESET}}$ pin to logic high. Auto-Boot mode allows the CS5460A to operate without the need for a microcontroller. Note that if the MODE pin is left unconnected, it will default to logic low because of an internal pull-down on the pin.

4.3.1 Auto-Boot Configuration

Figure 13 shows the typical connections between the CS5460A and a serial EEPROM for proper auto-boot operation. In this mode, $\overline{\text{CS}}$ and SCLK are driven outputs. SDO is always an output. During the auto-boot sequence, the CS5460A drives $\overline{\text{CS}}$ low, provides a clock output on SCLK, and drives out-commands on SDO. It receives the EEPROM data on SDI. The serial EEPROM must be programmed with the user-specified commands and register data that will be used by the CS5460A to change any of the default register values (if desired) and begin conversions.

Figure 13 also shows the external connections that would be made to a calibrator device, such as a PC

or custom calibration board. When the metering system is installed, the calibrator would be used to control calibration and/or to program user-specified commands and calibration values into the EEPROM. The user-specified commands/data will determine the CS5460A's exact operation, when the auto-boot initialization sequence is running. Any of the valid commands can be used.

4.3.2 Auto-Boot Data for EEPROM

This section illustrates what a typical set of code would look like for an auto-boot sequence. This code is what would be written into the EEPROM by the user. In the sequence below, the EEPROM is programmed so that it will first send out commands that write calibration values to the calibration registers inside the CS5460A, then it will enable the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ functionality and set a Pulse-Rate Register value. The LSD bit in the Mask Register is un-masked (this is described in section 4.3.4). Finally, the EEPROM code will initiate continuous conversions, and select one of the alternate pulse-output formats (e.g., set the MECH bit in the Control Register). The serial data for such a sequence is shown below in single-byte hexidecimal notation:
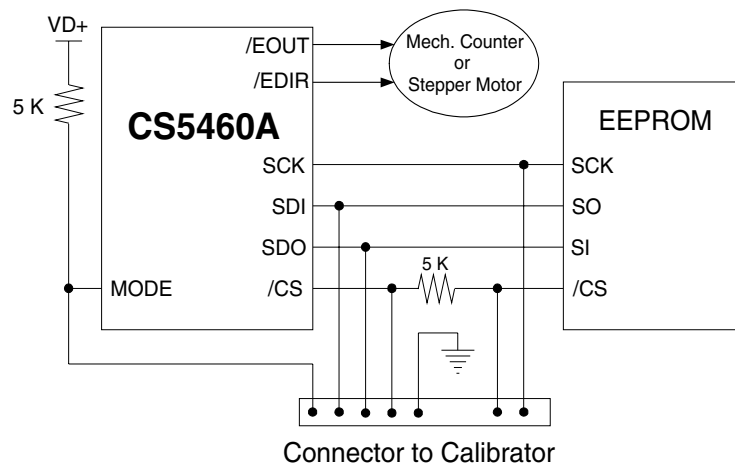
Figure 13. Typical Interface of EEPROM to CS5460A

40 00 00 61   ;In Configuration Register, turn high-pass filters on, set K=1.

44 7F C4 A9   ;Write value of 0x7FC4A9 to Current Gain Register.

46 7F B2 53   ;Write value of 0xFFB253 to DC Voltage Offset Register.

4C 00 00 14   ;Set Pulse Rate Register to 0.625 Hz.

74 00 00 04   ;Unmask bit #2 ("LSD" bit in the Mask Register).

E8   ;Start continuous conversions

78 00 01 40   ;Write STOP bit to Control Register, to terminate auto-boot initialization sequence, and set the $\overline{\text{EOUT}}$ pulse output to Mechanical Counter Format.

This data from the EEPROM will drive the SDI pin of the CS5460A during the auto-boot sequence.

The following sequence of user-controlled events will cause the CS5460A to execute the auto-boot mode initialization sequence: (A simple timing diagram for this sequence is shown below in Figure 14.) After the CS5460A has been powered on and has been allowed to initialize, if the MODE pin is set to logic high (or if the MODE pin was set/tied to logic high before/during power on), then

changing the $\overline{\text{RESET}}$ pin from active state to inactive state (low to high) will cause the CS5460A to drive $\overline{\text{CS}}$ pin low, and then issue the standard block read command out of the SDO line. Then the CS5460A will continue to issue SCLKs, to accept data from the EEPROM. A more detailed timing diagram can be found in the *SWITCHING CHARACTERISTICS* section of this data sheet.

4.3.3 Which EEPROMs Can Be Used?

Several industry-standard serial EEPROMs that will successfully run auto-boot with the CS5460A are listed below:

- Atmel   AT25010
                         AT25020
                         AT25040

- National Semiconductor   NM25C040M8
                             NM25020M8

- Xicor   X25040SI

These types of serial EEPROMs expect a specific 8-bit command word (00000011) in order to perform a memory download. The CS5460A has been hardware programmed to transmit this 8-bit command word to the EEPROM at the beginning of the auto-boot sequence.

The auto-boot sequence is terminated by writing a '1' to the STOP bit in the CS5460A's Control Register. This action is performed as the last command in the EEPROM command sequence. Once this
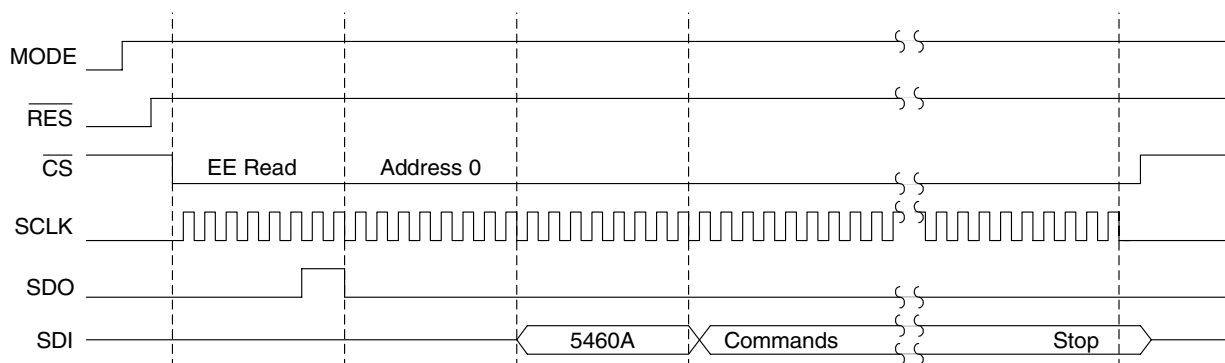
Figure 14. Timing Diagram for Auto-Boot Sequence

event occurs, SCLK stops, and $\overline{CS}$ rises, thereby reducing power consumed by the EEPROM. When the CS5460A is commanded by the EEPROM to perform a certain operation, it will continue to execute that operation after the STOP bit has been received. In the above example, the 'continuous conversion' command (0xE8) is issued from the EEPROM, and therefore the CS5460A will continue performing conversions even after the STOP bit is written.

4.3.4 Auto-Boot Reset during Brown-Out/Black-Out Conditions

The power line that is to be metered may enter a black-out or brown-out condition at certain times, due to problems at the power plant or other environmental conditions (ground fault, electrical storms, etc.) In such conditions, it is important for the CS5460A to be able to gracefully reset, so that it can continue normal metering operations once the power in the line is restored. When the CS5460A is controlled by a microcontroller, the microcontroller is usually programmed (by the user) to handle these power-fail-reset situations. In the case of auto-boot, the CS5460A is basically left on its own to reset itself, whenever line power is restored. Figure 15 shows a reasonably reliable way to configure the CS5460A's $\overline{RESET}$ and $\overline{INT}$ pins so that CS5460A to restart the Auto-Boot sequence after a brown-out or black-out condition. This configuration employs a diode, a resistor, and a capacitor on the $\overline{RESET}$ pin in attempt to allow the CS5460A to reboot after a sudden loss of power, followed by a reinstatement of power. This circuitry often helps the CS5460A to perform a smooth, graceful reset/reboot *before* it attempts to continue with A/D conversions.

Note in the above auto-boot example code set, that the LSD bit is un-masked, in order to cause a high-to-low transition on the $\overline{INT}$ pin whenever the PFMON threshold is reached on the PFMON pin. If a power supply loss condition is sensed on PFMON, then the $\overline{INT}$ pin is asserted to low, which allows the BAT85 diode to quickly drain the charge
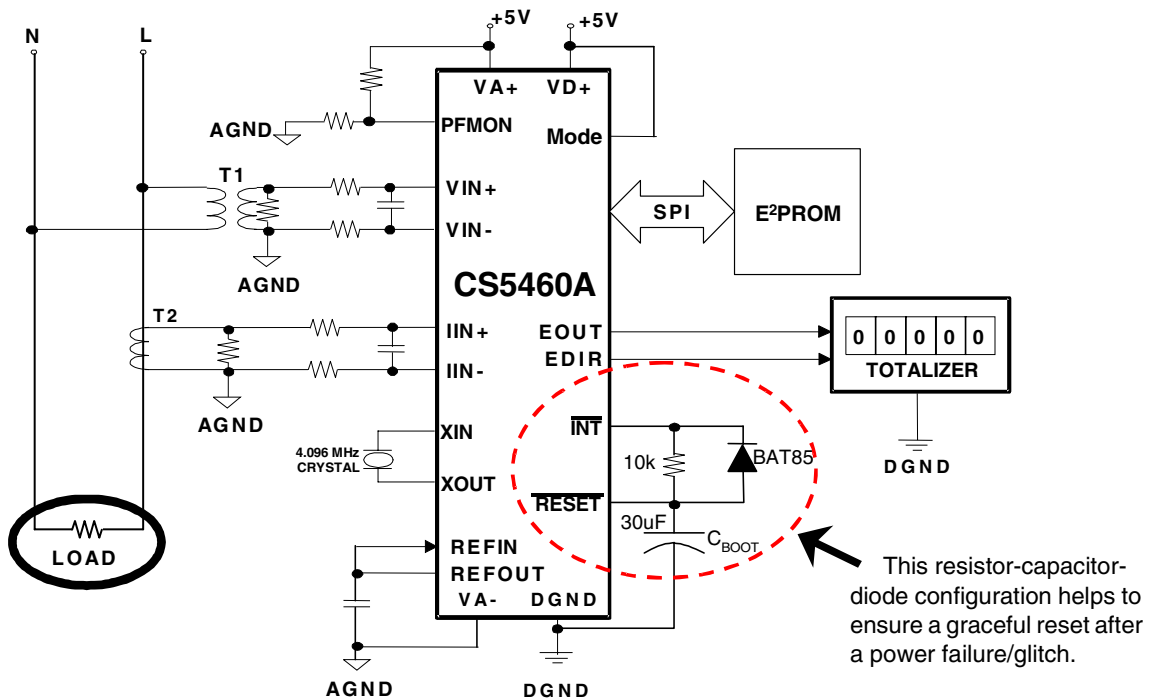
Figure 15. CS5460A Auto-Boot Configuration: Automatic Restart After Power Failure

on C_{BOOT}. But whenever the +5V power is restored, the resistor-capacitor network will force $\overline{RESET}$ to recharge slowly. The slow rise time on the $\overline{RESET}$ pin allows the oscillator circuitry and the internal reference circuitry enough time to stabilize before the CS5460A commences with the auto-boot sequence. This will allow the CS5460A to resume its normal metering operations after the power is restored. (User must provide suitable resistor divider configuration on the PFMON pin, see Figure 15.) This configuration is does not guarantee that the CS5460A will reset gracefully when it is exposed to *any* sudden disturbance in power.

4.4 Interrupt and Watchdog Timer

4.4.1 Interrupt

The $\overline{INT}$ pin is used to indicate that an event has taken place in the converter that needs attention. These events inform the system about operation conditions and internal error conditions. The $\overline{INT}$ signal is created by combining the Status Register with the Mask Register. Whenever a bit in the Status Register becomes active, and the corresponding bit in the Mask Register is a logic 1, the $\overline{INT}$ signal becomes active. The interrupt condition is cleared when the bits of the Status Register are returned to their inactive state.

4.4.1.1 Clearing the Status Register

Unlike the other registers, the bits in the Status Register can only be cleared (set to logic 0). When a word is written to the Status Register, any 1s in the word will cause the corresponding bits in the Status Register to be cleared. The other bits of the Status Register remain unchanged. This allows the clearing of particular bits in the register without having to know the state of the other bits. This mechanism is designed to facilitate handshaking and to minimize the risk of losing events that haven't been processed yet.

4.4.1.2 Typical use of the $\overline{INT}$ pin

The steps below show how interrupts can be handled.

- *Initialization*:

    Step I0 - All Status bits are cleared by writing FFFFFF (Hex) into the Status Register.

    Step I1 - The conditional bits which will be used to generate interrupts are then written to logic 1 in the Mask Register.

    Step I3 - Enable interrupts.

- *Interrupt Handler Routine*:

    Step H0 - Read the Status Register.

    Step H1 - Disable all interrupts.

    Step H2 - Branch to the proper interrupt service routine.

    Step H3 - Clear the Status Register by writing back the value read in step H0.

    Step H4 - Re-enable interrupts.

    Step H5 - Return from interrupt service routine.

    This handshaking procedure insures that any new interrupts activated between steps H0 and H3 are not lost (cleared) by step H3.

4.4.1.3 $\overline{INT}$ Active State

The behavior of the $\overline{INT}$ pin is controlled by the SI1 and SI0 bits of the Configuration Register. The pin can be active low (default), active high, active on a return to logic 0 (pulse-low), or active on a return to logic 1 (pulse-high). If the interrupt output signal format is set for either pulse-high or pulse-low, note that the duration of the $\overline{INT}$ pulse will be at least one DCLK cycle (DCLK = MCLK / K) although in some cases the pulse may last for 2 DCLK cycles.

4.4.1.4 Exceptions

The $\overline{IC}$ (Invalid Command) bit of the Status Register can only be cleared by performing the port ini-

tialization sequence. This is also the only Status Register bit that is active low.

To properly clear the WDT (Watch Dog Timer) bit of the Status Register, first read the Energy Register, then clear the bit in the Status Register.

4.4.2 Watch Dog Timer

The Watch Dog Timer (WDT) is provided as means of alerting the system that there is a potential breakdown in communication with the micro-controller. By allowing the WDT to cause an interrupt, a controller can be brought back, from some unknown code space, into the proper code for processing the data created by the converter. The time-out is preprogrammed to approximately 5 seconds. The countdown restarts each time the Energy Register is read. Under typical situations, the Energy Register is read every second. As a result, the WDT will not time out. Other applications that use the watchdog timer will need to ensure that the Energy Register is read at least once in every 5 second span.

4.5 Oscillator Characteristics

XIN and XOUT are the input and output, respectively, of an inverting amplifier to provide oscillation and can be configured as an on-chip oscillator, as shown in Figure 16. The oscillator circuit is designed to work with a quartz crystal or a ceramic resonator. To reduce circuit cost, two load capacitors C1 are integrated in the device, one between XIN and DGND, one between XOUT and DGND. Lead lengths should be minimized to reduce stray capacitance. With these load capacitors, the oscillator circuit is capable of oscillation up to 20 MHz. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

The CS5460A can be driven by a clock ranging from 2.5 to 20 MHz. The user must appropriately set the K divider value such that the internal DCLK will run somewhere between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the Configuration Register. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, then DCLK is 3 MHz, which is a valid value for DCLK. Note that if the K[3:0] bits are all set to zero, the value of the K divider value is 16.

4.6 Analog Inputs

The CS5460A accommodates a full-scale differential voltage range of ±250 mV on both input channels. (If the PGA setting on the current channel is set for the 50x gain setting instead of the 10x gain setting, then the full-scale range on the current channel reduces to ±50mV.) System calibration can be used to increase or decrease the full scale span of the converter as long as the calibration register values stay within the limits specified. See *Section 4.8, Calibration*, for more details.

4.7 Voltage Reference

The CS5460A is specified for operation with a +2.5 V reference between the VREFIN and VA-pins. The converter includes an internal 2.5 V reference (60 ppm/°C drift) that can be used by con-
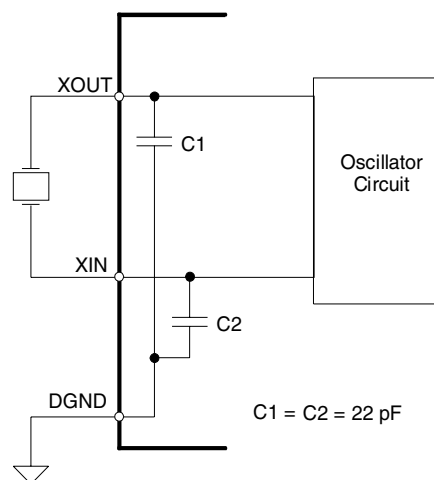
Figure 16. Oscillator Connection

necting the VREFOUT pin to the VREFIN pin of the device. If higher accuracy/stability is required, an external reference can be used.

4.8 Calibration

4.8.1 Overview of Calibration Process

The CS5460A offers digital calibration. The user determines which calibration sequence will be executed by setting/clearing one or more of the 8 bits in the *calibration command* word. For both channels, there are calibration sequences for both AC and DC purposes. Regardless of whether an AC or DC calibration sequence is desired, there are two basic types of calibration: system offset and system gain. When the calibration sequences are being performed by the CS5460A, the user must supply the input calibration signals to the "+" and "-" pins of the voltage-/current-channel inputs. These input calibration signals represent full-scale levels (for gain calibrations) and ground input levels (for offset calibrations).

The AC and DC calibration sequences are different. Depending on the user's specific metering application and accuracy requirements, some or all of the calibration sequences may not be executed by the user. (This is discussed in more detail in the following discussion). In order to help the reader to better understand the functionality of each calibration sequence, we first define the various calibration registers within the CS5460A.

4.8.2 The Calibration Registers

Refer to Figure 3 and Figure 24.

DC Voltage Offset Register and DC Current Offset Register - Store additive correction values that are used to correct for DC offsets which may be present on the voltage/current channels within the entire meter system. These registers are updated by the CS5460A after a DC offset calibration sequence has been executed.

Voltage Gain Register and Current Gain Register - Store the multiplicative correction values determined by the full-scale gain calibration signals that are applied (by the user) to the meter's voltage/current channels. These registers are updated by the CS5460A after either an AC or DC gain calibration sequence has been executed.

AC Voltage Offset Register and AC Current Offset Register - Store additive offset correction values that are used to correct for AC offsets which may be created on the voltage/current channels within the entire meter system. Although a noise signal may have an average value of zero [no DC offset] the noise may still have a non-zero rms value, which can add an undesirable offset in the CS5460A's Irms and Vrms results. These registers are updated by the CS5460A after an AC offset calibration sequence has been executed.

Referring to Figure 3, one should note that the AC offset registers affect the output results differently than the DC offset registers. The DC offset values are applied to the voltage/current signals very early in the signal path; the DC offset register value affects all CS5460A results. This is not true for the AC offset correction. The AC offset registers only affect the results of the rms-voltage/rms-current calculations.

Referring to Figure 3, the reader should note that there are separate calibration registers for the AC and DC offset corrections (for each channel). This is not true for gain corrections, as there is only one gain register per channel--AC and DC gain calibration results are stored in the same register. The results in the gain registers reflect either the AC or DC gain calibration results, whichever was performed most recently. Therefore, both a DC and AC offset can be applied to a channel at the same time, but only one gain calibration can be applied to each channel. The user must decide which type of gain calibration will be used: AC or DC, but not both.

To summarize, for both the voltage channel and the current channel, while the AC offset calibration sequence performs an entirely different function than the DC offset calibration sequence, the AC gain and DC gain calibration sequences perform the same function (but they accomplish the function using different techniques).

Since both the voltage and current channels have separate offset and gain registers associated with them, system offset or system gain can be performed on either channel without the calibration results from one channel affecting the other.

4.8.3 Calibration Sequence

1. The CS5460A must be operating in its *active* state, and ready to accept valid commands via the SPI interface, before a calibration sequence can be executed. The user will probably also want to clear the 'DRDY' bit in the Status Register.

2. The user should then apply appropriate calibration signal(s) to the "+" and "-" signals of the voltage/current channel input pairs. (The appropriate calibration signals for each type of calibration sequence are discussed next, in Sections 4.8.4 and 4.8.5.)

3. Next the user should send the 8-bit calibration command to the CS5460A serial interface. The calibration command is an 8-bit command. Various bits within this command specify the exact type of calibration that is to be performed (e.g., AC gain cal for voltage channel, DC offset cal for current channel, etc.) The user must set or clear these bits in the calibration command to correctly specify exactly which calibration sequence is to be executed.

4. After the CS5460A has finished running the desired internal calibration sequence and has stored the updated calibration results in the appropriate calibration registers, the DRDY bit is set (assuming that it had previously been cleared) in the Status Register to indicate that the calibration sequence has been completed. If desired, the results of the

calibration can now be read from the appropriate gain/offset registers, via the serial port.

Note that when the calibration command is sent to the CS5460A by the user, the device must *not* be performing A/D conversions (in either of the two acquisitions modes). If the CS5460A is running A/D conversions/computations in the 'continuous computation cycle' acquisition mode (C=1), the user must first issue the Power-Up/Halt Command to terminate A/D conversions/computations. If the CS5460A is running A/D conversions/computations in the 'single computation cycle' acquisition mode (C=0), then the user must either issue the Power-Up/Halt Command, or else wait until the single computation cycle has completed, before executing any calibration sequence. The calibration sequences will not run if the CS5460A is running in either of the two available acquisition modes.

4.8.4 Calibration Signal Input Level

For both the voltage and current channels, the differential voltage levels of the user-provided calibration signals must be within the specified voltage input limits (refer to "Differential Input Voltage Range" in *Section 1., Characteristics and Specifications*). For the voltage channel the peak differential voltage level can never be more than ±250 mV. The same is true for the current channel if the current channel input PGA is set for 10x gain. If the user sets the current channel's PGA gain to 50x, then the current channel's input limits are ±50 mV.

Note that for the AC/DC gain calibrations, there is an absolute limit on the RMS/DC voltage levels (respectively) that are selected for the voltage/current channel gain calibration input signals. The maximum value that the gain register can attain is 4. Therefore, for either channel, if the voltage level of a gain calibration input signal is low enough that it causes the CS5460A to attempt to set either gain register higher than 4, the gain calibration result will be invalid, and after this occurs, all CS5460A

results obtained when the part is running A/D conversions will be invalid.

4.8.5 Calibration Signal Frequency

The frequency of the calibration signals must be less than 1 kHz (assume MCLK/K = 4.096 MHz and K = 1). Optimally, the frequency of the calibration signal will be at the same frequency as the fundamental power line frequency of the power system that is to be metered.

4.8.6 Input Configurations for Calibrations

Figure 17 shows the basic setup for gain calibration. If a DC gain calibration is desired, the user must apply a *positive* DC voltage level. The user should set the value of this voltage such that it truly represents the *absolute maximum* peak instantaneous voltage level that needs to be measured across the inputs (including the maximum over-range level that must be accurately measured). In other words, the input signal must be a positive DC voltage level that represents the desired absolute peak full-scale value. However, in many practical power metering situations, an AC signal is preferred over a DC signal to calibrate the gain. If the user decides to perform AC gain calibration instead of DC, the user should apply an AC reference signal that is set to the desired maximum RMS level. Because the voltage/current waveforms that must be measured in most power systems are approximately sinusoidal in nature, the designer/user will most likely need to set the RMS levels of the AC gain calibration input signals such that they will be significantly lower than the voltage/current channel's maximum DC voltage input level. This must be done in order to avoid the possibility that the peak values of the AC waveforms that are to be measured will not register a value that would be outside the available output code range of the voltage/current A/D converters. For example, on the voltage channel, if the Voltage Gain Register is set to it's default power-on value of 1 before calibration, then the largest pure sinusoidal wave-

form that can be used in AC calibration is one whose RMS-value is ~0.7071 of the value of the voltage channel's peak DC input voltage value of ±250 mV. Thus the maximum value of the input sinusoid would be ~176.78mV (rms). But in many practical power metering situations, the user will probably want to reduce the RMS voltage input level of the AC gain calibration signal even further, to allow for some over-ranging capability. A typical sinusoidal calibration value which allows for reasonable over-range margin would be 0.6 of the voltage/current channel's maximum input voltage level. For the voltage channel, such a sine-wave would have a value of 0.6 x 250mV = 150mV (rms).

For the offset calibrations, there is no difference between the AC and DC calibration signals that must be supplied by the user: The user should simply connect the "+" and "-' pins of the voltage/current channels to their ground reference level. (See Figure 18.)

The user should not try to run both an offset and gain calibration at the same time. This will cause undesirable calibration results.
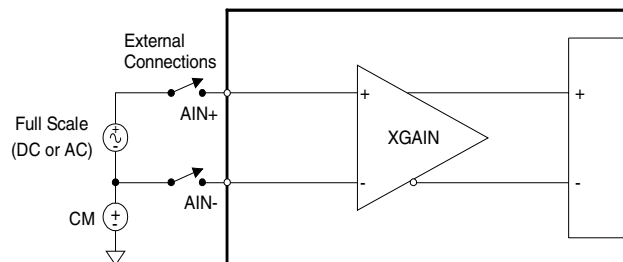
Figure 17. System Calibration of Gain.
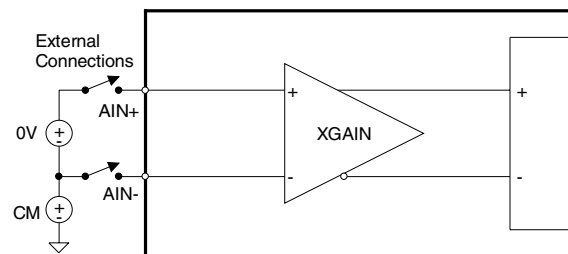
Figure 18. System Calibration of Offset.

4.8.7 Description of Calibration Algorithms

The computational flow of the CS5460A's AC and DC gain/offset calibration sequences are illustrated in Figure 19. This figure applies to both the voltage channel and the current channel. The following descriptions of calibration sequences will focus on the voltage channel, but apply equally to the current channel.

Note: For proper calibration, it is assumed that the value of the Voltage/Current Gain Registers are set to default (1.0) before running the *gain* calibration(s), and the value in the AC and DC *Offset* Registers is set to default (0) before running calibrations. This can be accomplished by a software or hardware reset of the device. The values in the voltage/current calibration registers *do* affect the results of the calibration sequences.

4.8.7.1 AC Offset Calibration Sequence

The idea of the AC offset calibration is to obtain an offset value that reflects the square of the RMS output level when the inputs are grounded. During normal operation, when the CS5460A is calculating the latest result for the RMS Voltage Register, this AC offset register value will be subtracted from the square of each successive voltage sample in order to nullify the AC offset that may be inherent in the voltage-channel signal path. Note that the value in the AC offset register is proportional to the *square* of the AC offset. First, the inputs should be grounded by the user, and then the AC offset calibration command should be sent to the CS5460A. When the AC offset calibration sequence is initiated by the user, a valid RMS Voltage Register value is acquired and squared. This value is then subtracted from the square of each voltage sample that comes through the RMS data path. See Figure 19.

4.8.7.2 DC Offset Calibration Sequence

The DC Voltage Offset Register holds the negative of the simple average of N samples taken while the DC voltage offset calibration was executed. The inputs should be grounded during DC offset calibration. The DC offset value is added to the signal path to nullify the DC offset in the system.

4.8.7.3 AC Gain Calibration Sequence

The AC voltage gain calibration algorithm attempts to adjust the Voltage Gain Register value such that the calibration reference signal level presented at the voltage inputs will result in a value of 0.6 in the RMS Voltage Register. The rms level of the calibration signal must be determined by the user. During AC voltage gain calibration, the value in the RMS Voltage Register is divided into 0.6. This result is the AC gain calibration result stored in the Voltage Gain Register.
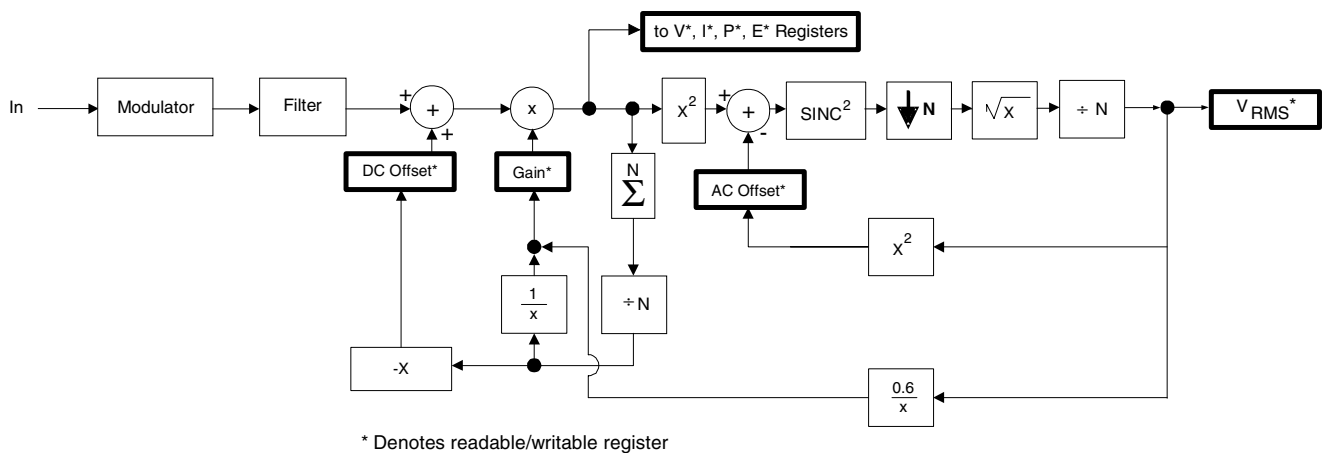
Figure 19. Calibration Data Flow

Two examples of AC calibration and the resulting shift in the digital output codes of the channel's instantaneous data registers are shown in Figures 20 and 21. Note Figure 21 shows that a positive (or negative) DC level signal can be used even though an AC gain calibration is being executed. However, an AC signal *cannot* be used if the DC gain calibration sequence is going to be executed.

4.8.7.4 DC Gain Calibration Sequence

Based on the level of the positive DC user-provided calibration voltage that should be applied across the "+' and "-'' inputs, the CS5460A determines the DC Voltage Gain Register value by averaging the Instantaneous Voltage Register's output signal values over one computation cycle (N samples) and then dividing this average into 1. Therefore, after the DC voltage gain calibration has been executed, the Instantaneous Voltage Register will read at full-scale whenever the DC level of the input signal is equal to the level of the DC calibration signal that was applied to the voltage channel inputs during

the DC gain calibration. For example, if a +230 mV DC signal is applied to the voltage channel inputs during the DC gain calibration for the current channel, then the Instantaneous Voltage Register will measure at unity whenever a 230 mV DC level is applied to the voltage channel inputs. See Figure 22. The reader should compare Figure 21 to Figure 22 to see the difference between the AC and DC calibration gain calibration sequences.

4.8.8 Duration of Calibration Sequence

The value of the Cycle Count Register (N) determines the number of conversions that will be performed by the CS5460A during a given calibration sequence. For DC offset/gain calibrations, the calibration sequence always takes at least N + 30 conversion cycles to complete. For AC offset/gain calibrations, the calibration sequence takes at least 6N + 30 A/D conversion cycles to complete, (about 6 computation cycles). If N is increased by the user, the accuracy of calibration results will increase.
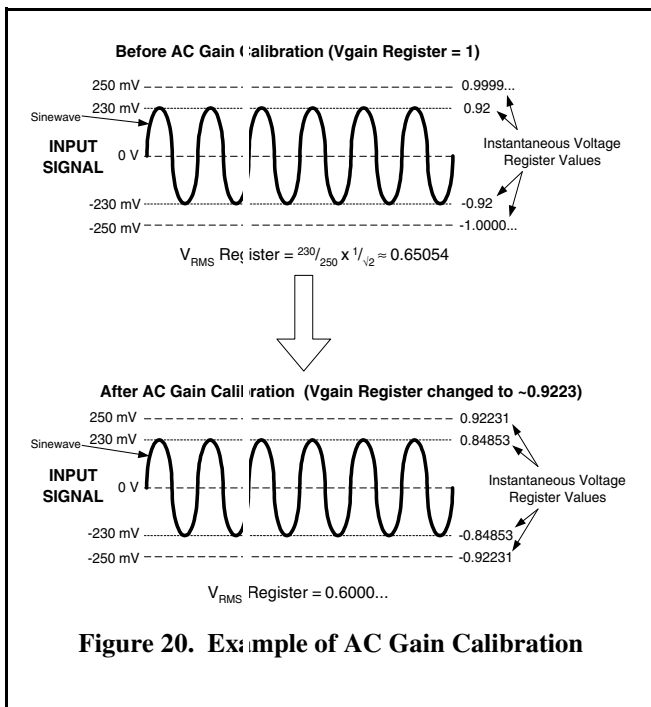
Figure 20. Example of AC Gain Calibration
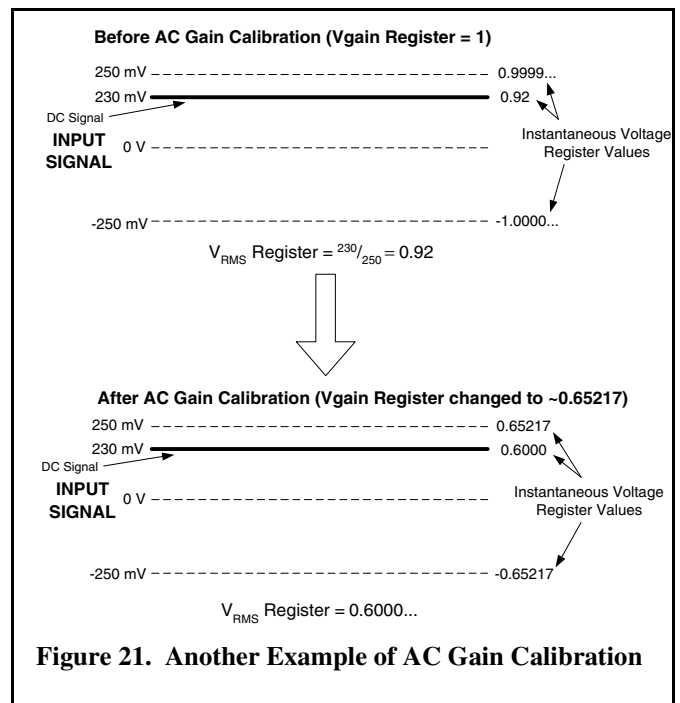
Figure 21. Another Example of AC Gain Calibration

Before DC Gain Calibration (Vgain Register = 1)

250 mV - 0.9999...
230 mV ━━━━━━━━━━━━━━━━━━━ 0.92
DC Signal
INPUT
SIGNAL   0 V -   Instantaneous Voltage
                                                                  Register Values

-250 mV -1.0000...

V_{RMS} Register = $^{230}/_{250}$ = 0.92

After DC Gain Calibration (Vgain Register changed to 1.0870)

230 mV ━━━━━━━━━━━━━━━━━━━ 0.9999...
DC Signal
INPUT
SIGNAL   0 V -   Instantaneous Voltage
                                                          Register Values

V_{RMS} Register = 0.9999...

Figure 22. Example of DC Gain Calibration
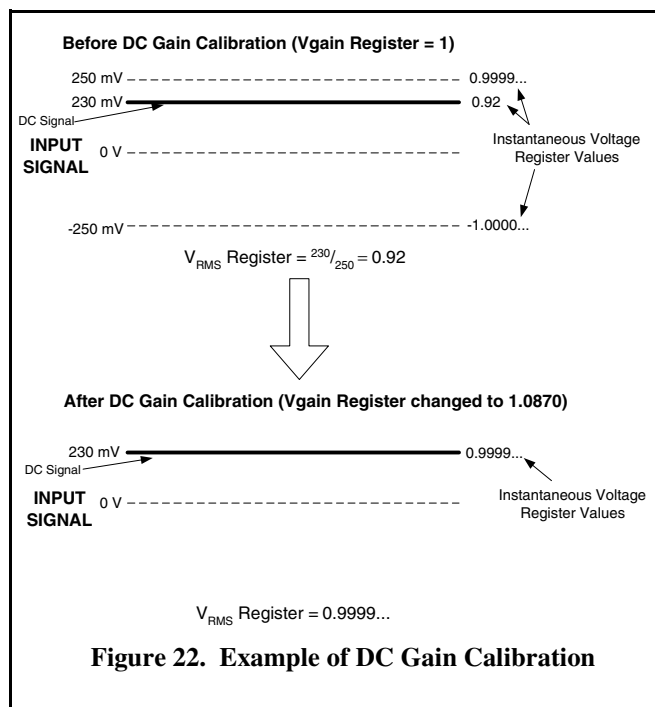
4.8.9 Is Calibration Required?

The CS5460A does not *have* to be calibrated. After the part is reset or powered on, the device is functional and can perform measurements without being calibrated. But the CS5460A's output is *always* affected by the values inside the various calibration registers. If no calibrations are executed by the user, then these registers will contain the default values (Gains = 1.0, DC Offsets = 0.0, AC Offsets = 0). Although the CS5460A can be used without performing an offset or gain calibration, the accuracy (with respect to a known voltage and current level) of the CS5460A will not be valid until after a gain/offset calibration is performed. Although the CS5460A will still exhibit the linearity + variation tolerances that are specified in Table 1, the reference voltage and current levels to which this linearity is referenced will be unknown for a given CS5460A sample. If no calibration is performed, these voltage/current reference levels exist based on the full-scale dc input voltage limits for each channel, which can be thought of as the voltages specified in the "Max Input" row of Table 1. But

these voltages will have a variation from part to part, as specified by the "Full-Scale Error" specs that are given for each channel, in the front of this data sheet (see Section 1). The previous statement also assumes that the offset on each channel is exactly zero, which would rarely (if ever) be true. A CS5460A must be calibrated to insure linearity + variation abilities of the devices can be referenced to known voltage/current levels, which then allows the CS5460A to obtain a corresponding accuracy + variation ability.

Also note that using gain calibration signal levels which cause the CS5460A to set the gain registers to a value that is less than unity will effectively decrease the guaranteed "±0.1% of reading" linearity + variation range (and therefore the accuracy range) of the respective channel. [Refer to Table 1.] This will occur whenever a DC gain calibration is performed using a DC signal that is less than the "Max Input" voltage levels specified for each channel in Table 1, or whenever an AC gain is performed using an AC signal whose RMS value is less then 60% of the "Max Input" voltage levels in Table 1. As an example, suppose the user runs the DC gain calibration sequence on the current channel, using a calibration signal level of 187.5 mV (DC). After this calibration is performed, the full-scale digital output code (0x7FFFFF in the Instantaneous Current Register) will be obtained whenever the input voltage across the IIN+ and IIN- pins is 187.5 mV (DC), which is 75% of the maximum available input voltage range [which is ±250 mV DC.] In this situation, the current channel input ranges for which ±0.1% accuracy + variation are guaranteed will be reduced to between 0.5mV (DC) and 187.5mV (DC), as opposed to what is specified in Table 1 [which would translate into a voltage range between 0.5mV (DC) and 250 mV (DC)].

Finally, remember that the ±0.1% (of reading) accuracy + variation guarantee is made with the assumption that the device has been calibrated with

MCLK = 4.096 MHz, K = 1, and N = 4000. If MCLK/K becomes too small, or if N is set too low (or a combination of both), then the CS5460A may not exhibit ±0.1% accuracy + variation.

4.8.10 Order of Calibration Sequences

Should offset calibrations be performed before gain calibrations? Or vice-versa? This section summarizes the recommended order of calibration.

1. If the user intends to include any DC content that may be present in the voltage/current and power/energy signals, then the DC offset calibration sequences should be run (for both channels) before any other calibration sequences. However if the user intends to remove the DC content present in either the voltage or current signals (by turning on the voltage channel HPF option and/or the current channel HPF option--in the Status Register) then the DC offset calibration for that channel does not need to be executed. Note that if *either* the voltage HPF or current HPF options are turned on, then any DC component that may be present in the power/energy signals will be removed from the CS5460A's power/energy results.

2. If the user intends to set the energy registration accuracy to within ±0.1% (with respect to reference calibration levels on the voltage/current inputs) then the user should next execute the gain calibrations for the voltage/current channels. The user can execute either the AC or DC gain calibration sequences.

3. Finally, the user should run the AC offset calibration sequences for the voltage and current channels. Simply ground the "+" and "-" inputs of both channels and execute the AC offset cal sequence.

4.8.11 Calibration Tips

To minimize digital noise, the user should wait for each calibration step to be completed before reading or writing to the serial port.

After a calibration is performed, the offset and gain register contents can be read and stored externally by the system microcontroller and recorded in memory. The same calibration words can be uploaded into the offset and gain registers of the converters when power is first applied to the system, or when the gain range on the current channel is changed.

4.9 Phase Compensation

Bits 23 to 17 of the Configuration Register are used to program the amount of phase delay that is added to the voltage channel signal path. This phase delay is applied to the voltage channel signal in order to compensate for phase delay that is may be introduced by the user-supplied voltage and current sensor circuitry, which is external to the CS5460A. Voltage and current transformers, as well as other sensor equipment applied to the front-end of the CS5460A inputs can often introduce a phase delay in the system, which distorts the phase relationship between the voltage and current signals that are to be measured. The user can set the phase compensation bits PC[6:0] in the Configuration Register to nullify this undesirable phase distortion between the two channels. The value in the 7-bit phase compensation word represents the delay that can be imposed on the voltage channel's analog input signal with respect to the current channel's analog input signal.

The CS5460A does not provide an automated phase calibration sequence. If the user is concerned about nullifying the phase shift between the voltage and current channels, the user must determine the optimal phase compensation setting experimentally. The default value of the phase compensation bits is 0000000. Note that this setting represents the closest time-delay (and therefore the smallest phase delay) between the voltage and current channel signal paths. That is, the phase delay inside the CS5460A is smallest with the 0000000 setting. But phase shifts introduced by the designer's external voltage/current sensor components may persuade the designer to intentionally impose a non-zero phase shift correction value in

the voltage channel. With the default setting, the phase delay on the voltage channel is 0.995 us (~0.0215 degrees assuming a 60 Hz power signal). Note that the 7-bit phase compensation word is a 2's complement binary number. With MCLK = 4.096 MHz and K=1, the range of the internal phase compensation ranges from -2.8 degrees to +2.8 degrees when the input voltage/current signals are at 60 Hz. In this condition, each step of the phase compensation register (value of one LSB) is ~0.04 degrees. The value in the 7-bit phase compensation word represents the delay on the voltage channel with respect to the current channel. For values of MCLK other than 4.096 MHz, these values for the span (-2.8 to +2.8 degrees) and for the step size (0.04 degrees) should be scaled by 4.096 MHz / (MCLK / K). For power line frequencies other than 60Hz (e.g., 50 Hz), the user can predict the values of the range and step size of the PC[6:0] bits by converting the above values to time-domain (seconds), and then computing the new range and step size (in degrees) with respect to the new line frequency.

To calibrate the phase delay, the user may try adjusting the phase compensation bits while the CS5460A is performing normal continuous conversions. Before doing so, the user should provide a purely resistive load (no inductance or capacitance) to the power line, such that nominal-level voltage and current signals from the power line are sensed into the voltage and current channels of the CS5460A. In this condition, any phase delay between the measured voltage and current signals is due only to phase delay introduced by the user's external voltage/current sensor circuitry. The objective is to adjust the phase compensation bits until the Energy Register value is maximized.

4.10 Time-Base Calibration Register

The Time-Base Calibration Register (notated as "TBC" in Figure 3) is used to compensate for slight errors in the XIN frequency. External oscillators and crystals have certain tolerances. If the user is concerned about improving the accuracy of the clock for energy measurements, the Time-Base Calibration Register can be manipulated to compensate for the frequency error. Note from Figure 3 that the TBC Register only affects the value in the Energy Register.

As an example, if the desired XIN frequency is 4.096 MHz, but during production-level testing, suppose that the average frequency of the crystal on a particular board is measured to actually be 4.091 MHz. The ratio of the desired frequency to the actual frequency is 4.096 MHz/4.091 MHz = ~1.00122219506. The TBC Register can be set to 1.0012223364 = 0x80280C(h), which is very close to the desired ratio.

4.11 Power Offset Register

Referring to Figure 3, note the "P_{off}" Register that appears just after the power computation. This register can be used to offset system power sources that may be resident in the system, but do not originate from the power line signal. These sources of extra energy in the system contribute undesirable and false offsets to the power/energy measurement results. For example, even after DC offset and AC offset calibrations have been run on each channel, when a voltage signal is applied to the voltage channel inputs and the current channel is grounded (i.e., there is zero input on the current channel), the current channel may still register a very small amount of RMS current. This non-zero RMS current value is caused by leakage of the voltage channel input signal into the current channel input signal path. The user can experimentally determine the amount of stray power that might be induced into the input pins, and then program the Power Offset Register to nullify the effects of this unwanted energy.

4.12 Input Protection - Current Limit

In Figures 6, 7, 8, and 9, note the series resistor R_{I+} which is connected to the IIN+ input pin. This resistor serves two purposes. First, this resistor functions in coordination with R_{I+} to form a first-order low-pass filter. The filter will a) remove any broadband noise that is far outside of the frequency range of interest, and also b) this filter serves as the *anti-aliasing filter*, which is necessary to prevent the A/D converter from receiving input signals whose frequency is higher than one-half of the sampling frequency (the Nyquist frequency). The second purpose of this resistor is to provide current-limit protection for the Iin+ input pin, in the event of a power surge or lightening surge. The role that R_{I+} contributes to input filtering will be discussed in the Section 4.13. But first the protection requirements for the Iin+/Iin- and Vin+/Vin-pins are discussed.

The voltage/current-channel inputs have surge-current limits of 100 mA. This applies to brief voltage/current spikes (<250 msec). The limit is 10 mA for DC input overload situations. To prevent permanent damage to the CS5460A, the designer must include whatever protection safeguards are necessary in their power meter design, to insure that these pin current limits are never exceeded, when CS5460A is operating in the intended power-line metering environment.

Focussing specifically on Figure 7, which shows how voltage/current transformers can be used as sensors, suppose for example that the requirements for a certain 120 VAC power system require that the power meter must be able to withstand up to a 8kV voltage spike on the power line during normal operating conditions. To provide a suitable sensor voltage input level to the voltage channel input pins of the CS5460A, the turns ratio of the voltage-sense transformer should be chosen such that the ratio is on the order of 1000:1. A voltage-sense transformer with a 1000:1 turns ratio will provide a 120 mV (rms) signal to the CS5460A's voltage

channel inputs, when the power line voltage is at the nominal level of 120 VAC. Therefore, a brief 8kV surge would be reduced to a 8V surge across R_1.

What happens when 8 volts is present across one of the analog input pins of the CS5460A? The Vin+/Vin- and Iin+/Iin- pins of the CS5460A are equipped with internal protection diodes. If a voltage is presented to any of these pins that is larger than approximately +/-7V (with respect to VA-pin) these protection diodes will turn on inside the CS5460A. But in order to prevent excessive current levels from flowing through the device, the value of R_1 must be large enough that when a 8V surge is present across the secondaries of the voltage-sense transformer, the brief surge current through R_{V+} should not be any greater than 100mA. Therefore, a minimum value for R_{V+} would be (8V - 7V) / 100mA = 10 Ohms. This value may be increased as needed, to easily obtain the desired cut-off frequency of the anti-aliasing filter on the voltage channel (described later), and also to provide some margin. But the designer should try to avoid using values for the protection resistors that are excessively high. A typical value for R_{V+} would be 470 Ohms.

The VIN- pin should also have a protection resistor (called R_{V-} in Figure 7). To maintain symmetry, the value of R_{V-} should be made equal to R_{V+}.

For the current channel inputs (Iin+ and Iin-), if we assume that the maximum current rating for this power line is 30A (RMS), then a suitable turns ratio for the current-sense transformer might be 200:1. Since the maximum load for a 120 VAC line rated at 30A would be 4 Ohms (for unity power factor) a 8kV surge across "L" and "N" could generate as much as 2000A (RMS) of current through the primaries of the current-sense transformer. This can in turn generate as much as 10V across the secondaries of the current-sense transformer. This voltage is high enough to turn on one or more of the internal protection diodes located off of the Iin+/Iin- pins.

Therefore, the value of the protection resistor that will limit the current flow to less than 100 mA would be (10V - 7V) / 100 mA = 30 Ohms. In order to provide some margin and to use the same resistor values that are used on the Vin+/Vin- pins, we could use 470 Ohms as a lower limit for the R_{I+} and R_{I-} resistors shown in Figure 7.

Referring to the circuit implementations shown in Figures 6, 8, and 9, note that when resistor-divider configurations are used to provide the voltage channel sense voltage, the VIN+ pin does not need an additional, separate, dedicated protection resistor. This is because the resistive voltage-divider already provides the series resistance that is needed for this protection resistance. (And note in Figure 8 that this is true for both the VIN+ pin and the VIN- pin.) In Figure 7, a voltage transformer is used as the voltage sensor. When any type of transformer is used as the sensor device for voltage (or current) channel, a dedicated protection resistor R_{V+} should be installed in series with the VIN+ pin, and similarly, a resistor (R_{V-}) should be installed in series to the VIN- input pin.

Additional considerations/techniques regarding the protection of the analog input pins against sudden high-frequency, high-level voltage/current surges are discussed in Section 4.14.

4.13 Input Filtering

Figure 6 shows how the analog inputs can be connected for a *single-ended* input configuration. Note here that the Vin- and Iin- input pins are held at a constant dc common-mode level, and the variation of the differential input signal occurs only on the Vin+ and Vin- pins. The common-mode level on the Vin-/Iin- pins is often set at (or very near) the CS5460A's common-mode ground reference potential. (The common-mode ground reference potential is defined by the voltage at the VA- pin.) But this is not required--the dc reference level of the Vin-/Iin- pins can be set to any potential between [VA-] and [(VA+) - 250mV]. In Figure 6,

observe the circuitry used in front of the current channel input pins as an example. The anti-aliasing filter can be constructed by calculating appropriate values for R_{I+} = R_{I-}, and C_{I+}. The sensor voltage that is created by the voltage drop across R_{SHUNT} is fed into the Iin+ pin, while the voltage at the Iin- pin is held constant.

Figure 7 shows a *differential bipolar* input configuration. Note in Figure 7 that the "+" and "-" input pins for the voltage/current channels are equally referenced above and below the CS5460A's ground reference voltage. Such a differential bipolar input configuration can be used because the CS5460A voltage/current channel inputs are able to accept input voltage levels as low as -250 mV (common-mode) below the VA- pin ground reference, which is defined by the voltage at the VA- pin. (In fact, if the designer desires it, the center-tapped reference of these differential input pairs could be connected to a DC voltage such as +2V, because +2V is within the available common-mode range of [VA-] and [VA+ - 250mV]. But this configuration would probably not be so practical in most situations.) In the differential bipolar input configuration, the voltage signals at the Vin- and Iin- pins will fluctuate in similar fashion to the Vin+/Iin+ pins, except the voltages at the "-" pins will be 180 degrees out of phase with respect to the voltage signals at the "+" pins. Therefore the signal paths to the "+" and "-" pins play an equal role in defining the differential voltage input signal. Because of this, the protection resistors placed on Vin-/Iin- pins will play an equally important role as the resistors on the Vin+/Iin+ pins, in defining the differential responses of the voltage/current channel input anti-aliasing filters. These resistors also serve as the current-limit protection resistors (mentioned earlier).

It should be noted that for the single-ended configurations for the voltage/current channels of Figure 6 and also for the voltage channel of Figure 9, the C_{V+} and C_{I+} capacitors could still be placed direct-

ly across the "+" and "-" pins of the voltage/current input channels, resulting in a differential type of configuration, even though the Vin- and Iin- lines are eventually connected to the ground reference of VA-. This would form a "hybrid" between a differential configuration and a single-ended configuration, because there will be some common-mode variation present on the input lines, but now the R_{V-} and R_{I-} resistors would play an equally important role (equal to R_{V+}/R_{I+} resistors) in determining the input filter characteristics. Such a configuration may actually be preferable to a true single-ended input configuration.

Before determining a typical set of values for R_{V+}, R_{V-}, C_{Vdiff}, R_{I+}, R_{I-}, and C_{Idiff} in Figure 7, several other factors should be considered:

1. Values for $R_{V+/I+}$, $R_{V-/I-}$, and $C_{Vdiff/Idiff}$ must be chosen with the desired lowpass cutoff frequencies in mind. In general, the cutoff frequencies should not be less than 10 times the cut-off frequencies of the internal voltage/current channel filters, which can be estimated by studying Figure 4 and Figure 5. From these figures, we see that the internal voltage channel cutoff frequency is at ~1400 Hz while the current channel cutoff frequency is at ~1600 Hz. If the cutoff frequency of the external anti-aliasing filter is much less than 10x these values (14000 Hz and 16000 Hz), then some of the harmonic content that may be present in the voltage/current signals will be attenuated by the voltage/current channel input anti-aliasing filters, because such 1st-order R-C filters will begin to roll off at a frequency of 1/10th of the filter's -3dB cutoff frequency. If the designer is not interested in metering energy that may be present in the higher harmonics (with respect to the fundamental power line frequency) then the cutoff frequencies on the voltage/current input networks can be reduced. However, relaxing the metering bandwidth is usually unacceptable, as most modern power meters are required to consider energy out to the 11th harmonic (at a minimum).

2. The first-order time-constants of the overall voltage and current channel sensor networks should be set such that they are equal (within reason), or at least close in magnitude. If the time-constants of the voltage/current sensor networks are not well-matched, then the phase relationship between the voltage-sense and current-sense signals will suffer an undesirable shift. In this situation, the real (true) power/energy measurements reported by the meter can contain significant error, because the power factor of the sensed voltage and current signals will be significantly different than the actual power factor on the power line. Note also that in addition to the time-constants of the input R-C filters, the phase-shifting properties of the voltage/current sensors may also contribute to the overall time-constants of the voltage/current input sensor networks. Therefore, this possible source of additional phase-shift caused by the sensor devices must also be considered as the designer selects the final R and C values for the voltage/current anti-aliasing filters. The designer should also note that as an alternative to, or in addition to the fine adjustment of the R and C values of the two anti-alias filters, the designer may also be able to adjust the CS5460A's phase compensation bits (see *Phase Compensation*) to more closely match the overall time-constants of the voltage/current input networks. But regardless of whether the phase compensation bits are or are not used to help more closely match the time-constants of the overall voltage/current input networks, this requirement of equal time-constants must ultimately be considered, when the designer selects the final R and C values that will be used to realize the voltage/current input anti-aliasing filters. (Of course, this factor may not turn out to be so important if the designer is confident that the mis-match between the two time-constants will not cause enough error to violate the given accuracy requirements for their particular power/energy metering application.)

3. Referring to the specs in *Section 1*, note that the differential input impedance across the current channel input pins is only 30 kOhm, which is significantly less than the impedance across the voltage channel input pins (which is 1 MOhm). While the impedance across the voltage channel is usually high enough to be ignored, the impedance across the current channel inputs may need to be taken into account by the designer when the desired cutoff frequencies of the filters (and the time-constants of the overall input networks) are calculated. Also, because of this rather low input impedance across the current channel inputs, the designer should note that the as the values for R_{I+} and/or R_{I-} are increased, the interaction of the current channel's input impedance can begin to cause a significant voltage drop situation within the current channel input network. If this is not taken into account, values may be chosen for $R_{I+} = R_{I-}$ that are large enough to cause the designer to believe that there is an unexplainable discrepancy between the expected (theoretical) sensor gain and the actual sensor gain of the current sensor network. Also, if this voltage drop effect is not considered, the designer may select values for R_{I+} and R_I that are slightly larger than they should be, in terms of maximizing the available dynamic range of the current channel input. And for the very same reason, the line-current-to-sensor-output-voltage reduction factor of the current sensor may not be optimized if this voltage division is not considered by the designer, for example when the value of the burden resistor is selected for a given current transformer. This should be considered, although the user should note that a slight voltage drop only causes a slight loss in available dynamic range, and the effects of this voltage drop on the current channel sensor gain can be removed during gain calibration of the current channel.

4. The filter capacitors C_{V+}, C_{V-}, C_{I+}, C_{I-}, C_{Vdiff}, and C_{Idiff} should also serve the purpose of attenuating very high-frequency RFI that can enter into the CS5460A's input pins. Therefore, during layout of the PCB, these capacitors should be placed in close proximity to their respective input pins.

We start with the current channel. [Note that for the purposes of this discussion, we assume that the phase-shifts caused by the voltage-sense transformer and current-sense transformer in Figure 7 are negligible or, at least equal, although such an assumption should definitely not be made in a real-life practical meter design situation.] Using commonly available values for our components, if we set $R_{I+} = R_{I-} = 470$ Ohms, then a value of $C_{Idiff} = 2.2$ uF will give us a -3dB cutoff frequency of 12626 Hz for the current channel. Then, for the voltage channel, if we also set $R_{V+} = R_{V-} = 470$ Ohms and $C_{Idiff} = 2.2$ uF, the -3dB cutoff frequency of the voltage channel's input filter will be 12250 Hz. If we were concerned about the effect that the difference in these two cutoff frequencies (and therefore the mis-match between the time-constants of the overall voltage/current input networks) would have on the accuracy of our power/energy results, we might take the trouble to use a non-standard resistor value for $R_{I+} = R_{I-}$ of (for example) 455 Ohms. This would shift the voltage channel's -3dB cutoff frequency of the filter on the voltage channel inputs to 12651 Hz, which would cause the first-order time-constant values of the voltage/current channel input filters to be more equal.

As was mentioned earlier, in addition to or as an alternative to slightly modifying the value of $R_{I+} = R_{I-}$ or $R_{V+} = R_{V-}$, we may be able to more closely match the voltage/current channel time-constants by adjusting the phase compensation bits, which might then allow the designer to avoid having to use less commonly-available resistor/capacitor values (such as $R_{I+} = R_{I-} = 455$ Ohms). Suppose that we do not slightly alter the values of $R_{I+} = R_{I-}$, so that the values of the R's and C's of both channels is again the same. In this case, we can estimate the first-order time-constants of the two R-C filters by

taking the reciprocal of the -3dB cutoff frequencies. If we subtract these two time-constants, we can conclude that after the voltage/current signals pass through their respective anti-aliasing filters, the sensed voltage signal will be delayed ~2.431 usec more than the current signal. If we assume that we are metering a 60 Hz power system, this implies that the sensed voltage signal will be delayed ~0.0525 degrees more than the current signal. Also, we note that when the PC[6:0] bits are set to their default setting of 0000000, the internal filtering stages of the CS5460A will impose an additional delay on the voltage signal of 0.0215 degrees, with respect to the current. (Again, we are assuming a 60 Hz power system). The total difference between the delay on the voltage fundamental and the current fundamental will therefore be ~0.074 degrees. But if we were to set the phase compensation bits to 1111110, the voltage will be delayed -0.08 degrees, which is the same as shifting the voltage forward by 0.08 degrees, which would bring the delays of the voltage-sense and current-sense signals much closer to each other. The phase compensation bits would then be an effective way to allow the designer to use the same R and C component values in both of these R-C filters.

As a final note, the reader should realize that the above situation is rather hypothetical. For example, if we assume that the tolerances of the R and C components that are used to build the two R-C filters is 0.1%, then either time-constant could vary by as much as much as ~±2.07 usec, which means that the delay between the voltage-sense and current-sense signals that is caused by these filters could vary by as much as ~±4.1 us, which is equivalent to a phase shift of ~±0.089 degrees (at 60Hz). This in turn implies that our conclusion to adjust the phase compensation bits, to shift the voltage signal forward by 0.08 degrees, could actually cause the voltage signal to be shifted as much as ~0.065 degrees ahead of the current signal. Thus, the use of the phase compensation bits to more

closely match the two time-constants may only be useful if a rather precise calibration operation is performed on each individual power meter, during product test.

4.14 Protection Against High-Voltage and/or High-Current Surges

In many power distribution systems, it is very likely that the power lines will occasionally carry brief but large transient spikes of voltage or current. Two common sources of such high-energy disturbances would be a surge in the line during a lightning storm, or a surge that is caused when a very inductive or capacitive load on the power line is suddenly turned on. In these situations, the input protection resistors and corresponding input filter capacitors (discussed in the previous sections) may not be sufficient to protect the CS5460A from such high-frequency voltage/current surges. The surges may still be strong enough to cause permanent damage to the CS5460A. Because of this, the designer should consider adding certain additional components within the voltage/current channel input circuitry which can help to protect the device from being permanently damaged by the surges. Referring to Figure 23, the addition of capacitors C1 and C2 can help to further attenuate these high-frequency power surges, which can greatly decrease the chances that the CS5460A will be damaged. Typical values for C1 and C2 may be on the order of 10pF, although the exact value is related to the reactive and resistive properties of the user's voltage and current sensor devices. In addition, diodes D1 - D4 can help to quickly clamp a high voltage surge voltage presented across the voltage/current inputs. An example of a suitable diode part number for this application is BAV199, which has the ability to turn on very quickly (very small turn-on time). A fuse could potentially serve this purpose as well (not shown). R3 and R4 can provide protection on the "-" sides of the two input pairs. Set R3 = R1 and R4 = R5. Finally, placing 50-Ohm resistors in series with the VA+ and VD+

pins is another technique that has sometimes proven to be effective in protecting the CS5460A from such high-level, high-frequency voltage/current surges. However, these 50-Ohm resistors may not be necessary if the protection on the analog input channels is sufficient, and this is not the most attractive solution, because these resistors will dissipate what can be a significant amount of power, and they will cause an undesirable voltage drop which decreases the voltage level of the VA+ and VD+ supply pins.

4.15 Improving RFI Immunity

During EMC acceptance testing of the user's power metering assembly, the performance of the CS5460A's A/D converters can be adversely affected by external radio frequency interference (RFI). Such external RFI can be coupled into the copper traces and/or wires on the designer's PCB. If RFI is coupled into any of the traces that tie into the CS5460A's Vin+/Vin- or Iin+/Iin- input pins, then errors may be present in the CS5460A output.

When such degradation in performance is detected, the user may improve the CS5460A's immunity to RF disturbance by configuring the "+" and "-" inputs of the voltage/current channel inputs such that they are more symmetrical. This is illustrated in Figure 23 with the addition of resistors R3 and R4, as well as capacitors C5 and C6. Note that the input circuitry that is placed in front of the voltage/current channel inputs in Figure 23 defines *single-ended* input configurations (for both channels). Therefore, these extra resistors and components are not needed to achieve the simple basic anti-aliasing filtering on the inputs. But the addition of these extra components can create more symmetry across the '+' and '-' inputs of the voltage/current input channels, and this can often help to reduce the CS5460A's susceptibility to RFI. The value of C5 should be the same as C3, (and so the designer may have to re-calculate the value of C3, since the addition of C5 will change the overall differential-/common-mode frequency responses of the input filter.) A similar point can be made for the
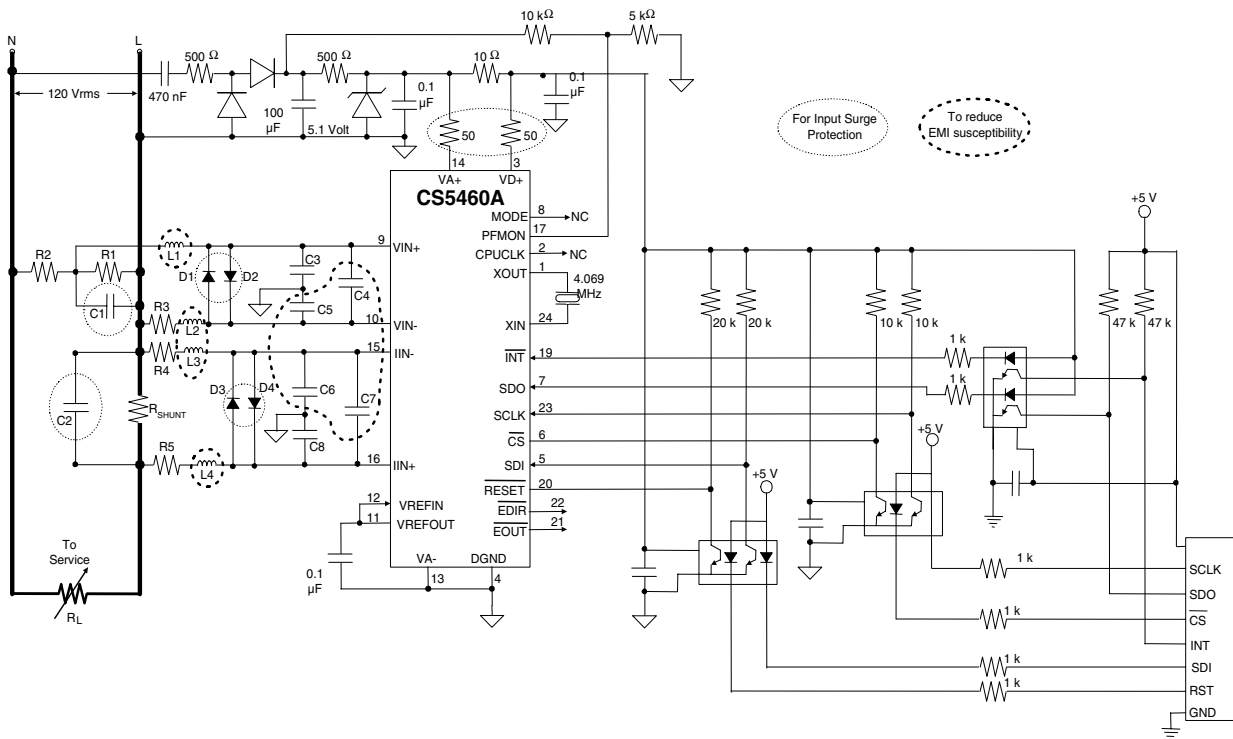
Figure 23. Input Protection for Single-Ended Input Configurations, using resistive divider and current shunt resistor. Note that the digital interface is isolated using opto-isolators.

addition of C6 (to match C8) on the current channel's input filter. Finally, C4 and C7 can also sometimes help to improve CS5460A's performance in the presence of RFI. All of these input capacitors (C3 - C8) should be placed in very close proximity to the '+' and '-' pins of the voltage/current input pairs in order to maximize their ability to protect the input pins from high-frequency RFI. In addition to or as an alternative to these capacitors, L1 - L4 can sometimes help to suppress the incoming RFI. Note that the additional components just discussed can sometimes actually *degrade* the CS5460A's immunity to RFI. The exact configuration that works best for the designer can vary significantly, according to the user's exact PCB layout/orientation. Finally, note that inside the CS5460A, the Vin+, Vin-, Iin+, and Iin- pins have all been buffered with ~10pF of internal capacitance (to VA-) in attempt to improve the device's immunity to external RFI.

4.16 PCB Layout

For optimal performance, the CS5460A should be placed entirely over an analog ground plane with both the VA- and DGND pins of the device connected to the analog plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip.

Note: Refer to the CDB5460A Evaluation Board for suggested layout details and Applications Note 18 for more detailed layout guidelines. Before layout, please call for our Free Schematic Review Service.

Schematic & Layout Review Service

Confirm Optimum
Schematic & Layout
Before Building Your Board.

For Our Free Review Service
Call Applications Engineering.

C a l l : (5 1 2) 4 4 5 - 7 2 2 2

5. REGISTER DESCRIPTION
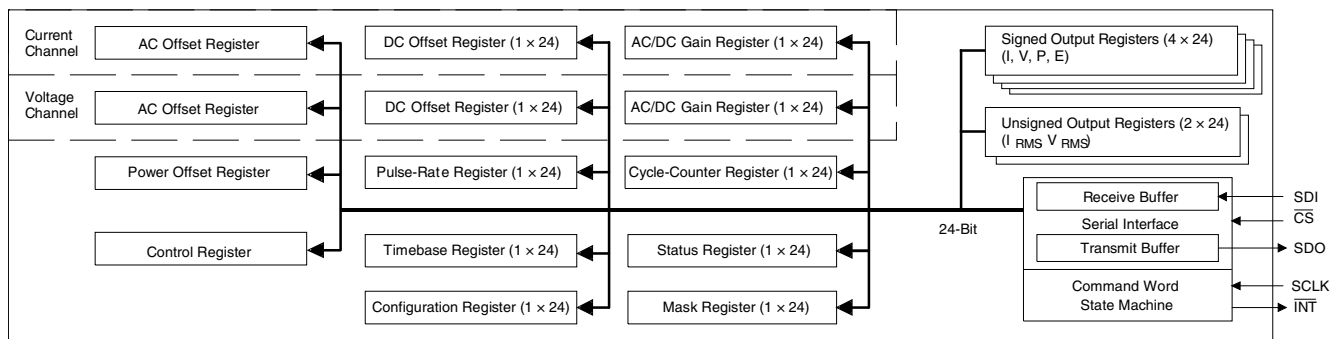
Figure 24. CS5460A Register Diagram

Note: 1. ** "default" => bit status after software or hardware reset

2. Note that all registers can be read from, and written to.

5.1 Configuration Register
Address: 0

23	22	21	20	19	18	17	16
PC6	PC5	PC4	PC3	PC2	PC1	PC0	Gi

15	14	13	12	11	10	9	8
EWA	Res	Res	SI1	SI0	EOD	DL1	DL0

7	6	5	4	3	2	1	0
RS	VHPF	IHPF	iCPU	K3	K2	K1	K0

Default** = 0x000001

K[3:0]   Clock divider. A 4 bit binary number used to divide the value of MCLK to generate the internal clock DCLK. The internal clock frequency is DCLK = MCLK/K.   The value of K can range between 1 and 16. Note that a value of "0000" will set K to 16 (not zero).

iCPU   Inverts the CPUCLK clock. In order to reduce the level of noise present when analog signals are sampled, the logic driven by CPUCLK should not be active during the sample edge.
0 = normal operation (default)
1 = minimize noise when CPUCLK is driving rising edge logic

IHPF   Control the use of the High Pass Filter on the Current Channel.
0 = High-pass filter is disabled. If VHPF is set, use all-pass filter. Otherwise, no filter is used. (default)
1 = High-pass filter is enabled.

VHPF   Control the use of the High Pass Filter on the voltage Channel.
0 = High-pass filter is disabled. If IHPF is set, use all-pass filter. Otherwise, no filter is used. (default)
1 = High-pass filter enabled

RS   Start a chip reset cycle when set 1. The reset cycle lasts for less than 10 XIN cycles. The bit is automatically returned to 0 by the reset cycle.

DL0   When EOD = 1, $\overline{\text{EDIR}}$ becomes a user defined pin. DL0 sets the value of the $\overline{\text{EDIR}}$ pin.
            Default = '0'

DL1   When EOD = 1, $\overline{\text{EOUT}}$ becomes a user defined pin. DL1 sets the value of the $\overline{\text{EOUT}}$ pin.
            Default = '0'

EOD   Allows the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins to be controlled by the DL0 and DL1 bits. $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ can also be accessed using the Status Register.
            0 = Normal operation of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins. (default)
            1 = DL0 and DL1 bits control the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins.

SI[1:0]   Soft interrupt configuration. Select the desired pin behavior for indication of an interrupt.
            00 = active low level (default)
            01 = active high level
            10 = falling edge (INT is normally high)
            11 = rising edge (INT is normally low)

Res   Reserved. These bits must be set to zero.

EWA   Allows the output pins of $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ of multiple chips to be connected in a wire-AND, using an external pull-up device.
            0 = normal outputs (default)
            1 = only the pull-down device of the $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pins are active

Gi   Sets the gain of the current PGA
            0 = gain is 10 (default)
            1 = gain is 50

PC[6:0]   Phase compensation. A 2's complement number used to set the delay in the voltage channel. When MCLK=4.096 MHz and K=1, the phase adjustment range is about -2.8 to +2.8 degrees and each step is about 0.04 degrees (this assumes that the power line frequency is 60 Hz). If (MCLK / K) is not 4.096 MHz, the values for the range and step size should be scaled by the factor 4.096MHz / (MCLK / K).
            Default setting is 0000000 = 0.0215 degrees phase delay (when MCLK = 4.096 MHz).

5.2 DC Current Offset Register and DC Voltage Offset Register

Address: 1 (DC Current Offset Register)
           3 (DC Voltage Offset Register)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

The DC Offset Registers are initialized to zero on reset, allowing the device to function and perform measurements. The register is loaded after one computation cycle with the current or voltage offset when the proper input is applied and the DC Calibration Command is received. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range ± full scale. The numeric format of this register is two's complement notation.

5.3 AC/DC Current Gain Register and AC/DC Voltage Gain Register

Address: 2 (Current Gain Register)
           4 (Voltage Gain Register)

MSB															LSB
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default** = 1.000

The Gain registers are initialized to 1.0 on reset, allowing the device to function and perform measurements. The Gain registers hold the result of either the AC or DC gain calibrations, whichever was most recently performed. If DC calibration is performed, the register is loaded after one computation cycle with the system gain when the proper DC input is applied and the Calibration Command is received. If AC calibration is performed, then after ~(6N + 30) A/D conversion cycles (where N is the value of the Cycle-Count Register) the register(s) is loaded with the system gain when the proper AC input is applied and the Calibration Command is received. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range $0.0 \leq$ Gain < 4.0.

5.4 Cycle Count Register

Address: 5

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default** = 4000

The Cycle Count Register determines the length of an energy and RMS conversion. A conversion cycle is derived from (MCLK/K)/(1024∗N) where MCLK is master clock, K is clock divider, and N is cycle count. N must be greater than 10 for I_{RMS}, V_{RMS} and energy calculations to be performed.

5.5 Pulse-Rate Register

Address: 6

MSB															LSB
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	.....	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

Default** = 32000.00Hz

The Pulse-Rate Register determines the frequency of the train of pulses output on the $\overline{EOUT}$ pin. Each $\overline{EOUT}$ pulse represents a predetermined magnitude of energy. The register's smallest valid value is 2^{-4} but can be in 2^{-5} increments.

5.6 I,V,P,E Signed Output Register Results

Address: 7 - 10

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

These signed registers contain the last value of the measured results of I, V, P, and E. The results are in the range of $-1.0 \le$ I, V, P, E < 1.0. The value is represented in two's complement notation, with the binary point place to the right of the MSB (which is the sign bit). I, V, P, and E are output results registers which contain signed values. Note that the I, V, and P Registers are updated every conversion cycle, while the E Register is only updated after each computation cycle. The numeric format of this register is two's complement notation.

5.7 I_{RMS}, V_{RMS} Unsigned Output Register Results

Address: 11,12

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

These unsigned registers contain the last value of the calculated results of I_{RMS} and V_{RMS}. The results are in the range of $0.0 \le I_{RMS}, V_{RMS} < 1.0$. The value is represented in binary notation, with the binary point place to the left of the MSB. I_{RMS} and V_{RMS} are output result registers which contain unsigned values.

5.8 Timebase Calibration Register

Address: 13

MSB															LSB
2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 1.000

The Timebase Calibration Register is initialized to 1.0 on reset, allowing the device to function and perform computations. The register is user loaded with the clock frequency error to compensate for a gain error caused by the crystal/oscillator tolerance. The value is in the range $0.0 \le$ TBC < 2.0.

5.9 Power Offset Register
Address: 14

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

This offset value is added to each power value that is computed for each voltage/current sample pair before being accumulated in the Energy Register. The numeric format of this register is two's complement notation. This register can be used to offset contributions to the energy result that are caused by undesirable sources of energy that are inherent in the system.

5.10 AC Current Offset Register and AC Voltage Offset Register
Address: 16 (AC Current Offset Register)
17 (AC Voltage Offset Register)

MSB															LSB
2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	.....	2^{-30}	2^{-31}	2^{-32}	2^{-33}	2^{-34}	2^{-35}	2^{-36}

Default** = 0.000

The AC offset registers are initialized to zero on reset, allowing the device to function and perform measurements. First, the ground-level input should be applied to the inputs. Then the AC Offset Calibration Command is should be sent to the CS5460A. After ~(6N + 30) A/D conversion cycles (where N is the value of the Cycle-Count Register), the gain register(s) is loaded with the square of the system AC offset value. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. Note that this register value represents the square of the AC current/voltage offset.

5.11 Status Register and Mask Register
Address: 15 (Status Register)
26 (Mask Register)

23	22	21	20	19	18	17	16
DRDY	EOUT	EDIR	CRDY	MATH	Res	IOR	VOR

15	14	13	12	11	10	9	8
PWOR	IROR	VROR	EOR	EOOR	Res	ID3	ID2

7	6	5	4	3	2	1	0
ID1	ID0	WDT	VOD	IOD	LSD	0	$\overline{IC}$

Default** = 0x000000 (Status Register)

0x000000 (Mask Register)

The Status Register indicates the condition of the chip. In normal operation writing a '1' to a bit will cause the bit to go to the '0' state. Writing a '0' to a bit will maintain the status bit in its current state. With this feature the user can simply write back to the Status Register to clear the bits that have been seen, without concern of clearing any newly set bits. Even if a status bit is masked to prevent the interrupt, the status bit will still be set in the Status Register so the user can poll the status.

The Mask Register is used to control the activation of the $\overline{INT}$ pin. Placing a logic '1' in the Mask Register will

allow the corresponding bit in the Status Register to activate the $\overline{\text{INT}}$ pin when the status bit becomes active.

$\overline{\text{IC}}$ Invalid Command. Normally logic 1. Set to logic 0 when the part is given an invalid command. Can be deactivated only by sending a port initialization sequence to the serial port (or by executing a software/hardware reset). When writing to the Status Register, this bit is ignored.

LSD   Low Supply Detect. Set when the voltage at the PFMON pin falls below the low-voltage threshold (PMLO), with respect to VA- pin. For a given part, PMLO can be as low as 2.3 V. LSD bit cannot be permanently reset until the voltage at PFMON pin rises back above the high-voltage threshold (PMHI), which is typically 100mV above the device's low-voltage threshold. PMHI will never be greater than 2.7 V.

IOD   Modulator oscillation detect on the current channel. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the current channel's Differential Input Voltage Range.

VOD   Modulator oscillation detect on the voltage channel. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the current channel's Differential Input Voltage Range.

         Note: This IOD and VOD bits may be 'falsely' triggered by very brief voltage spikes from the power line. This event should not be confused with a DC overload situation at the inputs, when the IOD and VOD bits will re-assert themselves even after being cleared, multiple times.

WDT   Watch-Dog Timer. Set when there has been no reading of the Energy Register for more than 5 seconds. (MCLK = 4.096 MHz, K = 1) To clear this bit, first read the Energy Register, then write to the Status Register with this bit set to logic '1'. When MCLK / K is not 4.096 MHz, the time duration is 5 * [4.096 MHz / (MCLK / K)] seconds.

ID3:0   Revision/Version Identification.

EOOR   The internal $\overline{\text{EOUT}}$ Energy Accumulation Register went out of range. Note that the $\overline{\text{EOUT}}$ Energy Accumulation Register is different than the Energy Register available through the serial port. This register cannot be read by the user. Assertion of the this bit can be caused by having an output rate that is too small for the power being measured. The problem can be corrected by specifying a higher frequency in the Pulse-Rate Register.

EOR   Energy Out of Range. Set when the calibrated energy value is too large or too small to fit in the Energy Register, which can be read via the serial port.

VROR   RMS Voltage Out of Range. Set when the calibrated RMS voltage value is too large to fit in the RMS Voltage Register.

IROR   RMS Current Out of Range. Set when the calibrated RMS current value is too large to fit in the RMS Current Register.

PWOR   Power Calculation Out of Range. Set when the *magnitude* of the calculated power is too large to fit in the Instantaneous Power Register.

VOR   Voltage Out of Range.

IOR   Current Out of Range. Set when the *magnitude* of the calibrated current value is too large or too small to fit in the Instantaneous Current Register.

MATH   General computation Indicates that a divide operation overflowed. This can happen normally in the course of computation. If this bit is asserted but no other bits are asserted, then there is no error, and this bit should be ignored.

CRDY   Conversion Ready. Indicates a new conversion is ready. This will occur at the output word rate, which is usually 4 kHz.

EDIR   Set whenever the EOUT bit asserted (see below) as long as the energy result is negative.

EOUT   Indicates that the energy limit has been reached for the $\overline{\text{EOUT}}$ Energy Accumulation Register, and so this register will be cleared, and one pulse will be generated on the $\overline{\text{EOUT}}$ pin (if enabled). The energy flow may indicate negative energy or positive energy. This must be determined by looking at the EDIR bit (above). This EOUT bit is cleared automatically when the energy rate drops below the level that produces a 4 KHz EOUT pin rate. The bit can also be cleared by writing to the Status Register. This status bit is set with a maximum frequency of 4 KHz (when MCLK/K is 4.096 MHz). When MCLK/K is not equal to 4.096 MHz, the user should scale the pulse-rate that one would expect to get with MCLK/K = 4.096 MHz by a factor of 4.096 MHz / (MCLK/K) to get the actual pulse-rate.

DRDY   Data Ready. When running in single or continuous conversion acquisition mode, this bit will indicate the end of computation cycles. When running calibrations, this bit indicates that the calibration sequence has completed, and the results have been stored in the offset or gain registers.

5.12 Control Register
Address: 28

23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res

15	14	13	12	11	10	9	8
Res	Res	Res	Res	Res	Res	Res	STOP

7	6	5	4	3	2	1	0
Res	MECH	Res	INTL	SYNC	NOCPU	NOOSC	STEP

Default** = 0x000000

STOP   1 = used to terminate the new EEBOOT sequence.

Res   Reserved. These bits must be set to zero.

MECH   1 = widens $\overline{\text{EOUT}}$ and $\overline{\text{EDIR}}$ pulses for mechanical counters.

INTL   1 = converts the $\overline{\text{INT}}$ output to open drain configuration.

SYNC   1 = forces internal A/D converter clock to synchronize to the initiation of a conversion command.

NOCPU   1 = converts the CPUCLK output to a one-bit output port.   Reduces power consumption.

NOOSC   1 = saves power by disabling the crystal oscillator for external drive.

STEP   1 = enables stepper-motor signals on the $\overline{\text{EOUT}}/\overline{\text{EDIR}}$ pins.

6. PIN DESCRIPTION

Crystal Out	**XOUT**	1 •	24	**XIN**	Crystal In
CPU Clock Output	**CPUCLK**	2	23	**SDI**	Serial Data Input
Positive Digital Supply	**VD+**	3	22	$\overline{\text{EDIR}}$	Energy Direction Indicator
Digital Ground	**DGND**	4	21	**EOUT**	Energy Output
Serial Clock Input	**SCLK**	5	20	$\overline{\text{INT}}$	Interrupt
Serial Data Output	**SDO**	6	19	$\overline{\text{RESET}}$	Reset
Chip Select	$\overline{\text{CS}}$	7	18	**NC**	No Connect
Mode Select	**MODE**	8	17	**PFMON**	Power Fail Monitor
Differential Voltage Input	**VIN+**	9	16	**IIN+**	Differential Current Input
Differential Voltage Input	**VIN-**	10	15	**IIN-**	Differential Current Input
Voltage Reference Output	**VREFOUT**	11	14	**VA+**	Positive Analog Supply
Voltage Reference Input	**VREFIN**	12	13	**VA-**	Analog Ground

Clock Generator

|		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - A gate inside the chip is connected to these pins and can be used with a crystal to provide the system clock for the device. Alternatively, an external (CMOS compatible clock) can be supplied into XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.

Control Pins and Serial Data I/O

Serial Clock Input	5	**SCLK -** A clock signal on this pin determines the input and output rate of the data for the SDI and SDO pins respectively. This input is a Schmitt trigger to allow for slow rise time signals. The SCLK pin will recognize clocks only when $\overline{\text{CS}}$ is low.
Serial Data Output	6	**SDO -** SDO is the output pin of the serial data port. Its output will be in a high impedance state when $\overline{\text{CS}}$ is high.
Chip Select	7	$\overline{\text{CS}}$ **-** When low, the port will recognize SCLK. An active high on this pin forces the SDO pin to a high impedance state. $\overline{\text{CS}}$ should be changed when SCLK is low.
Mode Select	8	**MODE** - When at logic high, the CS5460A can perform the auto-boot sequence with the aid of an external serial EEPROM to receive commands and settings. When at logic low, the CS5460A assumes normal "host mode" operation. This pin is pulled down to logic low if left unconnected, by an internal pull-down resistor to DGND.
Interrupt	20	$\overline{\text{INT}}$ **-** When $\overline{\text{INT}}$ goes low it signals that an enabled event has occurred. $\overline{\text{INT}}$ is cleared (logic 1) by writing the appropriate command to the CS5460A.
Energy Output	21	**EOUT -** The energy output pin output a fixed-width pulse rate output with a rate (programmable) proportional to energy.
Energy Direction Indicator	22	$\overline{\text{EDIR}}$ - The energy direction indicator indicates if the measured energy is negative.
Serial Data Input	23	**SDI -** the input pin of the serial data port. Data will be input at a rate determined by SCLK.

Measurement and Reference Input

Differential Voltage Inputs	9,10	**VIN+, VIN- -** Differential analog input pins for voltage channel.

Voltage Reference Output	11	**VREFOUT -** The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 2.5 V and is reference to the VA- pin on the converter.
Voltage Reference Input	12	**VREFIN -** The voltage input to this pin establishes the voltage reference for the on-chip modulator.
Differential Current Inputs	15,16	**IIN+, IIN- -** Differential analog input pins for current channel.

Power Supply Connections

Positive Digital Supply	3	**VD+ -** The positive digital supply is nominally +5 V ±10% relative to DGND.
Digital Ground	4	**DGND -** The common-mode potential of digital ground must be equal to or above the common-mode potential of VA-.
Negative Analog Supply	13	**VA- -** The negative analog supply pin must be at the lowest potential.
Positive Analog Supply	14	**VA+ -** The positive analog supply is nominally +5 V ±10% relative to VA-.
Power Fail Monitor	17	**PFMON -** The power fail Monitor pin monitors the analog supply. Typical threshold level (PMLO) is 2.45 V with respect to the VA- pin. If PFMON voltage threshold is tripped, the LSD (low-supply detect) bit is set in the Status Register. Once the LSD bit has been set, it will not be able to be reset until the PFMON voltage increases ~100 mV (typical) above the PMLO voltage. Therefore, there is hysteresis in the PFMON function.
RESET	19	**Reset -** When reset is taken low, all internal registers are set to their default states.

Other

No Connection	18	**NC -** No connection. Pin should be left floating.

7. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING
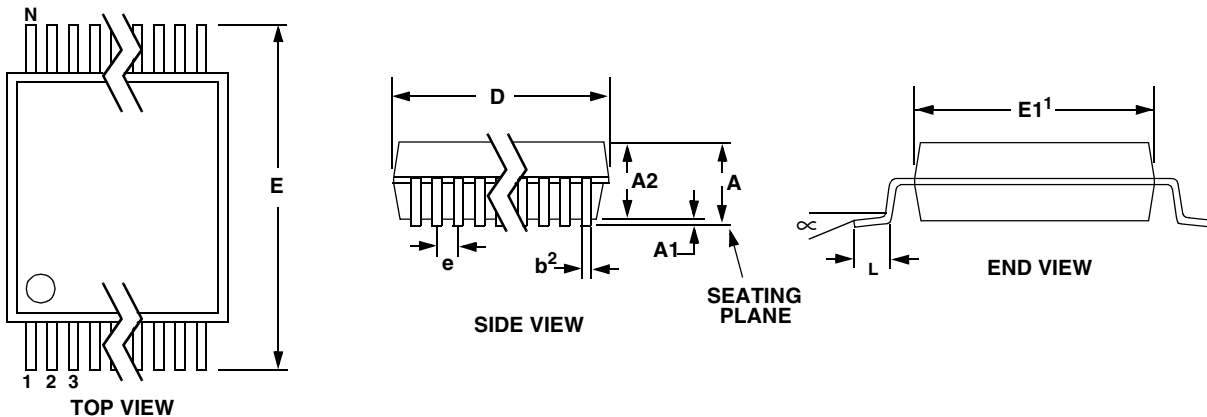
	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
$\propto$	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

CRYSTAL

• Notes •

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