SONY

CXB1549Q

Laser Diode Driver

Description

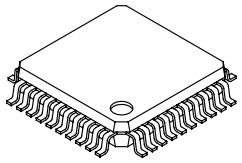
The CXB1549Q is a high-speed monolithic Laser Diode Driver/Current Switch with ECL/PECL input level. Open collector outputs are provided at the output pins (Q, QBX) and have the capacity of driving modulation current of 50mAp-p at a max. data rate of 1.25Gbps (Min.). Along with the modulation current generator there is the laser diode bias generator which has capacity of sourcing up to 60mA (Bias). The laser diode current can be controlled by either a voltage or current into the bias adjust pin (BiasAdj) and the bias set pin (SBias), depending on how these pins are configured. Control of the diode bias current is achieved through the APC (Automatic Power Control) circuitry. In order to avoid having a large current go through the laser diode, this IC also provides an Activity detector and Power on Reset functions for Laser Safety. The Activity detector circuit detects data edge transitions and if no data transition occur after a certain time period, then both the modulation and bias current are shutdown.

The Power on Reset circuit holds the modulation and bias current off for a set period of time while the system power is applied. Additionally, this IC has an internal Duty Cycle correction circuit that can control the falling edge of the input pulse up to a maximum of 0.2ns (Min.).

Features

- Maximum data rate (NRZ): 1.25Gbps
- Power on Reset function
- Alarm and Shutdown function
- Signal Duty cycle correction
- Automatic Power Control (APC) for bias current
- Activity detector function for laser safety
- Power indicate function
- Differential PECL inputs or AC coupled inputs

40 pin QFP (Plastic)



Application

- Gbit-ethernet: 1.25Gb/s
- SONET/SDH: 622Mb/s
- Fibre channel: 532Mb/s, 1.062Gb/s

Absolute Maximum Ratings

• Supply voltage	$V_{CC} - V_{EE}$	–0.3 to +6.0	V
• Input voltage	V_{IN}	V_{EE} to Vcc	V
• Differential input voltage	$\lvert V_D - V_{DB} \rvert$	0 to 2.5	V
• Bias output current		0 to 80	mA
• Modulation output current		0 to 70	mA
• SBias input/output current		0 to 5	mA
• Input bias control current	Iset (Ibiasadj)	0 to 5	mA
• Input bias control voltage	Vset (Vbiasadj)	0 to 3	V
• Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

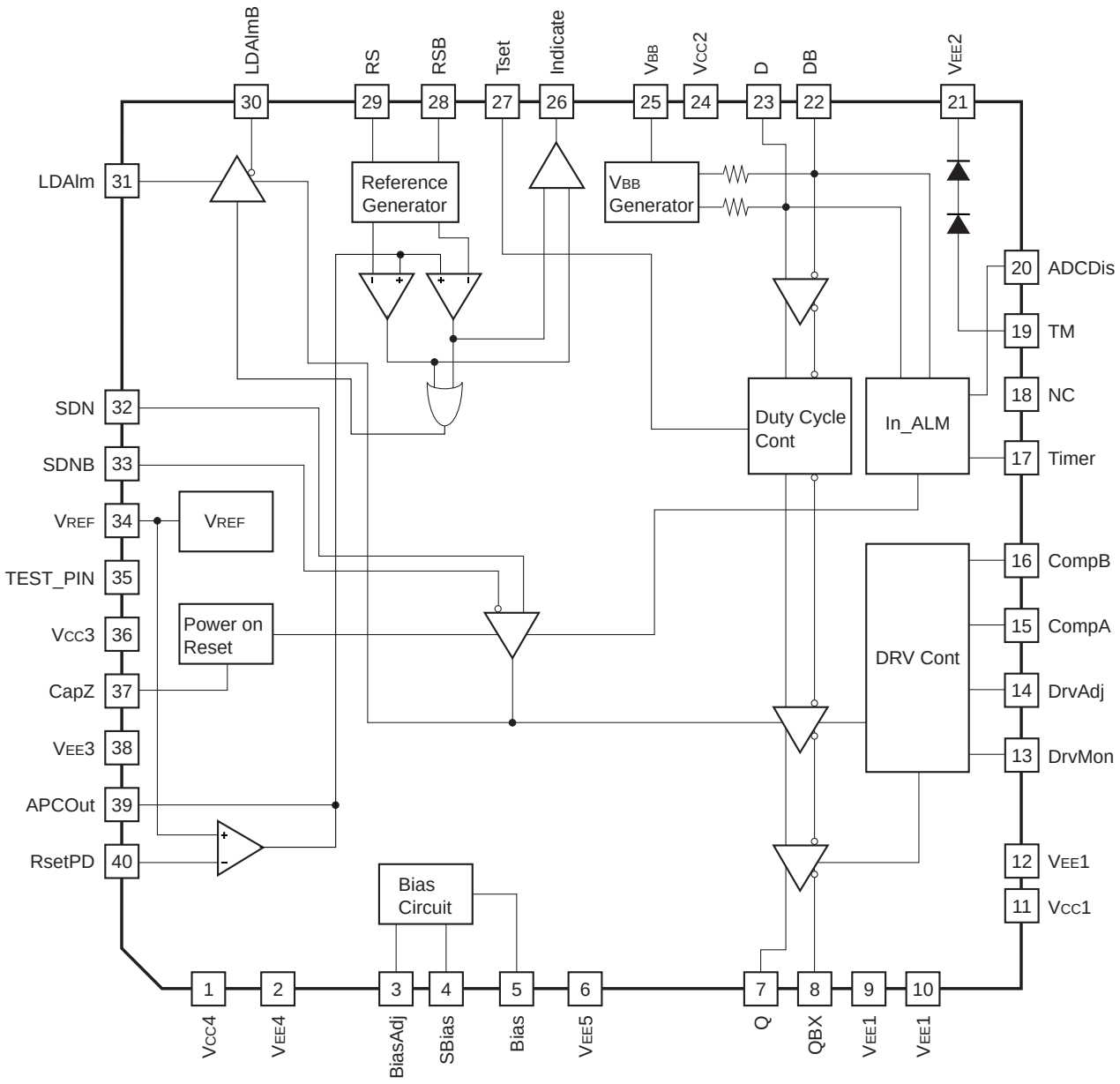
• DC power supply voltage	$V_{CC} - V_{EE}$	3.14 to 3.46	V
• Operating ambient temperature	Ta	–40 to +85	°C

Structure

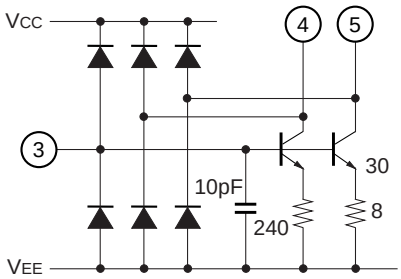
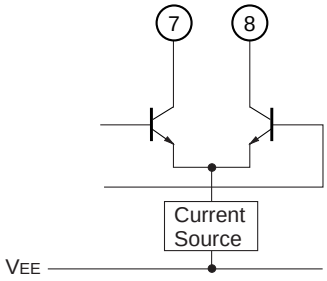
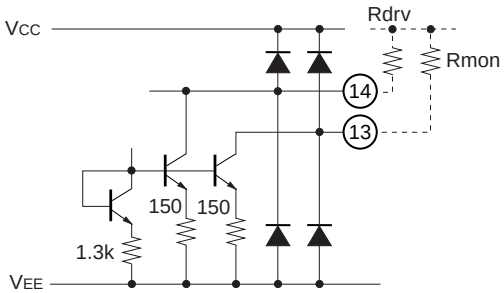
Bipolar silicon monolithic IC

E98313B92-PS

Block Diagram and Pin Assignment

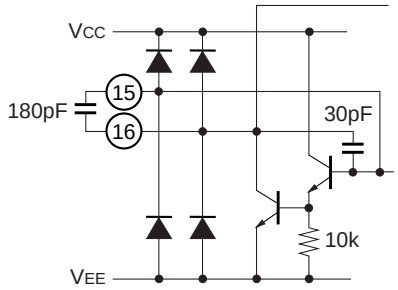
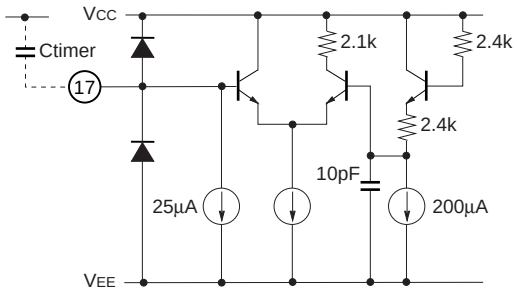
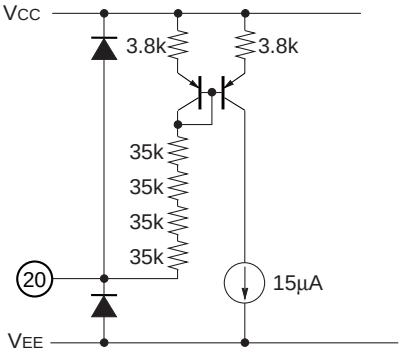


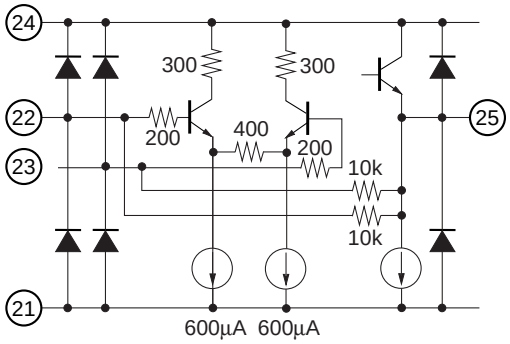
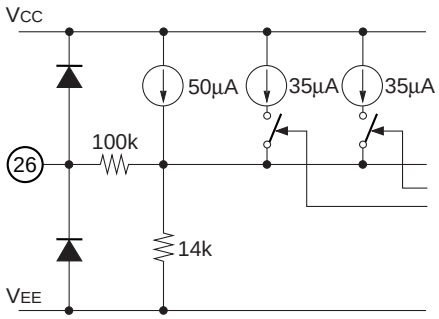
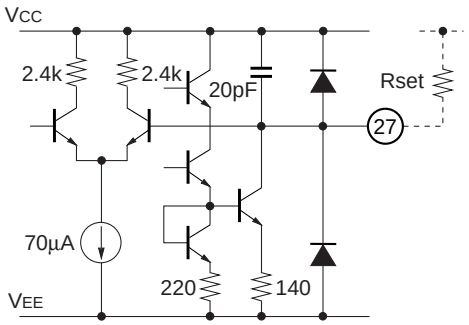
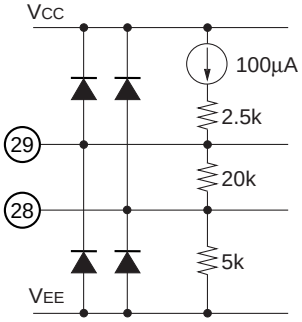
Pin Description

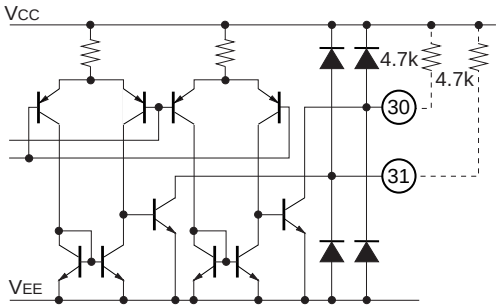
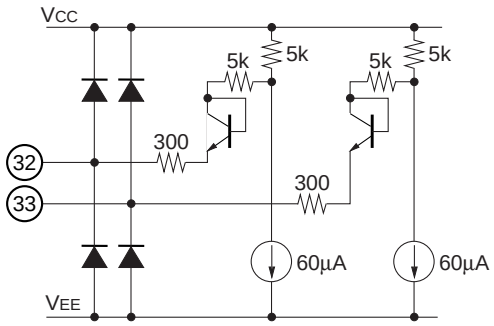
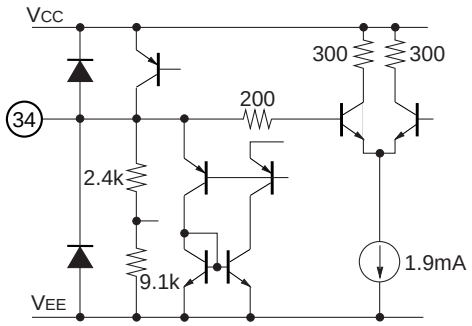
Pad No.	Symbol	Typical voltage [V]		Equivalent circuit	Description
		DC	AC		
1	$V_{CC}4$	3.3			Positive power supply pin for APC circuit.
2	$V_{EE}4$	0			Negative power supply pin for APC circuit.
3	BiasAdj	1.5 to 0			Sets Laser bias current pin.
4	SBias	0mA to 2.5mA			Sets Laser bias current or monitor pin.
5	Bias	0mA to 60mA			Laser bias current output pin. Open collector output.
6	$V_{EE}5$	0			Negative power supply pin for Bias circuit.
7	Q	1.3 to 3.3	6mA to 30mA*1 6mA to 50mA*2		Laser modulation current output pin. Open collector output.
8	QBX	1.3 to 3.3	6mA to 30mA*1 6mA to 50mA*2		Complementary current output pin. Q and QBX are not symmetrical output. Use Q output for Laser modulation.
9, 10	$V_{EE}1$	0			Negative power supply pin for Driver circuit.
11	$V_{CC}1$	3.3			Positive power supply pin for Driver circuit.
12	$V_{EE}1$	0			Negative power supply pin for Driver circuit.
13	DrvMon		0µA to 600µA		Sets Laser modulation current (IQ) monitor pin. IQ is monitored by connecting a resistor (Rmon) to this pin.
14	DrvAdj		0µA to 600µA		Sets Laser modulation current pin (IQ). IQ is controlled by connecting a resistor (Rdrv) to this pin. Refer to Fig.2.

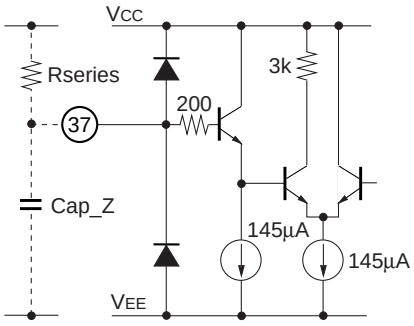
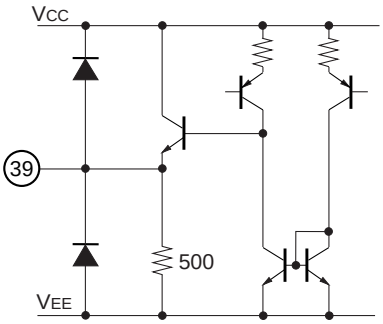
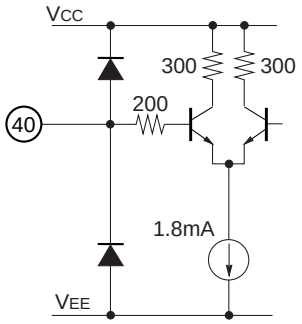
*1 Ta = –40 to 0°C

*2 Ta = 0 to +85°C

Pad No.	Symbol	Typical voltage [V]		Equivalent circuit	Description
		DC	AC		
15	CompA				Modulation current driver compensation pin. Normally, connects 180pF Capacitor across CompA and CompB pins.
16	CompB				
17	Timer				Capacitor port pin for activity detector (IN_ALM) operation. This pin set the period of inactive time for activity detector. Inactive time is controlled by connecting a capacitor to this pin. Refer to Fig.6.
18	NC				No Connect pin.
19	TM	1.5			Chip temperature monitor pin.
20	ADCDis	VEE to VCC (open)			This pin control the activity detector Circuit. High (connected to Vcc or open): an activity detector is disable. Low (connected to VEE): an activity detector is enable.
21	VEE2	0			Negative power supply pin for Data input circuit.

Pad No.	Symbol	Typical voltage [V]		Equivalent circuit	Description
		DC	AC		
22	DB		1.6 to 2.4		Differential PECL data inputs pins. These two inputs are internally biased by 10kΩ to V_{BB}.
23	D		1.6 to 2.4		
24	$V_{CC}2$	3.3			Positive power supply pin for Data input circuit.
25	V_{BB}	2			Reference bias voltage. (Option)
26	Indicate		0.7 to 1.7		The analog voltage high impedance output pin which indicate of whether the optical power of Laser diode is operated normal or not. The power output range has following relationship. High Light Indication; Vo ≥ 1.7V Nominal Operation; Vo = 1.2V Low Light Indication; Vo ≤ 0.7V
27	Tset				Selector for output duty cycle control pin. This pin controls the trailing edge of the input high pulse. Variable delay limit of that is from 0 to 0.2ns. Duty cycle is controlled by connected a resistor value between Vcc and this pin. Refer to Fig.1.
28	RSB	0.5			Window comparator top/bottom threshold voltage pin for LD_ALARM. The alarm (fail) threshold assert voltage can be set by the external resistor. Default voltages are RS equal to 2.5V and RSB equal to 0.5V.
29	RS	2.5			

Pad No.	Symbol	Typical voltage [V]		Equivalent circuit	Description
		DC	AC		
30	LDAlmB		0.2 to 3		Complementary open collector TTL outputs. Asserted when the fault is detected in the Laser monitor diode circuit.
31	LDAlm		0.2 to 3		
32	SDN		0 to 3.3		Complementary TTL inputs pin to disable output current. (shutdown input) When left open = "High"
33	SDNB		0 to 3.3		
34	V_{REF}	1.7			Temperature compensated reference voltage pin for APC. 1.7V (Constant for V_{EE} reference)
35	TEST_PIN	OPEN			Do not connect.
36	$V_{CC}3$	3.3			Positive power supply pin for Signal Detect circuit.

Pad No.	Symbol	Typical voltage [V]		Equivalent circuit	Description
		DC	AC		
37	CapZ				Capacitor and resistor port pins for slow start up. This pin controls the initial turn-on time of this IC (release time of bias and modulation current). The time for this function is set by an external RC network. Refer to Fig.7.
38	VEE3	0			Negative power supply pin for Signal Detect circuit.
39	APCOut				Output pin of APC OP-Amp. This signal control to bias adjust pins. (BiasAdj and SBias)
40	RsetPD				Monitor PD connect pin.

Electrical Characteristics

DC Electrical Characteristics

(V_{CC} = 3.14 to 3.46V, V_{EE} = 0V, Ta = –40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
DC Power supply voltage	Vdc	$V_{CC} – V_{EE}$	3.14	3.3	3.46	V
Power supply current	I_{EE}	I_Q = 0mA, I_{BIAS} = 0mA	–76	–59	—	mA
Modulation output current range	I_Q1	Ta = –40 to 0°C	6	—	30	
	I_Q2	Ta = 0 to +85°C	6	—	50	
Modulation output voltage range	V_Q		V_{CC} – 2	—	V_{CC}	V
Bias output current range	I_B		0	—	60	mA
Bias output voltage range	V_B		V_{CC} – 2	—	V_{CC}	V
Ratio of IB vs. Iset	IBvslset		14	22	27	—
ECL input High voltage	V_{EIH}		V_{CC} – 1.17	—	V_{CC} – 0.81	V
ECL input Low voltage	V_{EIL}		V_{CC} – 1.84	—	V_{CC} – 1.48	
SDN, SDNB, Reset input High voltage	V_{TIH}		2	—	V_{CC}	
SDN,SDNB, Reset input Low voltage	V_{TIL}		0	—	0.8	
LDA, LDAB output High voltage	V_{TOH}	I_{OH} = –10µA, R_L = 4.7kΩ	V_{CC} – 0.1	—	V_{CC} + 0.2	
LDA, LDAB output Low voltage	V_{TOL}	I_{OL} = 1mA, R_L = 4.7kΩ	0	—	0.4	
Reference bias voltage for OP Amp	V_{REF}		1.5	1.7	1.9	
Operating current range of V_{REF}	V_{REF}drv		–500	—	+500	µA

AC Electrical Characteristics

(V_{CC} = 3.14 to 3.46V, V_{EE} = 0V, Ta = –40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Data Rate	fdmax		1.25	—	—	Gbps
Rise time (20 to 80%)	tr	I_Q = 20mA, R_L = 25Ω	—	100	—	ps
Fall time (20 to 80%)	tf	I_Q = 20mA, R_L = 25Ω	—	200	—	
Max. variable High pulse width by duty cycle control	tdelay	Data rate = 1.25Gbps	0.2	—	—	ns
Max. setting time range of IN_Alarm	ts_alm		20	—	—	µs
Max. setting time range of POR	ts_por		150	—	—	
Shut down time	tsut_off		—	—	10	
Shut down recovery time	tsut_on		—	—	100	

DC and AC Electrical Characteristics for OpAmp of APC Circuitry

(V_{CC} = 3.14 to 3.46V, V_{EE} = 0V, Ta = –40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}		1.2	—	2.8	V
Output voltage range	V_O		0.6	—	2	V
Input bias current	I_B		—	7	—	µA
Input offset voltage	V_{OFF}		—	2.5	—	mV
Input offset Input current	I_{OFF}		—	0.7	—	µA
Input impedance	Z_{IN}		—	12	—	kΩ
Output drive current	I_O		–5.0	—	1.0	mA
Through rate	SR		—	1.9	—	V/µs
Open loop gain	Av		—	55	—	dB
Unity gain band-width	funit		—	20	—	MHz

Description of each function block

1. Data Buffer

Data Buffer is comprised of the data buffer and delay generator. ECL/PECL data is input to the data buffer at a maximum data rate of 1.25Gbps. This data is buffered and input to the delay circuitry. The delay circuitry adds a delay to the falling edge of the pulse up to a maximum of 0.2ns (Min.). The delay is set by a single external resistor between the delay set pin (Tset-Pin 27) and Vcc. A plot of the high pulse width vs. set resistance (Rset) is shown in Fig. 1.

2. V_{BB} Generator

This circuit provides a reference bias voltage to the data buffer for AC coupling inputs.

3. Modulation Current Generator

This circuit can sink up to 50mA of current to modulate the laser diode. The modulation current is set by an external resistor to Vcc at modulation current set pin (DrvAdj-Pin 14). There is also a modulation current monitor pin (DrvMon-Pin 13) that allows the IC user to monitor the modulation current. By putting an external fixed resistor between Vcc and DrvMon pin, you can monitor the modulation current by measuring the voltage of DrvMon pin. The modulation current and monitor current are in the rate of approximately 50:1 (Refer to Figs. 8 and 9). A plot of the modulation current vs. setting resistance (Rdrv) is shown in Fig. 2.

4. Laser Diode Bias Current Generator

This circuit is a very large current source capable of sourcing up to 60mA of current to bias the laser diode on. The circuit is a 22 to 1 (for current – current setting) current mirror that can be controlled externally two ways.
The first of these is to tie the BiasAdj (Pin 3) and SBias (Pin 4) terminals together and inject a current into the two terminals. The Bias (Pin 5) terminal is connected to the laser diode. Laser diode bias current vs. control current (Iset) characteristics is shown in Fig. 3.
The second method of controlling the laser diode current is to ties the SBias (Pin 4) terminal to Vcc and tune the BiasAdj (Pin 3) terminal with a voltage source. Varying the voltage at the BiasAdj terminal will vary the current through the laser diode. Laser diode bias current vs. control voltage characteristics is shown in Fig. 4.

5. APC (Automatic Power Control) Circuitry

The APC Circuitry is comprised of the window comparator, APC OpAmp, laser diode alarm circuit and the diode power indicator.
The APC OpAmp is normally configured as an inverting integrator. The inverting input is connected to the photo diode that monitors the light intensity from the laser diode. The photo diode converts the received light from the laser diode to a current. The output of the OpAmp then drives the laser diode current bias adjust pin, and the laser diode bias set pin is held at Vcc via a resistor. With the OpAmp configured as an inverting integrator, the OpAmp can tune the diode current inversely to the current in the photo diode. That is to say that if a low current is detected by the photo diode the integrator output goes up causing more bias current to go through the diode. If the photo diode current is high, then the output of the OpAmp will go low causing less bias current to flow through the laser diode.
The output of the APC OpAmp drives a window comparator. The function of the window comparator is to detect when the output of the APC OpAmp goes above or below a preset reference voltage for each comparator (RS, RSB). When this happens the comparators outputs cause the laser diode alarm circuit (LDAlm) to go high alerting the system that the laser diode current is either to high or to low.
The window comparator also drives the laser diode power indicator circuit (Indicate). This circuit is comprised of two switches and one fixed current sources. When the APC OpAmp output is such that the laser diode bias current is at its nominal set point, the output of the power indicator is at approximately 1.2Vdc. If the APC OpAmp output goes low, the output of the power indicator increases to approximately 1.7Vdc, indicating a high laser diode power condition. If the output of the APC OpAmp goes high, the output of the power indicator drops to approximately 0.7Vdc.
Also connected to the output of the window comparator is laser alarm circuitry. This circuit alerts the user of the device when the laser diode power level has risen either twice the normal set power or half the normal set power. A high voltage at the laser diode alarm output indicates an alarm event. The laser diode alarm output is disabled whenever a shutdown event is encountered.

6. Shutdown and Input Alarm Circuitry

This portion of the circuit disables both the modulation current driver and the laser diode bias generator under various conditions. The function block diagram for all of the shutdown mechanisms for the circuit is shown in Fig. 5. Shown below is the signal priority primarily for the reset function.

1) Power on Reset
2) Shutdown, Input Alarm

The Shutdown circuit has complementary TTL input to disable output current. Shown below is the desired truth table for the shutdown function.

SDN	SDNB	output current
Low	Low	Off
Low	High	On
High	Low	Off
High	High	Off

The Activity detector (In_ALM) circuit is designed to detect an input pulse transition. If there is no input pulse transition over a period time determined by the user, then the shutdown circuit is enabled causing the modulation current and laser bias current to be shutdown. Inactive time is set by external capacitor value between Timer pin (Pin 17) and V_{CC}. Inactive time vs. Ctimer is shown in Fig.6.

The Power on reset circuit is an inverting comparator that has an external RC network with CapZ pin (Pin 37) that is connected between Vcc and V_{EE}. At power up, the RC begins to charge up towards the reference voltage of the comparator. Since this is an inverting comparator the output will stay high until the capacitor charges above the reference. As long as the comparator output is high, the laser diode is disabled. As soon as the capacitor charges up beyond the reference, the output of the circuit goes low and the laser diode is enabled and ready for normal operation. A plot of the power on reset time vs. capacitance for a 10kΩ resistor (Rseries) is shown in Fig. 7.

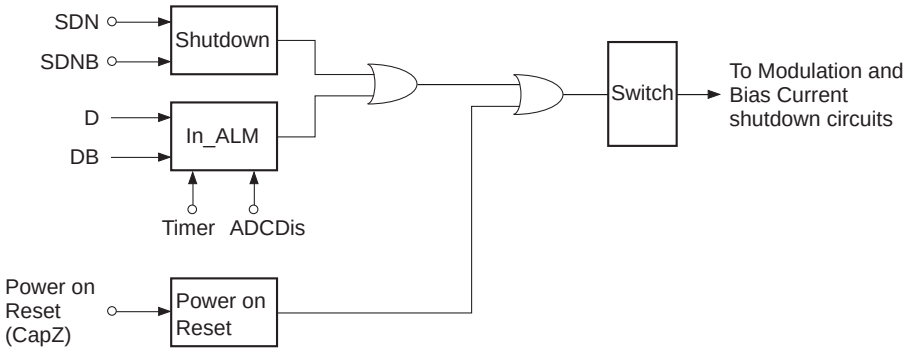


Fig.5. Shutdown and In_ALM Functional Block Diagram

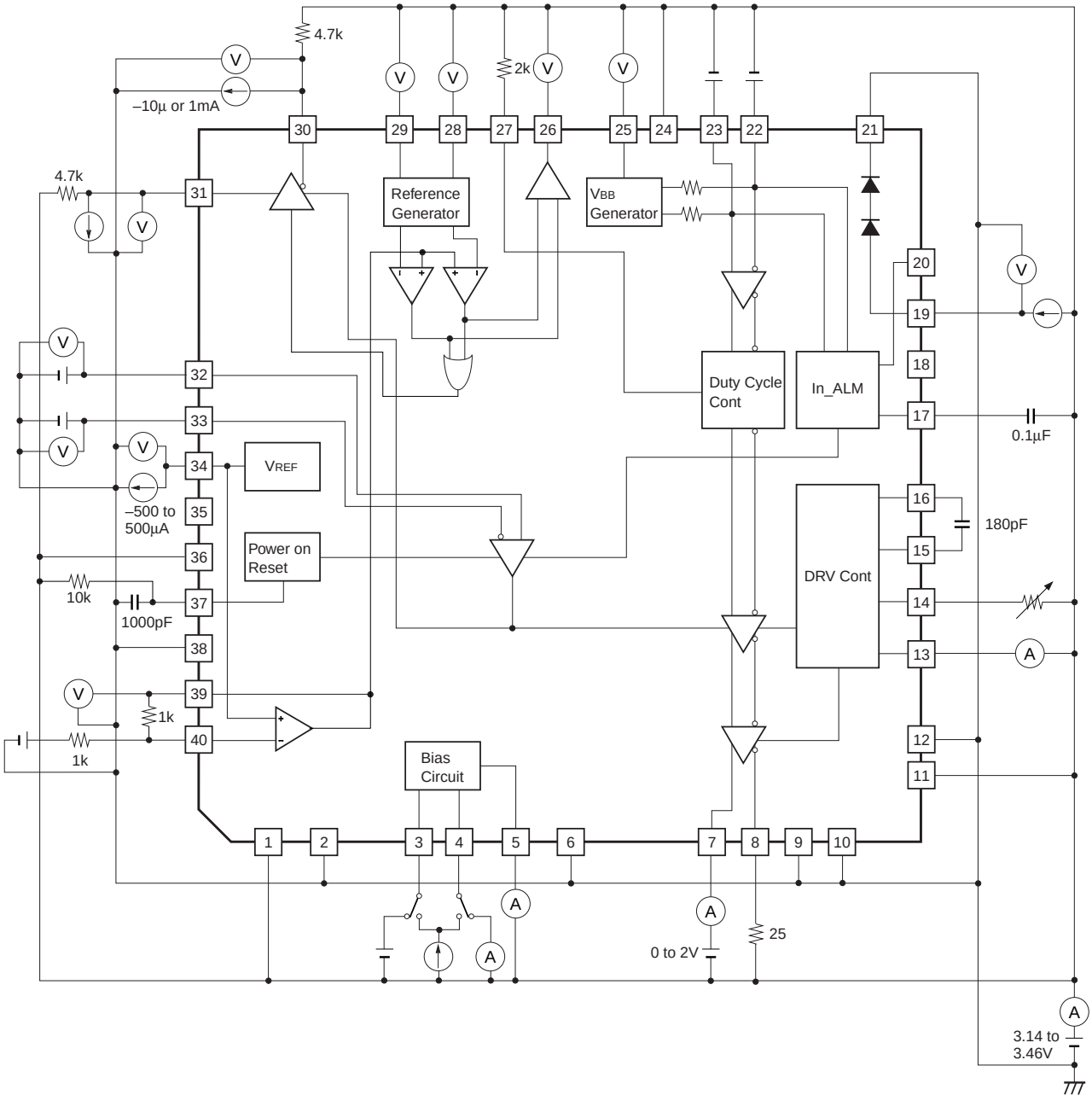
7. Others

Pay attention to handling this IC because its electrostatic discharge strength is weak.

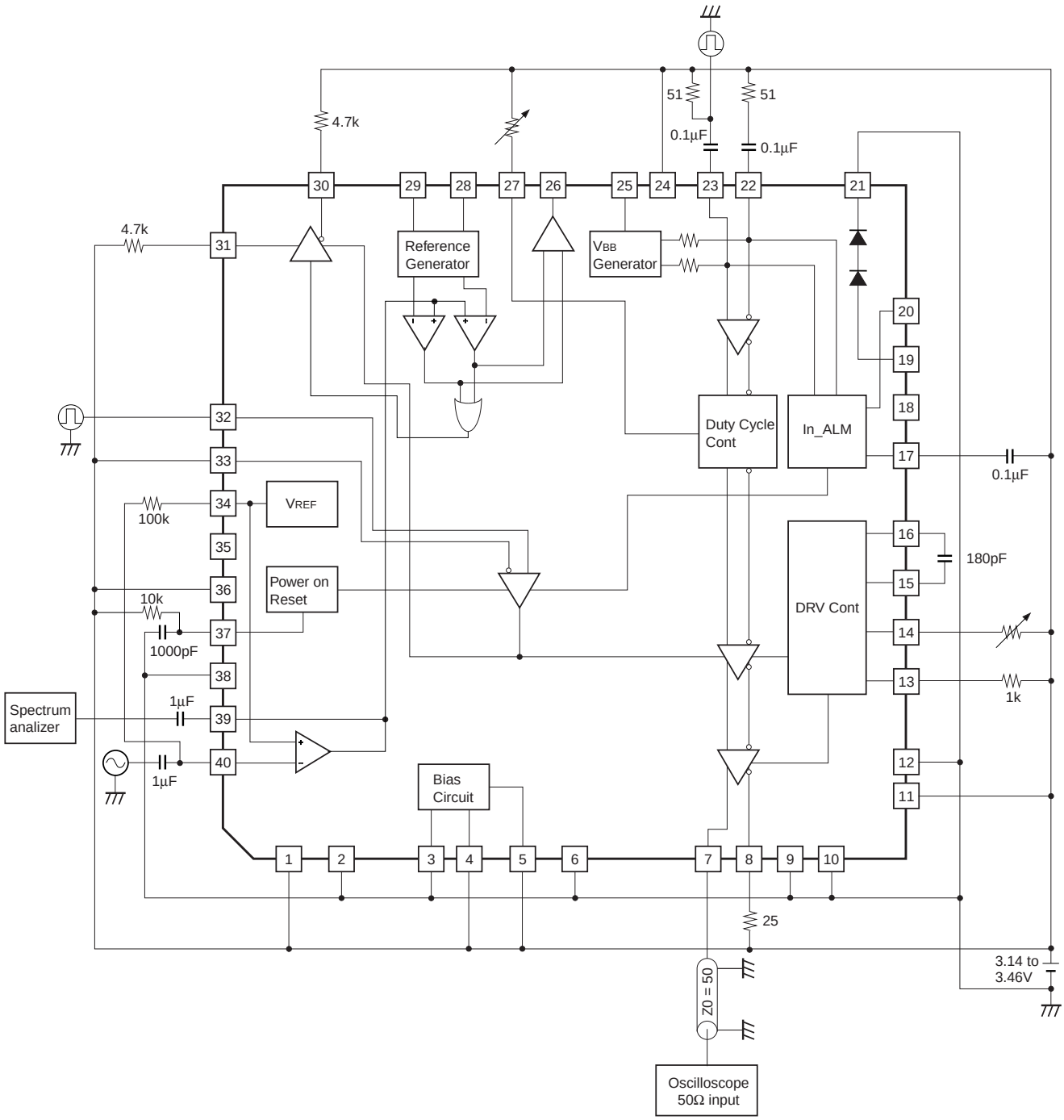
The Tset terminal (27pin) has to be connected through a resistor to Vcc.

Do not leave this pin open or connect to Vcc directly.

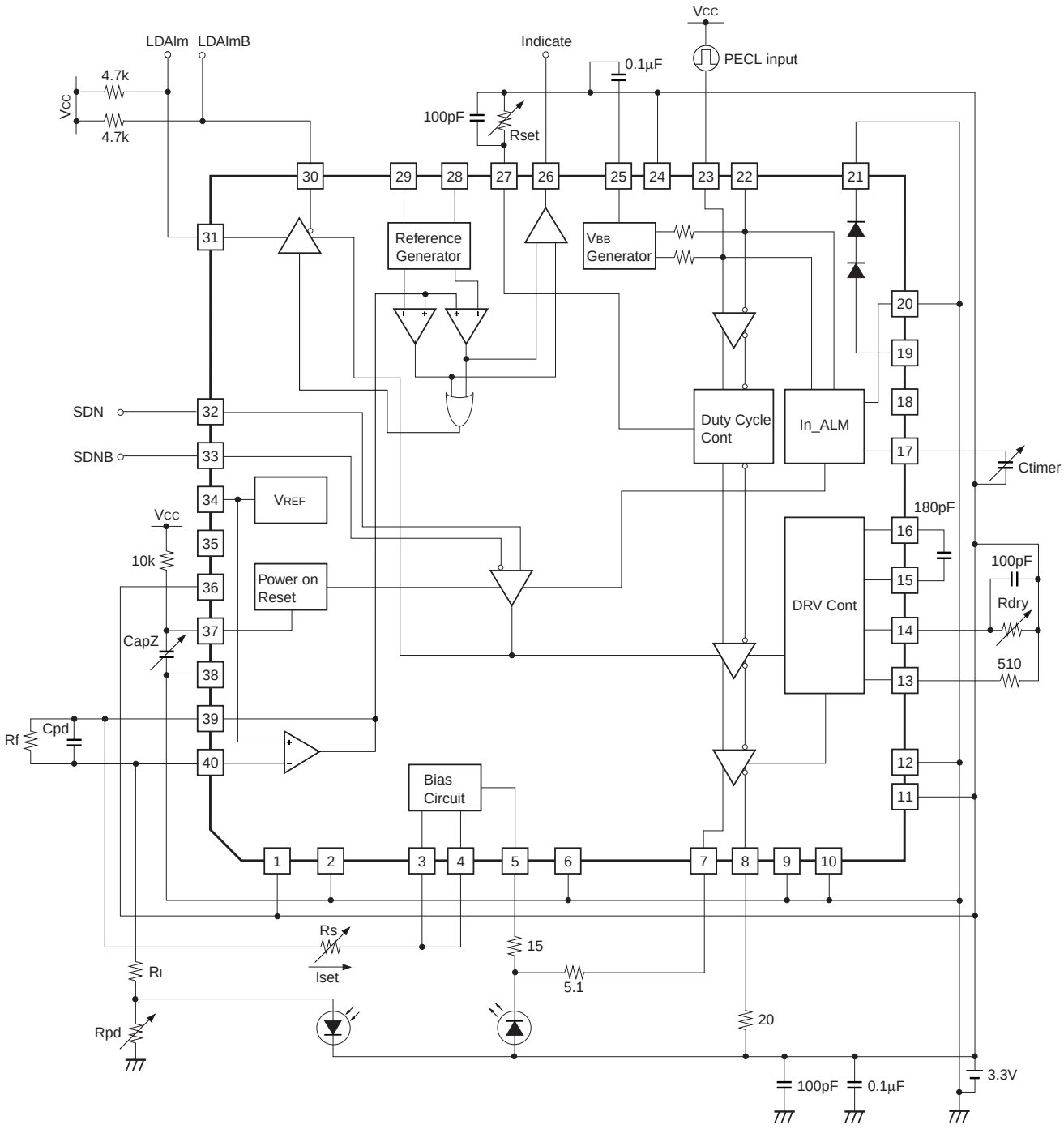
DC Electrical Characteristics Measurement Circuit



AC Electrical Characteristics Measurement Circuit



Application Circuit (at V_{CC} = 3.3V, V_{EE} = 0V)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

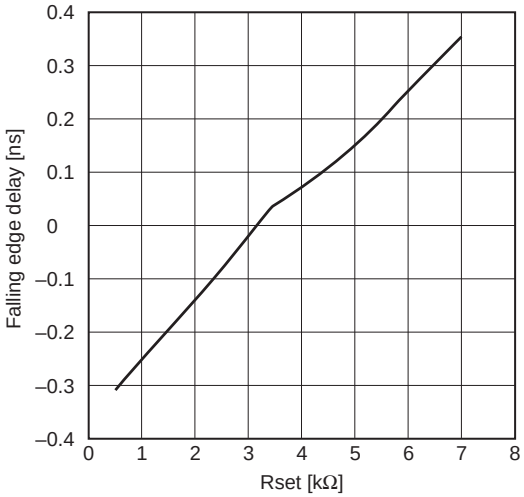


Fig. 1. Delay vs. Rset Characteristic at 1ns input data pulse apply

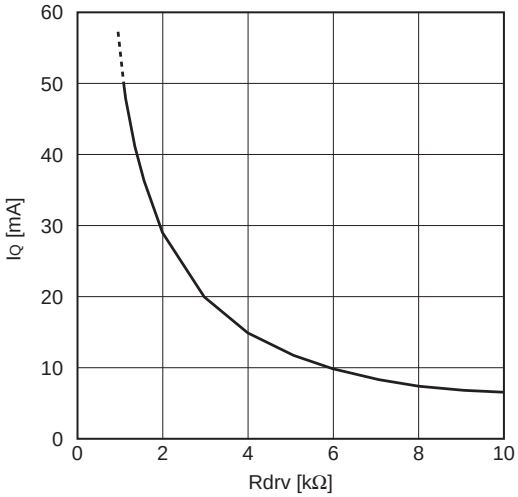


Fig. 2. Modulation Current (I_Q) vs. Rdrv Characteristics

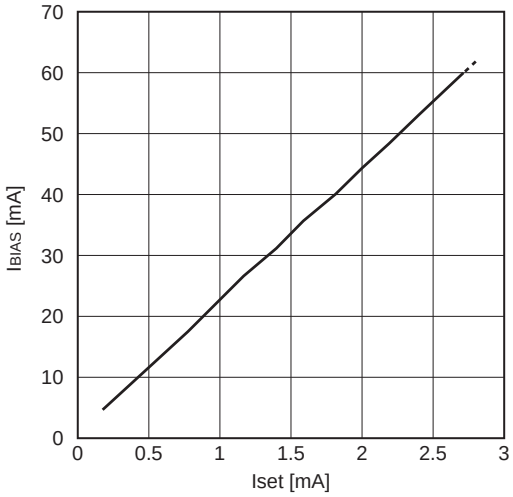


Fig. 3. Bias Current (I_{BIAS}) vs. Bias adjust current (Iset) Characteristics

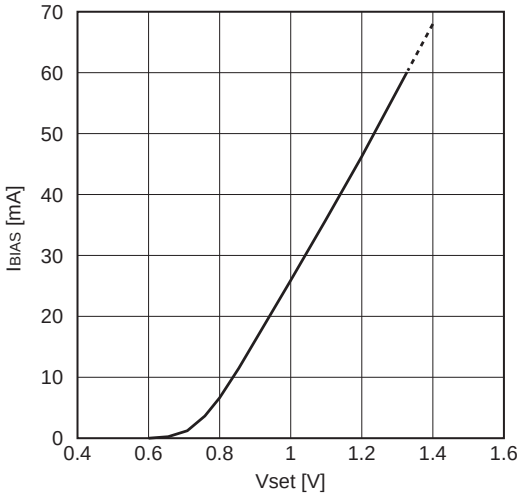


Fig. 4. Bias Current (I_{BIAS}) vs. Bias adjust voltage (Vset) Characteristics

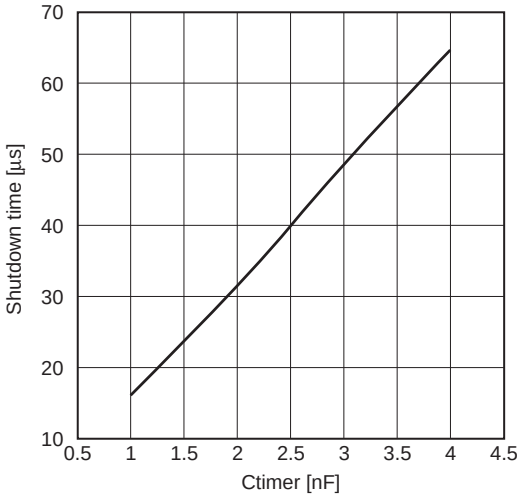


Fig. 6. Shutdown Time vs. Ctimer Characteristics

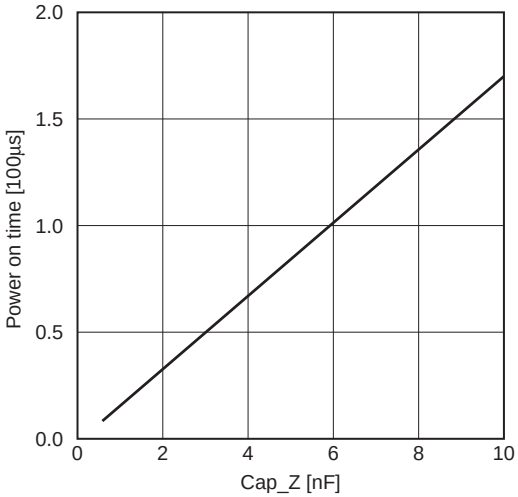


Fig. 7. Power on Reset Time vs. Cap_Z Characteristics (Rseries = 10kΩ)

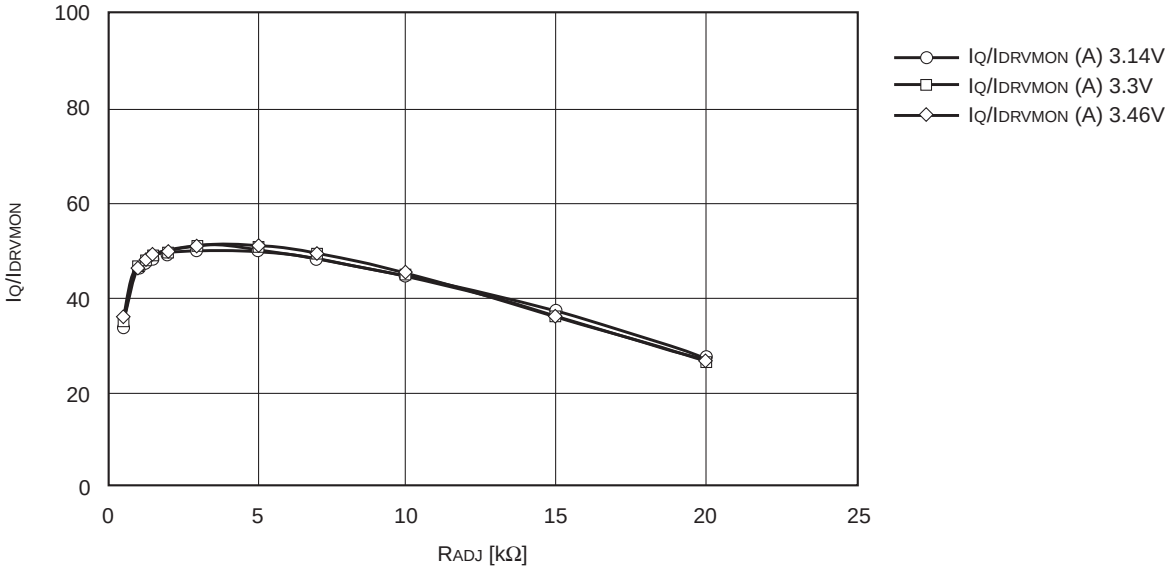


Fig. 8. Ratio of Modulation Current (I_Q)/Modulation Monitor Current (I_{DRVMON}) vs. Rdrv Characteristics (Electrical)

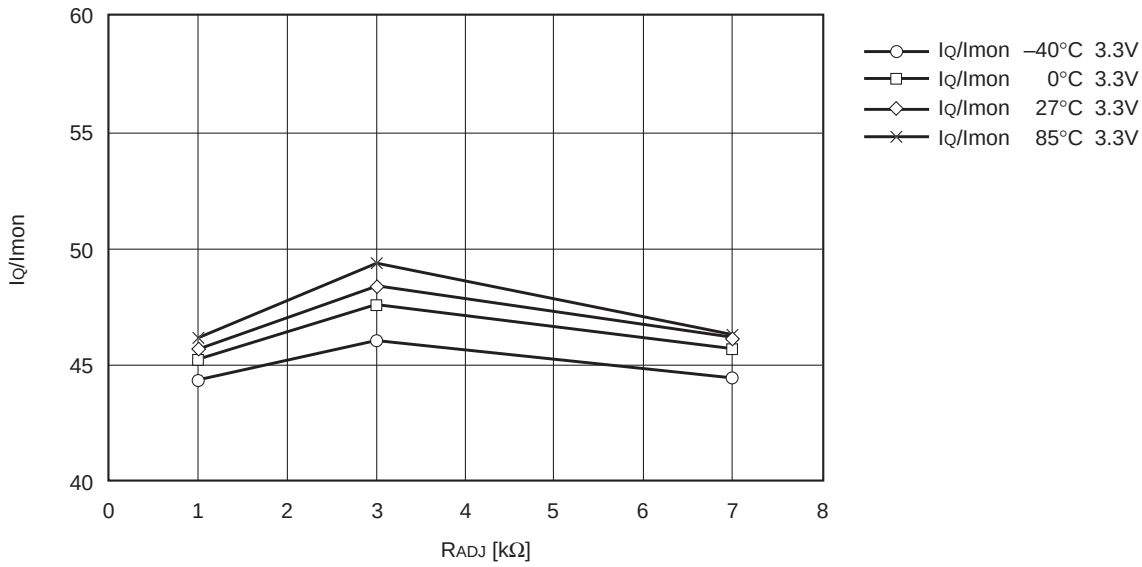
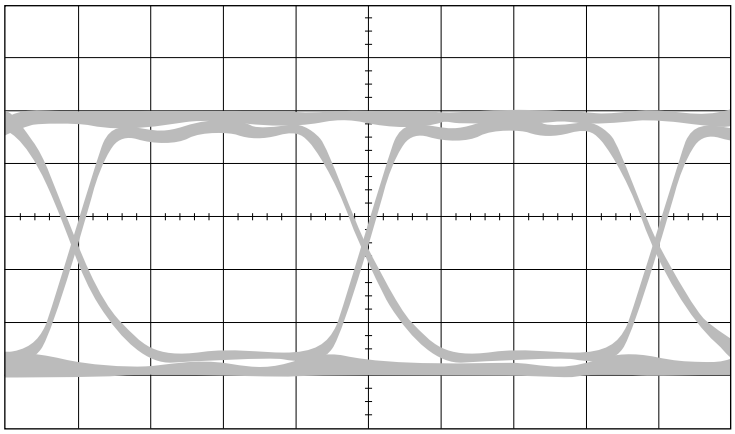


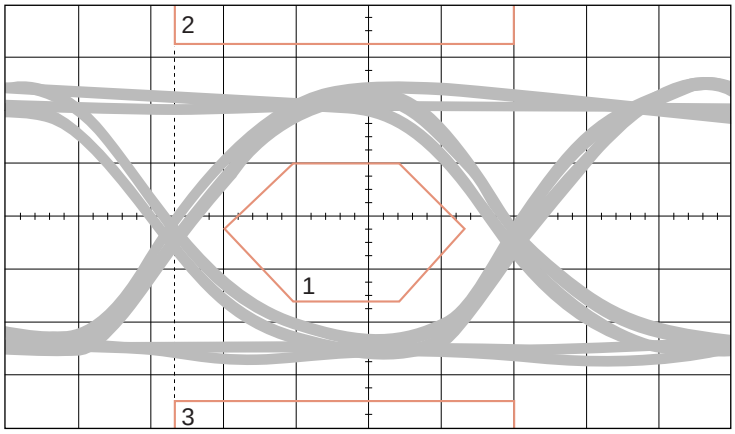
Fig. 9. Ratio of Modulation Current (I_Q)/Modulation Monitor Current (I_{DRVMON}) vs. Rdrv Characteristics (Temperature)



V_{CC} = 0V
V_{EE} = –3.3V
RL = 25Ω
Ta = 27°C
IQ = 30mA
Single input
Pattern = $PRBS2^{23} – 1$
Data Rate 1.25Gbps

Ch.1 :150mV/div, Offset: –300mV
Bandwidth: 20.0GHz
Time Base : 200ps/div

Fig. 10. Electrical Output Waveform



V_{CC} = 0V
V_{EE} = –3.3V
FP – LD (λ = 1330nm)
Ta = 27°C
Single Input
Pattern = $PRBS2^{23} – 1$
Data Rate 1.06Gbps
Filter (Cut Off 700Mbps)
Mask: FC1063

Ch.2 :5.0mV/div, Offset: 12.8mV
Bandwidth: 12.4GHz
Time Base:200ps/div

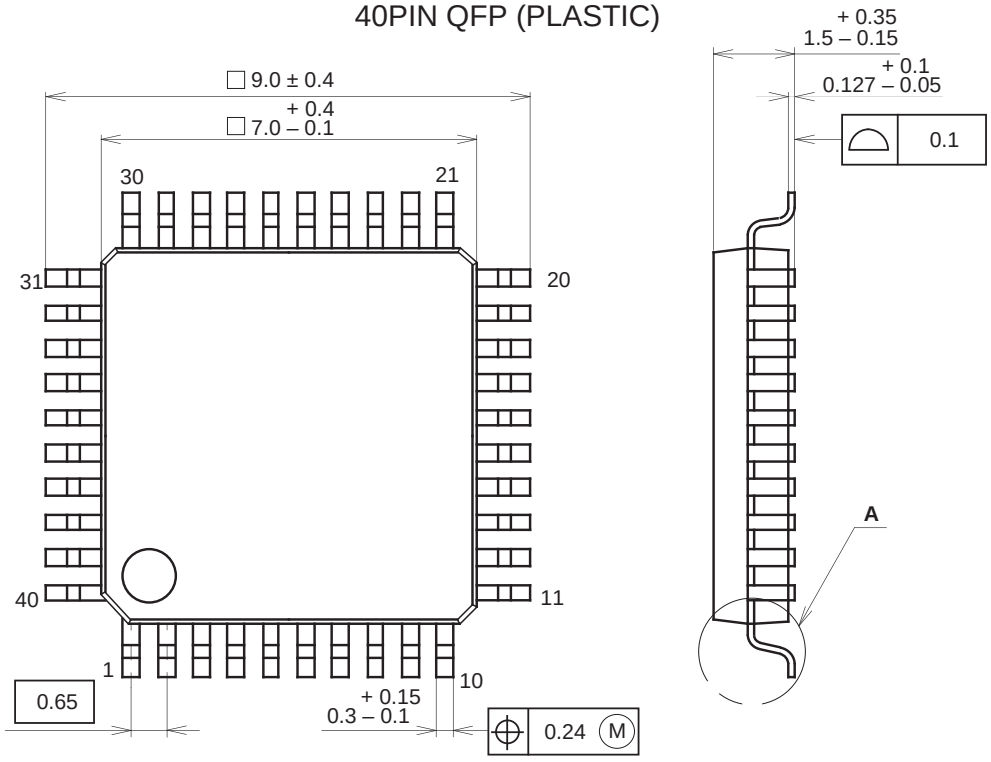
Fig. 11. Optical Output Waveform

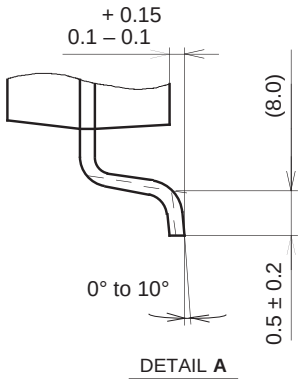
CXB1549Q

PIN#	PIN NAME	PIN#	PIN NAME
1	$V_{CC}4$	21	$V_{EE}2$
2	$V_{EE}4$	22	DB
3	BiasAdj	23	D
4	SBias	24	$V_{CC}2$
5	Bias	25	V_{BB}
6	$V_{EE}5$	26	Indicate
7	Q	27	Tset
8	QBX	28	RSB
9	$V_{EE}1$	29	RS
10	$V_{EE}1$	30	LDAlmB
11	$V_{CC}1$	31	LDAlm
12	$V_{EE}1$	32	SDN
13	DrvMon	33	SDNB
14	DrvAdj	34	V_{REF}
15	CompA	35	TEST_PIN
16	CompB	36	$V_{CC}3$
17	Timer	37	CapZ
18	NC	38	$V_{EE}3$
19	TM	39	APCOut
20	ADCDis	40	RsetPD

Package Outline Unit: mm

40PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-40P-L01
EIAJ CODE	QFP040-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).