HD66764

176-channel Common Driver for Color Displays

HITACHI

Rev.1.0
September, 2001

Description

The HD66764 is a common-driver LSI for systems with color-liquid-crystal dot-matrix graphic displays. It incorporates 176 LCD drive circuits and power-supply circuits. An external capacitor is also needed for the liquid crystal display.

This LSI, when used with the HD66763 384-channel segment driver with on-chip RAM, is suitable for color displays of cellular phones to a maximum of 128-by-176 dots.

Features

- LCD drive circuits
  — 176 outputs
- Internal power-supply circuit
  — Step-up circuit: twice to 12 times, positive-polarity inversion
  — Bias setting: 1/2 to 1/13, programmable
  — Contrast adjustment: 128-level programmable volume
  — Dividing resistors: built-in (controls the bias)
  — Setting: serial transfer from the HD66763 segment driver
- Low power consumption
- Power-supply voltage
  — Vcc = 1.8 to 3.6 V
- LCD drive voltage
  — VLCD-VEE = 10 to 44 V (VM standard: ± 5 to ± 2 2 V)
- Package
  — TCP and chip

Hitachi semiconductor

Type Number

Type Number	External Appearance
HD66764TB0	TCP
HCD66764BP	Die with Au bump

HD66764 PAD arrangement

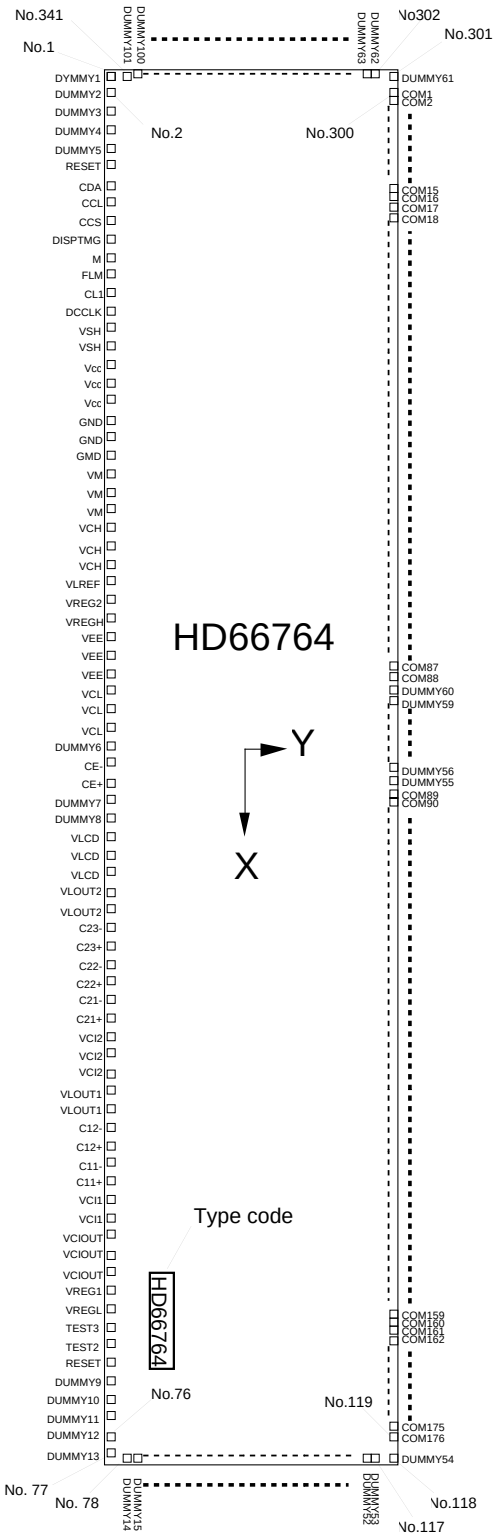
- Chip size : 10.2mm x 3.3mm
- Chip thickness : 550um (typ.)
- PAD coordinates : PAD center
- Coordinate origin : chip center
- Au bump size (PAD number is shown in the bracket) :

(1) 80um x 80um
DUMMY1(1) to DUMMY13(77)
DUMMY54(118), DUMMY61(301)

(2) 45um x 80um
COM1(300) to COM16(285)
COM161(134)to COM176(119)
DUMMY14(78) to DUMMY53(117)
DUMMY62(302) to DUMMY101(341)

(3)35um x 80um
COM17(284) to COM88(213)
DUMMY55(207) to DUMMY60(212)
COM89(206) to COM160(135)

- Au bump height : 15um (typ.)



HD66764 PAD Coordinate (Unit : um)

No	pad name	X	Y
1	DUMMY1	-4932	-1476
2	DUMMY2	-4699	-1476
3	DUMMY3	-4598	-1476
4	DUMMY4	-4498	-1476
5	DUMMY5	-4398	-1476
6	RESET	-4194	-1476
7	CDA	-4049	-1476
8	CCL	-3904	-1476
9	CCS	-3759	-1476
10	DISPTMG	-3615	-1476
11	M	-3470	-1476
12	FLM	-3325	-1476
13	CL1	-3180	-1476
14	DCCLK	-3035	-1476
15	VSH	-2824	-1476
16	VSH	-2724	-1476
17	VCC	-2624	-1476
18	VCC	-2524	-1476
19	VCC	-2424	-1476
20	GND	-2224	-1476
21	GND	-2124	-1476
22	GND	-2024	-1476
23	VM	-1823	-1476
24	VM	-1723	-1476
25	VM	-1623	-1476
26	VCH	-1423	-1476
27	VCH	-1323	-1476
28	VCH	-1223	-1476
29	VLREF	-1023	-1476
30	VREG2	-922	-1476
31	VREGH	-822	-1476
32	VEE	-622	-1476
33	VEE	-522	-1476
34	VEE	-422	-1476
35	VCL	-222	-1476
36	VCL	-122	-1476
37	VCL	-22	-1476
38	DUMMY6	179	-1476
39	CE-	279	-1476
40	CE+	379	-1476
41	DUMMY7	479	-1476
42	DUMMY8	579	-1476
43	VLCD	779	-1476
44	VLCD	879	-1476
45	VLCD	979	-1476
46	VLOUT2	1180	-1476
47	VLOUT2	1280	-1476
48	C23-	1380	-1476
49	C23+	1480	-1476
50	C22-	1580	-1476
51	C22+	1680	-1476
52	C21-	1780	-1476
53	C21+	1880	-1476
54	VCI2	2081	-1476
55	VCI2	2181	-1476
56	VCI2	2281	-1476
57	VLOUT1	2381	-1476
58	VLOUT1	2481	-1476
59	C12-	2581	-1476
60	C12+	2681	-1476
61	C11-	2781	-1476
62	C11+	2881	-1476
63	VCI1	2982	-1476
64	VCI1	3082	-1476
65	VCIOUT	3282	-1476
66	VCIOUT	3382	-1476
67	VCIOUT	3482	-1476
68	VREG1	3682	-1476
69	VREGL	3782	-1476
70	TEST3	3882	-1476
71	TEST2	3983	-1476
72	RESET	4194	-1476
73	DUMMY9	4398	-1476
74	DUMMY10	4498	-1476
75	DUMMY11	4598	-1476
76	DUMMY12	4699	-1476
77	DUMMY13	4932	-1476
78	DUMMY14	4932	-1159
79	DUMMY15	4932	-1099
80	DUMMY16	4932	-1039
81	DUMMY17	4932	-979
82	DUMMY18	4932	-919
83	DUMMY19	4932	-859
84	DUMMY20	4932	-798
85	DUMMY21	4932	-738
86	DUMMY22	4932	-678
87	DUMMY23	4932	-618
88	DUMMY24	4932	-558
89	DUMMY25	4932	-498
90	DUMMY26	4932	-438
91	DUMMY27	4932	-378
92	DUMMY28	4932	-318
93	DUMMY29	4932	-257
94	DUMMY30	4932	-197
95	DUMMY31	4932	-137
96	DUMMY32	4932	-77
97	DUMMY33	4932	-17
98	DUMMY34	4932	43
99	DUMMY35	4932	103
100	DUMMY36	4932	163
101	DUMMY37	4932	224
102	DUMMY38	4932	284
103	DUMMY39	4932	344
104	DUMMY40	4932	404
105	DUMMY41	4932	464
106	DUMMY42	4932	524
107	DUMMY43	4932	584
108	DUMMY44	4932	644
109	DUMMY45	4932	705
110	DUMMY46	4932	765
111	DUMMY47	4932	825
112	DUMMY48	4932	885
113	DUMMY49	4932	945
114	DUMMY50	4932	1005
115	DUMMY51	4932	1065
116	DUMMY52	4932	1125
117	DUMMY53	4932	1185
118	DUMMY54	4932	1474
119	COM176	4728	1474
120	COM175	4668	1474
121	COM174	4608	1474
122	COM173	4547	1474
123	COM172	4487	1474
124	COM171	4427	1474
125	COM170	4367	1474
126	COM169	4307	1474
127	COM168	4247	1474
128	COM167	4187	1474
129	COM166	4127	1474
130	COM165	4067	1474
131	COM164	4006	1474
132	COM163	3946	1474
133	COM162	3886	1474
134	COM161	3826	1474
135	COM160	3766	1474
136	COM159	3716	1474
137	COM158	3666	1474
138	COM157	3616	1474
139	COM156	3565	1474
140	COM155	3515	1474
141	COM154	3465	1474
142	COM153	3415	1474
143	COM152	3365	1474
144	COM151	3315	1474
145	COM150	3265	1474
146	COM149	3215	1474
147	COM148	3164	1474
148	COM147	3114	1474
149	COM146	3064	1474
150	COM145	3014	1474
151	COM144	2964	1474
152	COM143	2914	1474
153	COM142	2864	1474
154	COM141	2814	1474
155	COM140	2763	1474
156	COM139	2713	1474
157	COM138	2663	1474
158	COM137	2613	1474
159	COM136	2563	1474
160	COM135	2513	1474
161	COM134	2463	1474
162	COM133	2413	1474
163	COM132	2362	1474
164	COM131	2312	1474
165	COM130	2262	1474
166	COM129	2212	1474
167	COM128	2162	1474
168	COM127	2112	1474
169	COM126	2062	1474
170	COM125	2012	1474
171	COM124	1962	1474
172	COM123	1911	1474
173	COM122	1861	1474
174	COM121	1811	1474
175	COM120	1761	1474
176	COM119	1711	1474
177	COM118	1661	1474
178	COM117	1611	1474
179	COM116	1561	1474
180	COM115	1510	1474

HD66764 PAD Coordinate (Continue) (Unit : um)

No	pad name	X	Y
181	COM114	1460	1474
182	COM113	1410	1474
183	COM112	1360	1474
184	COM111	1310	1474
185	COM110	1260	1474
186	COM109	1210	1474
187	COM108	1160	1474
188	COM107	1109	1474
189	COM106	1059	1474
190	COM105	1009	1474
191	COM104	959	1474
192	COM103	909	1474
193	COM102	859	1474
194	COM101	809	1474
195	COM100	759	1474
196	COM99	708	1474
197	COM98	658	1474
198	COM97	608	1474
199	COM96	558	1474
200	COM95	508	1474
201	COM94	458	1474
202	COM93	408	1474
203	COM92	358	1474
204	COM91	307	1474
205	COM90	257	1474
206	COM89	207	1474
207	DUMMY55	125	1474
208	DUMMY56	75	1474
209	DUMMY57	25	1474
210	DUMMY58	-25	1474
211	DUMMY59	-75	1474
212	DUMMY60	-125	1474
213	COM88	-205	1474
214	COM87	-255	1474
215	COM86	-305	1474
216	COM85	-355	1474
217	COM84	-405	1474
218	COM83	-455	1474
219	COM82	-506	1474
220	COM81	-556	1474
221	COM80	-606	1474
222	COM79	-656	1474
223	COM78	-706	1474
224	COM77	-756	1474
225	COM76	-806	1474
226	COM75	-856	1474
227	COM74	-907	1474
228	COM73	-957	1474
229	COM72	-1007	1474
230	COM71	-1057	1474
231	COM70	-1107	1474
232	COM69	-1157	1474
233	COM68	-1207	1474
234	COM67	-1257	1474
235	COM66	-1308	1474
236	COM65	-1358	1474
237	COM64	-1408	1474
238	COM63	-1458	1474
239	COM62	-1508	1474
240	COM61	-1558	1474

No	pad name	X	Y
241	COM60	-1608	1474
242	COM59	-1658	1474
243	COM58	-1709	1474
244	COM57	-1759	1474
245	COM56	-1809	1474
246	COM55	-1859	1474
247	COM54	-1909	1474
248	COM53	-1959	1474
249	COM52	-2009	1474
250	COM51	-2059	1474
251	COM50	-2110	1474
252	COM49	-2160	1474
253	COM48	-2210	1474
254	COM47	-2260	1474
255	COM46	-2310	1474
256	COM45	-2360	1474
257	COM44	-2410	1474
258	COM43	-2460	1474
259	COM42	-2510	1474
260	COM41	-2561	1474
261	COM40	-2611	1474
262	COM39	-2661	1474
263	COM38	-2711	1474
264	COM37	-2761	1474
265	COM36	-2811	1474
266	COM35	-2861	1474
267	COM34	-2911	1474
268	COM33	-2962	1474
269	COM32	-3012	1474
270	COM31	-3062	1474
271	COM30	-3112	1474
272	COM29	-3162	1474
273	COM28	-3212	1474
274	COM27	-3262	1474
275	COM26	-3312	1474
276	COM25	-3363	1474
277	COM24	-3413	1474
278	COM23	-3463	1474
279	COM22	-3513	1474
280	COM21	-3563	1474
281	COM20	-3613	1474
282	COM19	-3663	1474
283	COM18	-3713	1474
284	COM17	-3764	1474
285	COM16	-3824	1474
286	COM15	-3884	1474
287	COM14	-3944	1474
288	COM13	-4004	1474
289	COM12	-4064	1474
290	COM11	-4124	1474
291	COM10	-4184	1474
292	COM9	-4245	1474
293	COM8	-4305	1474
294	COM7	-4365	1474
295	COM6	-4425	1474
296	COM5	-4485	1474
297	COM4	-4545	1474
298	COM3	-4605	1474
299	COM2	-4665	1474
300	COM1	-4725	1474

No	pad name	X	Y
301	DUMMY61	-4932	1474
302	DUMMY62	-4932	1185
303	DUMMY63	-4932	1125
304	DUMMY64	-4932	1065
305	DUMMY65	-4932	1005
306	DUMMY66	-4932	945
307	DUMMY67	-4932	885
308	DUMMY68	-4932	825
309	DUMMY69	-4932	765
310	DUMMY70	-4932	705
311	DUMMY71	-4932	644
312	DUMMY72	-4932	584
313	DUMMY73	-4932	524
314	DUMMY74	-4932	464
315	DUMMY75	-4932	404
316	DUMMY76	-4932	344
317	DUMMY77	-4932	284
318	DUMMY78	-4932	224
319	DUMMY79	-4932	163
320	DUMMY80	-4932	103
321	DUMMY81	-4932	43
322	DUMMY82	-4932	-17
323	DUMMY83	-4932	-77
324	DUMMY84	-4932	-137
325	DUMMY85	-4932	-197
326	DUMMY86	-4932	-257
327	DUMMY87	-4932	-318
328	DUMMY88	-4932	-378
329	DUMMY89	-4932	-438
330	DUMMY90	-4932	-498
331	DUMMY91	-4932	-558
332	DUMMY92	-4932	-618
333	DUMMY93	-4932	-678
334	DUMMY94	-4932	-738
335	DUMMY95	-4932	-798
336	DUMMY96	-4932	-859
337	DUMMY97	-4932	-919
338	DUMMY98	-4932	-979
339	DUMMY99	-4932	-1039
340	DUMMY100	-4932	-1099
341	DUMMY101	-4932	-1159

Pin Functions

Table 1 Pin Functions

Signal Name	Quantity	Input/ Output	Connected to	Function
Vcc	1	-	Power supply	VCC-GND: Logic-circuit power supply. Supply the same voltage as for the HD66763.
GND	1	-	Power supply	
VLCD	1	-	Power supply or VLOUT2	LCD-drive-circuit power supply, positive side.
VEE	1	-	Power supply or VCL	LCD-drive-circuit power supply, negative side.
VciOUT	1	-	Vci1 and capacitor for stabilization or open	Outputs a regulated voltage derived from Vcc. Connect a capacitor for stabilization. When this pin is not used, leave it open.
Vci1	1	-	VciOUT or power supply	Voltage-input pin for step-up circuit 1. When the Vci adjuster is used, input the power supply from VciOUT. When not used, input the external power supply.
Vci2	1	-	VLOUT1 or power supply	Voltage-input pin in step-up circuit 2. When the internal step-up circuit is not used, leave this pin open.
VCH VSH VM VCL	4	-	Capacitor for stabilization and VSH of HD66763 or external power supply	When the internal power supply circuit is used, the LCD-drive-level power supply is output here. VCH, VM, and VCL are used for the common driver, and VSH for the segment driver. Connect a capacitor for stabilization of the display quality. When the internal power-supply circuit is not used, connect the output of the external power-supply circuit. However, VSH need not be supplied.
VLOUT1	1	-	Step-up capacitance/ Vci2 pin	A voltage that doubles or triples the voltage between Vci1 and GND is output here. The step-up factor can be set in an internal register.
VLOUT2	1	-	Step-up capacitance/ VLCD pin	A voltage that is boosted from the voltage between Vci1/Vci2 and GND is output here. The step-up factor can be set in an internal register.
C11+, C11- to C23+, C23-	10	-	Step-up capacitance or open	Connect a step-up capacitor according to the step-up factor. When the internal step-up circuit is not used, leave this pin open.
CE+, CE-	2	-	Step-up capacitance or open	Connect a step-up capacitor for generating the VCL level from the VCH and VM levels. When the internal step-up circuit is not used, leave this pin open.

Table 1 Pin Functions (cont)

Signal Name	Quantity	Input/ Output	Connected to	Function
VREGL	1	-	External reference voltage	Reference voltage input. Connect an external reference voltage. Input current is not supplied from this pin. Therefore, External voltage can be generated by regulator which uses divided resistor.
VREG1	1	-	VREGH	A voltage that doubles, triples, quadruples, or quintuples the voltage on VREGL is output here.
VREGH	1	-	VREG1	Connects the output of VREG1.
VREG2	1	-	VLREF or open	A voltage that doubles, triples, quadruples, or quintuples the voltage on VREGH is output here.
VLREF	1	-	VREG2 or external power supply	Input for the LCD drive voltage. When the internal amplification circuit is used, the output of VREG2 is connected here. When the circuit is not used, supply external power.
RESET1*/ RESET2*	2	Input	External reset circuit	Reset pin. When a low level is input here, the LSI is reinitialized. Be sure to apply a signal to this pin during the system's power-on reset. RESET1* and RESET2* are equivalent. So apply a signal to either pin as required and leave the other pin open.
CL1	1	Input	CL1 of HD66763	Clock input pin. The output of the LCD changes on the falling edge of this signal.
FLM	1	Input	FLM of HD66763	Frame-synchronization with the segment driver.
M	1	Input	M of HD66763	Inputs the current-alternating signal from the LCD output. When output is selected, the following levels are output: Low: VCL, high: VCH When output is not selected, VM is output.
DISPTIMG	1	Input	DISPTMG of HD66763	A display timing signal. DISPTMG = 1: display, DISPTMG = 0: non-display
DCCLK	1	Input	DCCLK of HD66763	A clock for the step-up circuit that is supplied from HD66763.
CCL	1	Input	CCL of HD66763	Operates as a clock for the transfer of register settings. Latches data on the rising edge of the clock.
CDA	1	Input	CDA of HD66763	Operates as the data for the transfer of register settings.
CCS*	1	Input	CCS* of HD66763	A chip-select signal. Low: selected (data-transfer enabled), high: not selected (data-transfer disabled)

Table 1 Pin Functions (cont)

Signal Name	Quantity	Input/ Output	Connected to	Function
COM1 to COM176	176	Output	Liquid crystal	Signals to drive the common lines. Output either of VCL, VCH, or VM levels. When selected, VCH or VCL is output. When not selected, VM is output. When the display is off, the GND level is output.
TEST2, TEST3	2	Output	Open	Test pins. Leave these pins open.

Internal Block Diagram

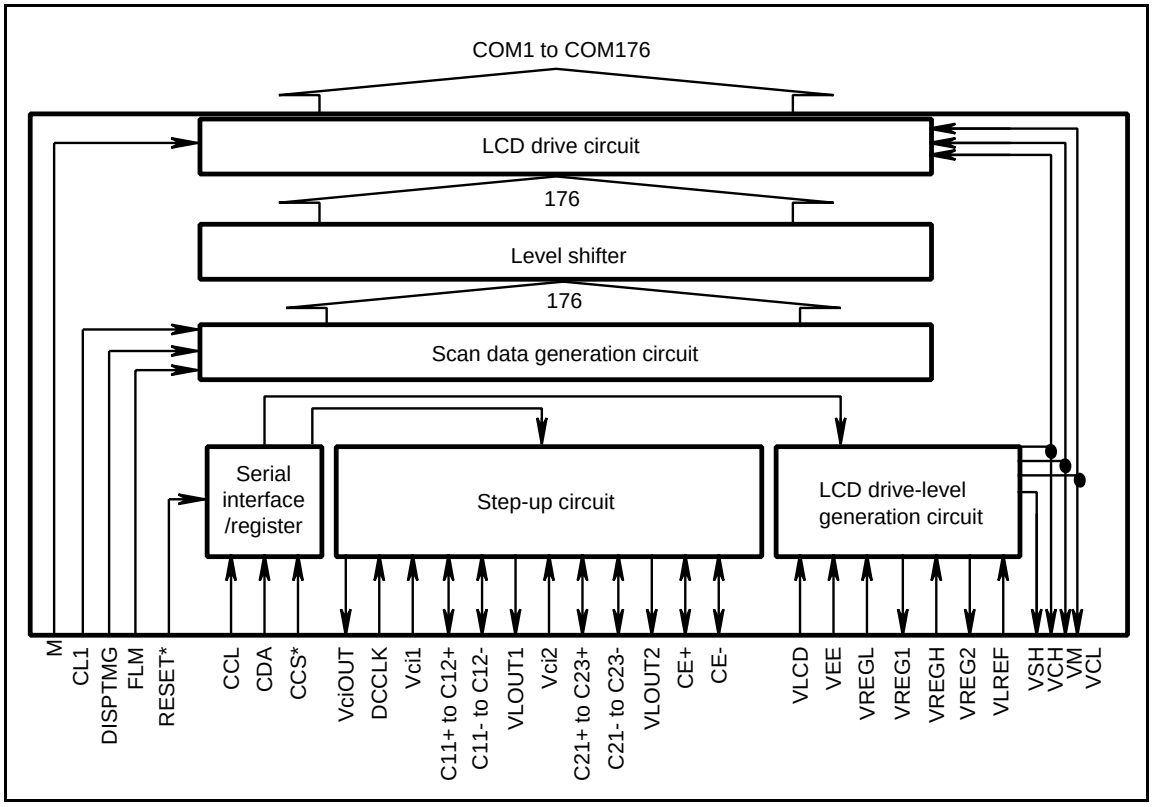


Figure 1 Block Diagram

1. Step-up circuit

Boosts the Vci1 voltage by from two to 12 times. The required voltage is generated by combining double or triple step-up and double, triple, or quadruple step-up. The factor is controlled by register settings. A negative-polarity voltage is also generated. For details, refer to the section on the LCD Voltage Generation Circuit.

2. LCD-drive-level generation circuit

Generates the VCH, VSH, VM, or VCL levels required to drive the LCDs. The VSH level is supplied to the HD66763.

3. Interface circuit

Transfers the data to the internal control register.

4. Scan data generation circuit

Produces the output signals for the common lines at logic levels, as selected and in the selected direction, in synchronization with the FLM signal.

5. Level shifter

Shifts the level from Vcc-GND power supply for operation of the logic circuits to VLCD-VEE for the LCD drive circuit.

6. LCD drive circuit

Outputs one of VCH, VM, or VCL according to the combination of data and the M signal from the scan data generation circuit.

Instructions

Outline

The HD66764 has seven internal registers. The data is written to these registers by using a common serial data interface. This interface can be directly connected with the HD66763 segment driver for the automatic transfer of instructions. When an instruction is written to the HD66763 via the bus from the CPU, it is output from the serial interface of the HD66763, and the HD66764 receives the instruction to make a setting in one of its internal registers.

In the bit configuration for the transfer of instructions, the upper three bits are index numbers that indicate the target register of the transfer, and the lower 13 bits are the data.

Detailed Description

Power Control 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	BS2	BS1	BS0	BT3	BT2	BT1	BT0	DC2	DC1	DC0	AP1	AP0	SLP
Index code															

Figure 2 Power Control 1 Instruction

BS2-0: Set the LCD drive bias within the range from 1/2 to 1/13. Set the bias according to the LCD drive duty cycle and LCD drive voltage.

BT3-0: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the LCD drive duty and power-supply voltage to be used. Set the output of VLOUT1 to 5.5 V or lower.

DC2-0: Set the step-up cycle of the step-up circuit. When the cycle is accelerated, the driving ability of the step-up circuit becomes high, but its current consumption is increased, too. Adjust the cycle with consideration of the display quality and the current consumption.

AP1-0: Adjust the amount of fixed current from the fixed current source in the operational amplifier circuit for the LCD drive-level power. When the amount of fixed current becomes large, the LCD driving ability and the quality of the display become high, but the current consumption is increased. Adjust the fixed current with consideration of the display quality and the current consumption. During times when there is no display, such as in the sleep or standby modes, AP1-0 can be set to (0, 0) and the current consumption is reduced by shutting the operational amplifier down.

SLP: Sets the sleep mode. When SLP = 1, bits AP1/0 and DISP in the first-screen driving-control register are all fixed to 0. This stops the operation of the power-supply circuit and turns off the display at the same time. The state of SLP bit does not change the values of these bits.

Table 2 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	LCD Drive Bias Value
0	0	0	1/13 bias
0	0	1	1/12 bias
0	1	0	1/11 bias
0	1	1	1/10 bias
1	0	0	1/9 bias
1	0	1	1/8 bias
1	1	0	1/4 bias
1	1	1	1/2 bias

Table 3 BT Bits and VLOUT1 and VLOUT2 Outputs

BT3	BT2	BT1	BT0	VLOUT1 Output	VLOUT2 Output
0	0	0	0	2 x Vci1	2 x Vci2
0	0	0	1	3 x Vci1	2 x Vci2
0	0	1	0	2 x Vci1	3 x Vci2
0	0	1	1	3 x Vci1	3 x Vci2
0	1	0	0	2 x Vci1	4 x Vci2
0	1	0	1	3 x Vci1	4 x Vci2
0	1	1	0	2 x Vci1	Step-up stopped
0	1	1	1	3 x Vci1	Step-up stopped
1	0	0	0	2 x Vci1	Vci1 + Vci2
1	0	0	1	3 x Vci1	Vci1 + Vci2
1	0	1	0	2 x Vci1	Vci1 + 2 x Vci2
1	0	1	1	3 x Vci1	Vci1 + 2 x Vci2
1	1	0	0	2 x Vci1	Vci1 + 3 x Vci2
1	1	0	1	3 x Vci1	Vci1 + 3 x Vci2
1	1	1	0	2 x Vci1	Vci2
1	1	1	1	3 x Vci1	Vci2

Table 4 DC Bits and Step-up Cycle

DC2	DC1	DC0	Step-up Cycle in Step-up Circuit 1	Step-up Cycle in Step-up Circuit 2/3
0	0	0	DCCLK	DCCLK
0	0	1	DCCLK divided by two	DCCLK
0	1	0	DCCLK	DCCLK divided by two
0	1	1	DCCLK divided by two	DCCLK divided by two
1	0	0	DCCLK	DCCLK divided by three
1	0	1	DCCLK divided by two	DCCLK divided by three
1	1	0	DCCLK	DCCLK divided by four
1	1	1	DCCLK divided by two	DCCLK divided by four

Table 5 AP Bits and Amount of Current in Operational Amplifier

AP1	AP0	Amount of Current in Operational Amplifier
0	0	Operation of the operational amplifier and step-up circuit are stopped.
0	1	Small
1	0	Medium
1	1	Large

Power Control 2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0

Index code

Figure 3 Power Control 2 Instruction

VC2-0: Adjust the VciOUT voltage to fraction of Vcc. The voltage of VLOUT1 can be controlled when VciOUT is connected to Vci1. When VC2 = 1, the Vci1 amplifier operation is stopped, and any voltage can be externally applied to the Vci1 pin.

Table 6 VC Bits and Vci Adjustment Reduction Factor

VC2	VC1	VC0	Adjusted Vci Magnification Factor
0	0	0	0.92 x Vcc
0	0	1	0.83 x Vcc
0	1	0	0.76 x Vcc
0	1	1	0.68 x Vcc
1	*	*	No amplification of Vci1 (external input to Vci1).

Contrast Adjustment

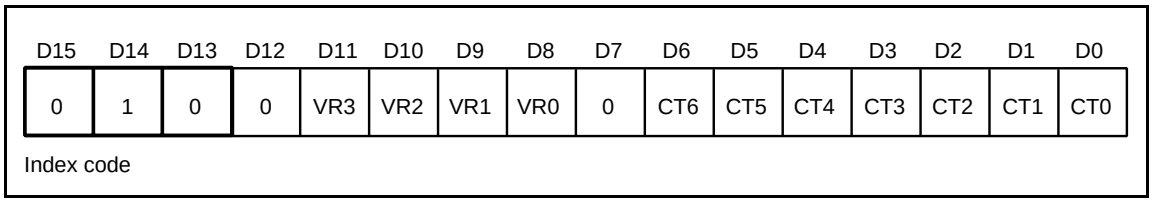


Figure 4 Contrast Adjustment Instruction

CT6-0: Control the LCD drive voltage to adjust contrast to one of 128 steps.

VR3-0: Amplifies the output voltage (VREG2) in the LCD-drive reference-voltage generator to from four to 25 times the voltage on VREGL. The value of VREG1 must not exceed 5.5 V.

Table 7 CT Bits and Contrast

Value to be Set to CT Bits							
CT6	**CT5**	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**	**Contrast**
0	0	0	0	0	0	0	3.84R (minimum)
0	0	0	0	0	0	1	3.81R
0	0	0	0	0	1	0	3.78R
0	0	0	0	0	1	1	3.75R
0	0	0	0	1	0	0	3.72R
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0.06R (maximum)
1	1	1	1	1	1	1	0.03R (maximum)

Table 8 VR Bits and VREG and VLREF Voltages

VR3	VR2	VR1	VR0	VREG1 Voltage	VREG2 Voltage	VLREF Voltage
0	0	0	0	VREGL x 2	VREGH x 2	VREGL x 4
0	0	0	1	VREGL x 3	VREGH x 2	VREGL x 6
0	0	1	0	VREGL x 4	VREGH x 2	VREGL x 8
0	0	1	1	VREGL x 5	VREGH x 2	VREGL x 10
0	1	0	0	VREGL x 2	VREGH x 3	VREGL x 6
0	1	0	1	VREGL x 3	VREGH x 3	VREGL x 9
0	1	1	0	VREGL x 4	VREGH x 3	VREGL x 12
0	1	1	1	VREGL x 5	VREGH x 3	VREGL x 15
1	0	0	0	VREGL x 2	VREGH x 4	VREGL x 8
1	0	0	1	VREGL x 3	VREGH x 4	VREGL x 12
1	0	1	0	VREGL x 4	VREGH x 4	VREGL x 16
1	0	1	1	VREGL x 5	VREGH x 4	VREGL x 20
1	1	0	0	VREGL x 2	VREGH x 5	VREGL x 10
1	1	0	1	VREGL x 3	VREGH x 5	VREGL x 15
1	1	1	0	VREGL x 4	VREGH x 5	VREGL x 20
1	1	1	1	VREGL x 5	VREGH x 5	VREGL x 25

1st Screen Driving Position

2nd Screen Driving Position

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	DISP	CMS	SPT	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
1	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
1	0	1	0	0	0	0	0	SS27	SS27	SS25	SS24	SS23	SS22	SS21	SS20
1	1	0	0	0	0	0	0	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20

Index code

Figure 5 1st and 2nd Screen Driving Position Instruction

DISP: Controls the display operation. When DISP = 0, the GND level is output from all common outputs. When the GND level is output, the segment output can turn the display off. When DISP = 1, the display operates.

CMS: Selects the scan direction for output of the common driver. When CMS = 0, a direction is from COM1 to COM176, and, when CMS = 1, it is from COM176 to COM1.

SPT: When SPT = 1, driving is in two-screen division mode. For details, refer to the section on the Screen-division Driving Function of the HD66763.

SS17-10: Specify the start position of driving for the first screen, in units of raster rows. The common driver is provided to LCDs from the value set here plus one.

SE17-10: Specify the end position of driving for the first screen, in units of raster rows. The common driver is provided to LCDs up to the value set here plus one.

SS27-20: Specify the start position of driving for the second screen, in units of raster rows. The common driver is provided to LCDs from the value set here plus one.

SE27-20: Specify the end position of driving for the second screen, in units of raster rows. The common driver is provided to LCDs up to the value set here plus one.

Common Serial Transfer

Register settings are transferred from the HD66763. The interface is made up of the common chip select (CCS*), transfer clock (CCL), and data input (CDA) lines.

Data transfer starts when the falling edge of the CCS* line indicates that data is to be transferred. Transfer is ended when the rising edge of the CCS* line indicates that the transfer is over. Bits are transferred in 16-bit units, and the data is transferred in order from MSB to LSB.

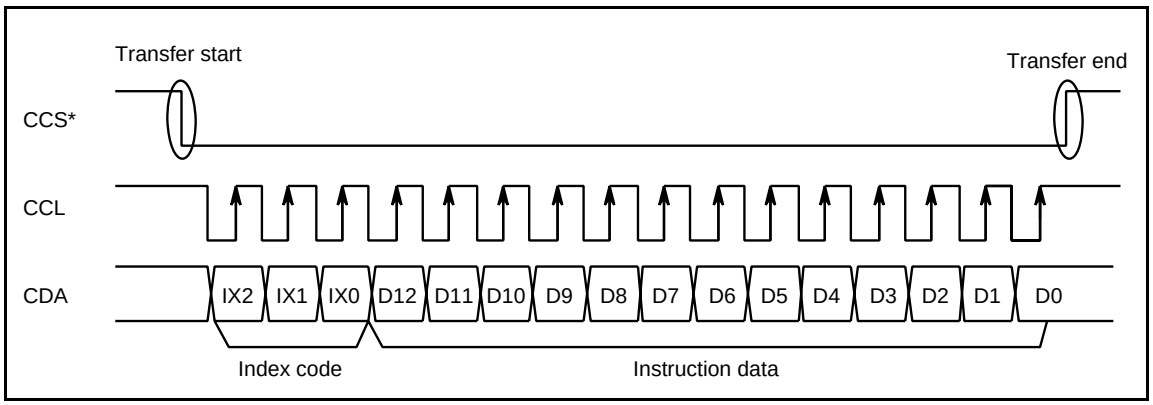


Figure 6 Format for Data Transfer

Interface with LCD Panel

Setting the CMS bit can change the direction of the common signal. The LCD panel and HD66764 can be connected in several ways. When CMS = 0, scanning is in order from COM1 to COM176, and, CMS = 1, it is from COM176 to COM1. When the placement of the screen is adjusted, the display on the LCD grid be made to run from any horizontal or vertical position, in either direction.

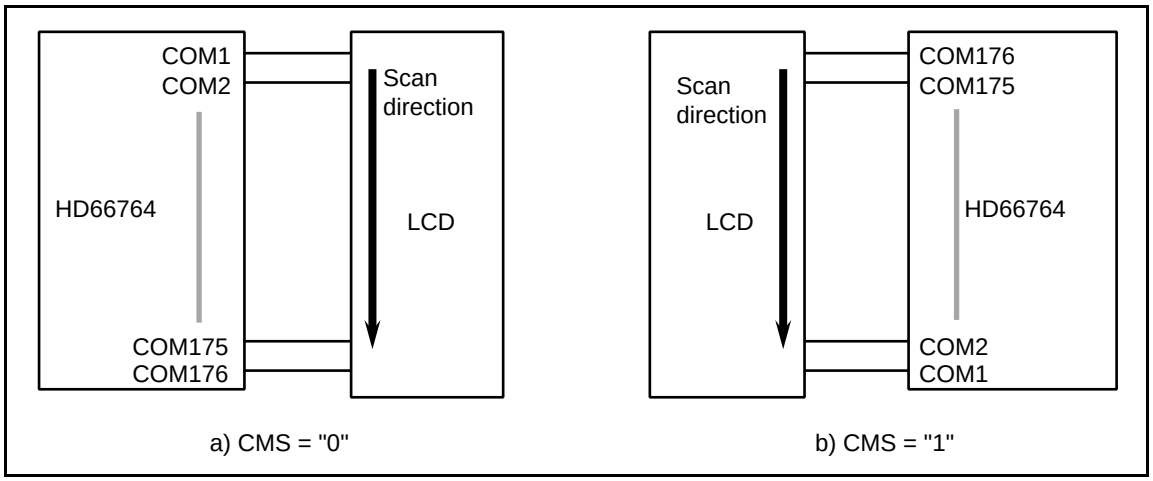


Figure 7 Interface between HD66764 and LCD Panel

Table 9 Common Output to be Used

Display Duty Cycle	CMS = 0	CMS = 1
1/16	COM1 to COM16	COM176 to COM160
1/24	COM1 to COM24	COM176 to COM152
1/32	COM1 to COM32	COM176 to COM144
1/40	COM1 to COM40	COM176 to COM136
1/48	COM1 to COM48	COM176 to COM128
1/56	COM1 to COM56	COM176 to COM120
1/64	COM1 to COM64	COM176 to COM112
1/72	COM1 to COM72	COM176 to COM104
1/80	COM1 to COM80	COM176 to COM96
1/88	COM1 to COM88	COM176 to COM88
1/96	COM1 to COM96	COM176 to COM80
1/104	COM1 to COM104	COM176 to COM72
1/112	COM1 to COM112	COM176 to COM64
1/120	COM1 to COM120	COM176 to COM56
1/128	COM1 to COM128	COM176 to COM48
1/136	COM1 to COM136	COM176 to COM40
1/144	COM1 to COM144	COM176 to COM32
1/152	COM1 to COM152	COM176 to COM24
1/160	COM1 to COM160	COM176 to COM16
1/168	COM1 to COM168	COM176 to COM8
1/176	COM1 to COM176	COM176 to COM1

Note: The above values apply when SS17 to SS10 = H'00.

Example of System Configuration

Figure 8 shows an LCD panel with 128 (horizontal)-by-176 (vertical) dots, configured by using the HD66763 segment driver with built-in display memory. Only two chips are needed to drive the LCD display.

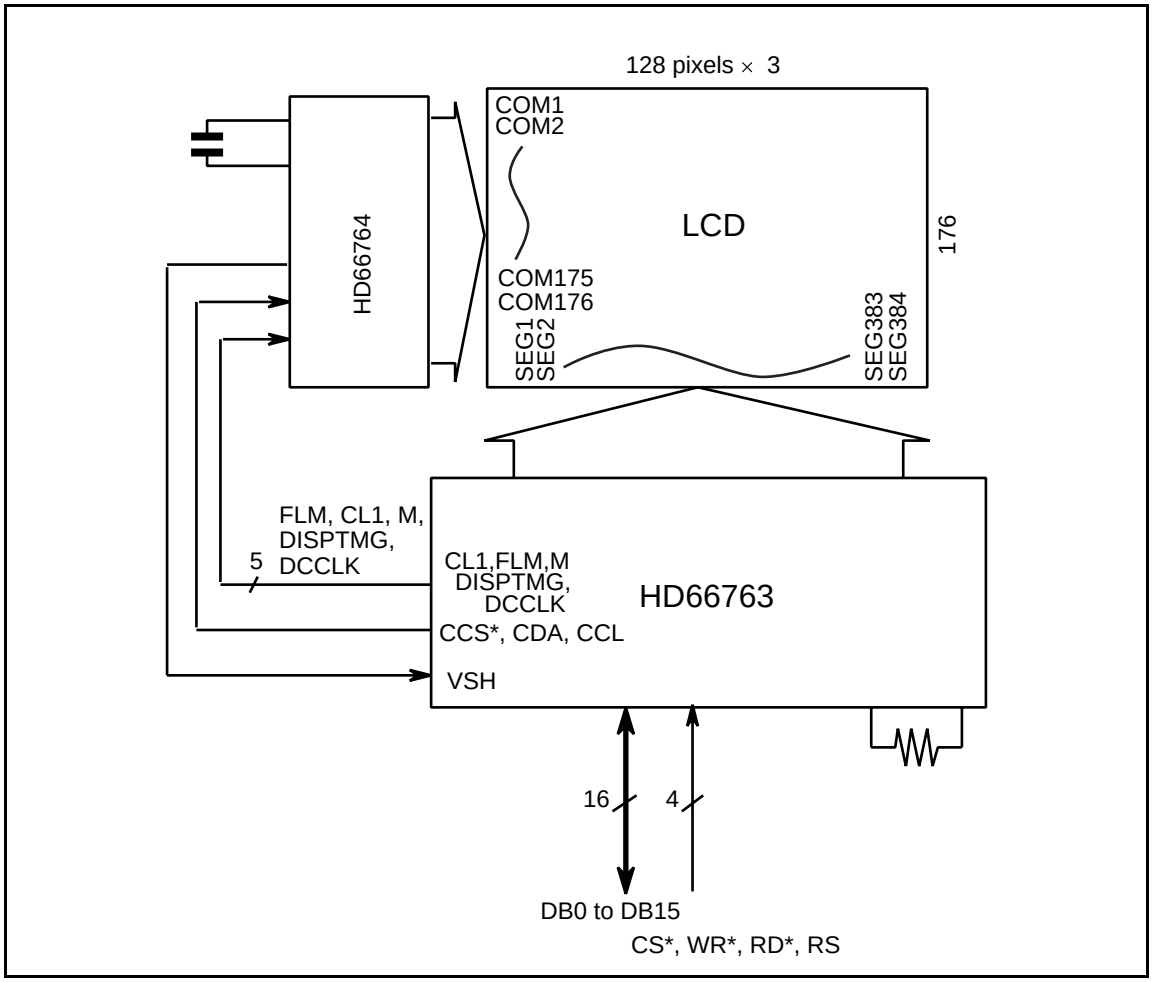


Figure 8 System Configuration

Example of Connection with HD66763

Figure 9 shows an example of connection with the HD66763 segment driver.

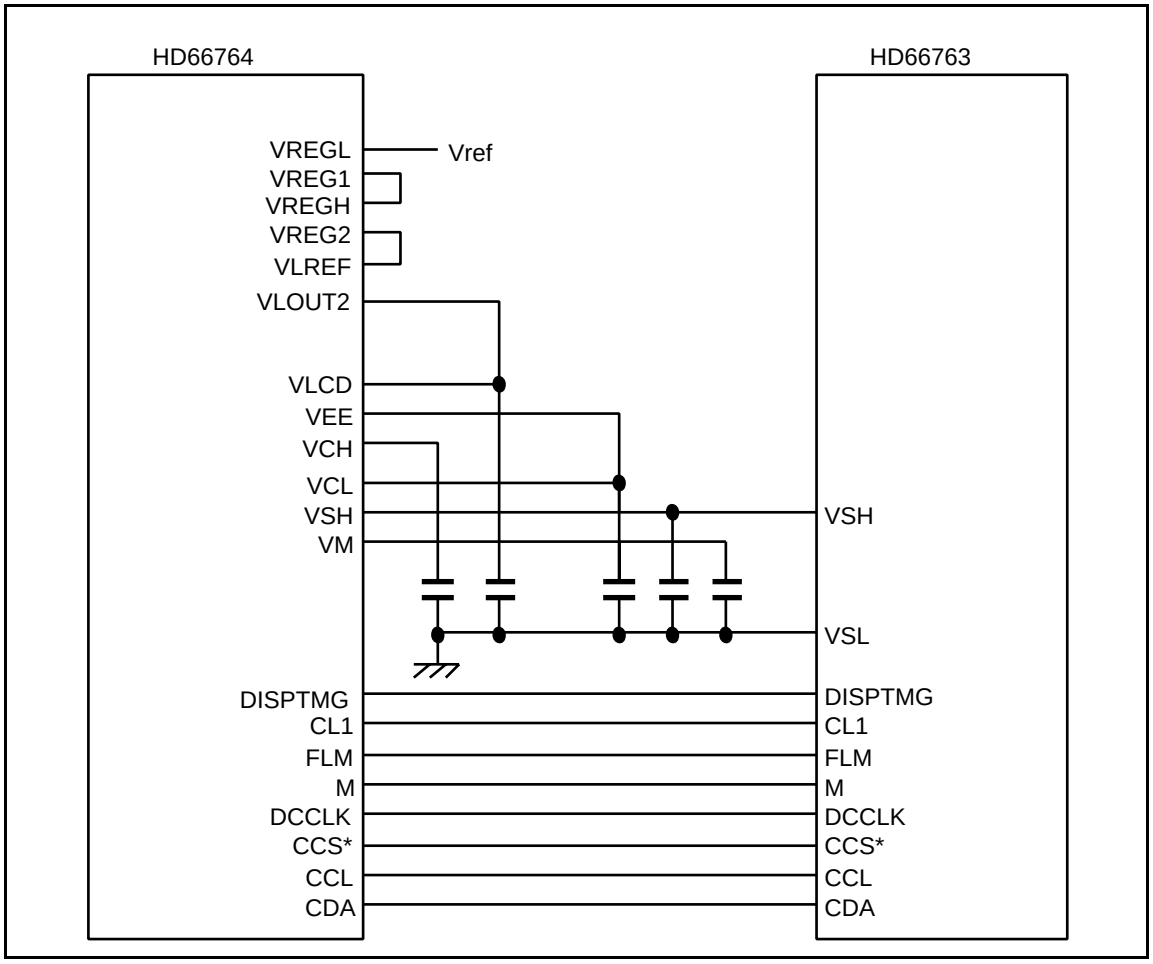
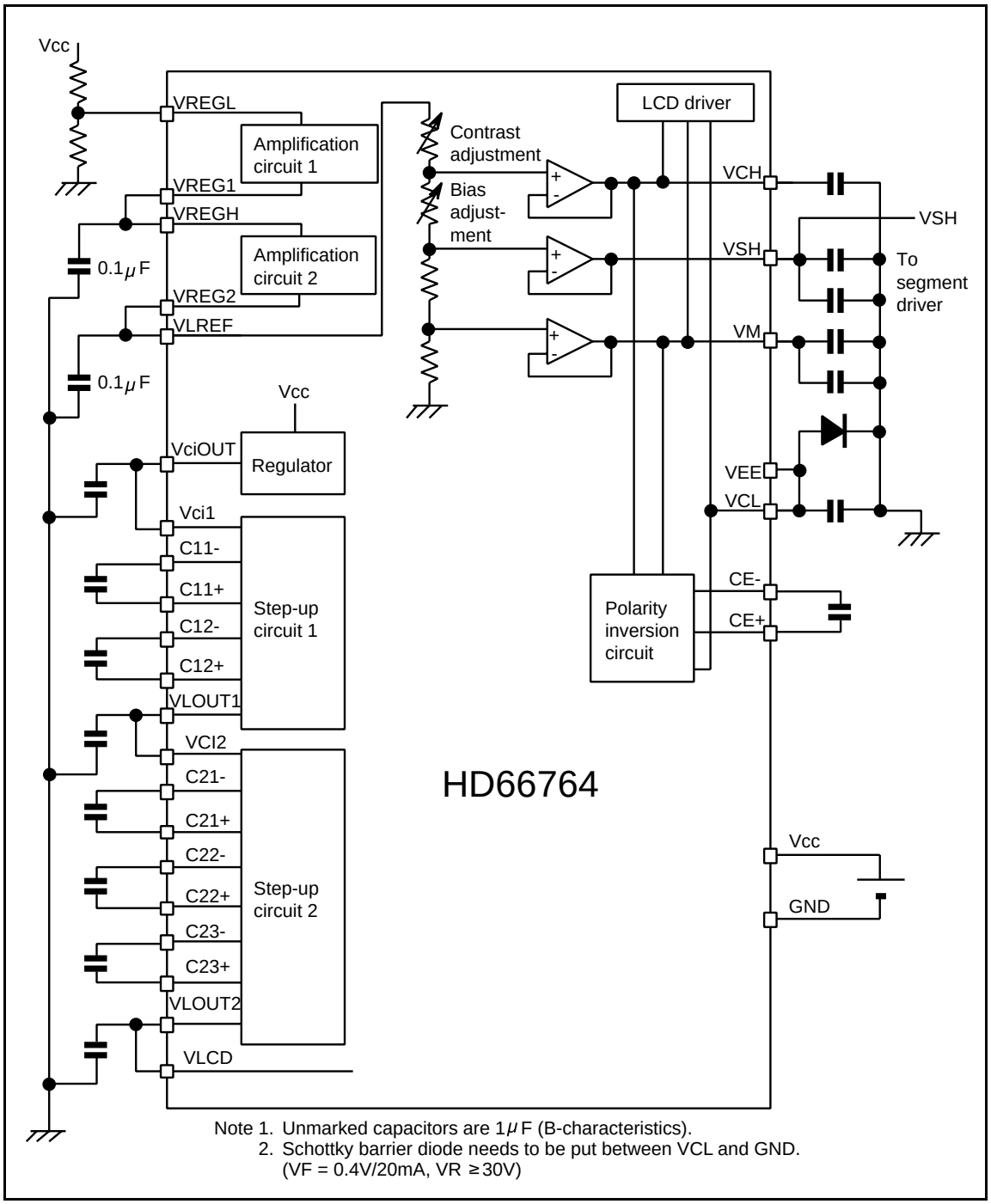


Figure 9 Example of Connection with HD66763

LCD Voltage Generation Circuit

Figure 10 shows a configuration of the HD66764 LCD drive voltage generation circuit. It consists of step-up circuit 1 that doubles or triples the voltage that is applied to Vci, step-up circuit 2 that multiplies the voltage from step-up circuit 1 by one to four times, and step-up circuit 3 that generates a VCL level by inverting the VCH level centered around the VM level. These circuits generate VLCD and VCL that are required to drive the LCDs. When the voltage input to VREGL is amplified in amplification circuit 1 or 2, the level (VCH, VSH, or VM) that drives the LCD is generated by resistance division according to VLREF. Since the input current for VREGL hardly flows, VREGL can be generated by high-resistance division to lower the power consumption. Connect VSH to HD66763.



Note 1. Unmarked capacitors are 1μF (B-characteristics).
2. Schottky barrier diode needs to be put between VCL and GND.
(VF = 0.4V/20mA, VR ≥ 30V)

Figure 10 Configuration of Internal Power Circuit

Notes: 1. Generate an output voltage (VLOUT1) from step-up circuit 1 within the range from 4.5 to 6.0 V.
2. Do not allow the output voltage (VLOUT2) from step-up circuit 2 to exceed 22 V.
3. Generate an output voltage (VREG1) from amplification circuit 1 within the range from 4.5 to 6.0 V.
4. Generate an output voltage (VREG2) from amplification circuit 2 that is lower than VLCD.
5. When a capacitor with polarity is used, be sure that an inverted voltage is not applied to it in any state of the system.
6. Vci1/Vci2 is used as both the reference voltage input and power supply in the step-up circuit. Keep sufficient LCD drive current.
7. The rated voltage of the capacitors are as follows. When actual voltage is less than 16V, 16V rated voltage capacitors can be used.
   6.3V : VREG1, VciOUT, C11, C12, VLOUT1, C21, C22, C23, VSH, VM
   25V(16V) : VREG2, VLOUT2, VCH, CE, VCL

LCD Drive Voltage

The required voltage can be calculated by applying the following expressions. Drive voltages are standard; generate a voltage to suit the panel to be used.

$$VSH - VM,\ VM - VSL = \frac{1}{2}\sqrt{\frac{2\sqrt{N}}{\sqrt{N} - 1}} \times Vth$$

$$VCH - VM,\ VM - VCL = \frac{1}{2}\sqrt{\frac{2N\sqrt{N}}{\sqrt{N} - 1}} \times Vth$$

Vth: Threshold voltage of the LCD panel to be used.
N: Display duty cycle.

LCD Drive Bias

An optimal bias can be calculated by applying the following expression. The value that has been calculated is theoretically optimal. If a lower bias value than the optimal value is used to drive the LCD, contrast may be reduced depending on lighting conditions. However, the power consumption can be reduced by lowering the drive voltage. Adjust the value according to the system to be used.

$$\text{Bias value} = \frac{1}{\sqrt{N}}$$

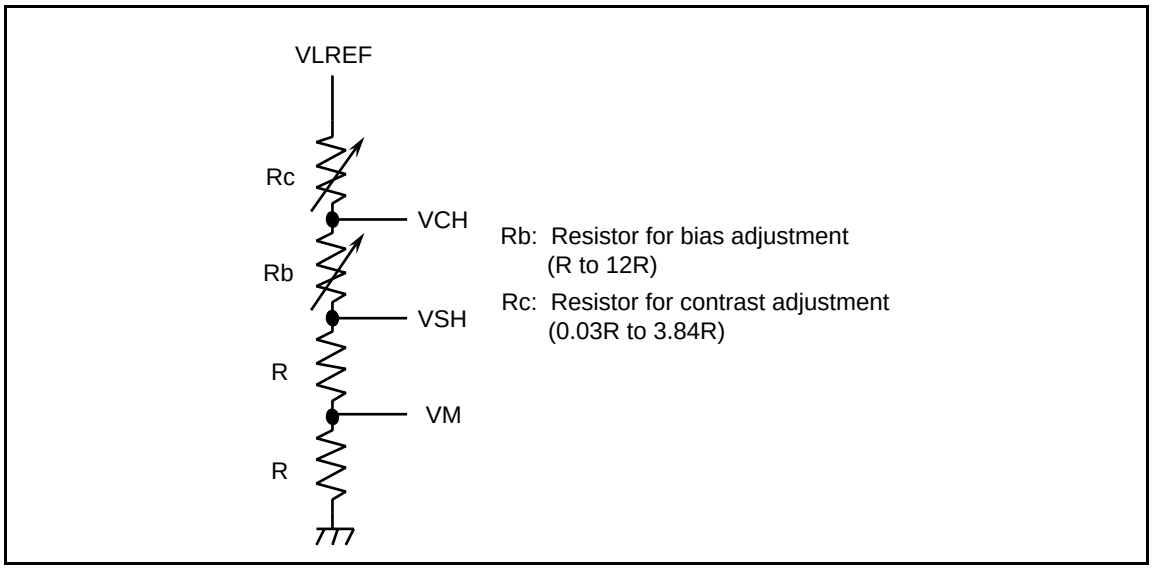


Figure 11 Rb and Rc Resistors

Table 10 BS Bits, LCD Drive Bias Value, and Rb Resistor Value

BS2	BS1	BS0	LCD Drive Bias Value	Rb Resistor Value
0	0	0	1/13 bias	12R
0	0	1	1/12 bias	11R
0	1	0	1/11 bias	10R
0	1	1	1/10 bias	9R
1	0	0	1/9 bias	8R
1	0	1	1/8 bias	7R
1	1	0	1/4 bias	3R
1	1	1	1/2 bias	R

Power-on/off Sequence

To prevent pulse lighting of LCD screens at power-on/off, the power-on/off sequence is activated as shown below. However, since the sequence depends on LCD materials to be used, confirm the conditions by using your own system.

Power-on Sequence

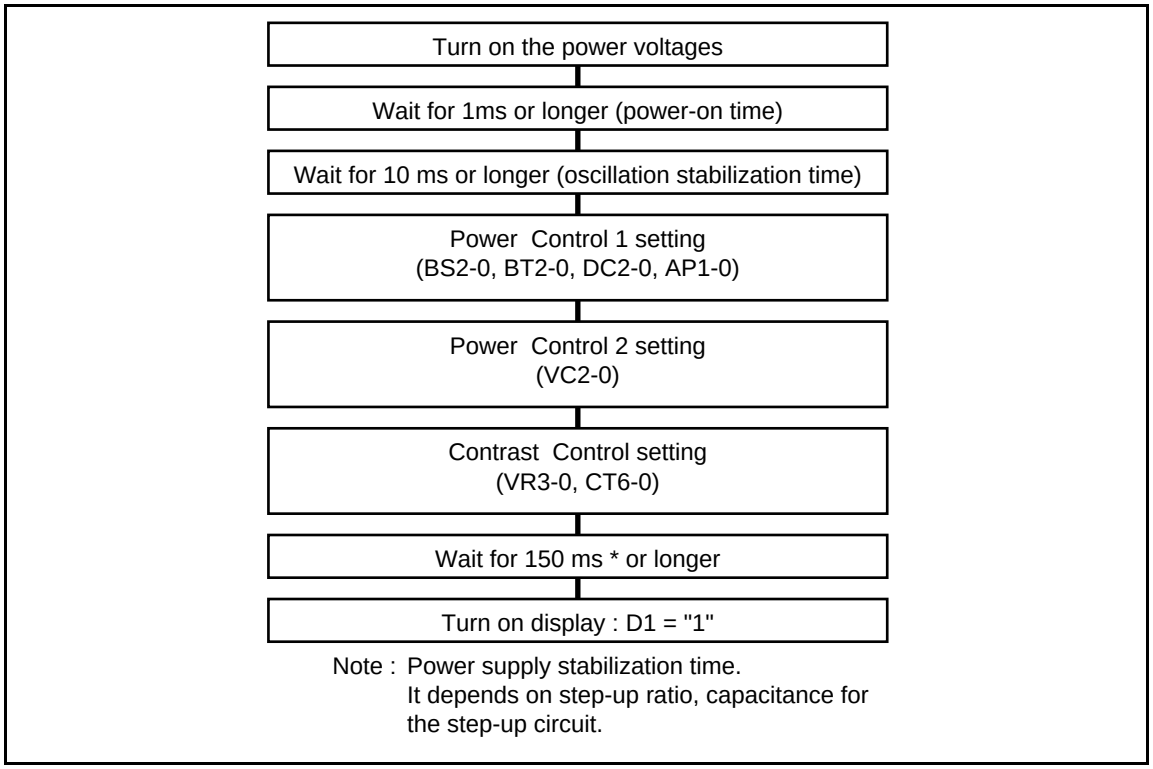


Figure 12 Power-on Sequence

Power-off Sequence

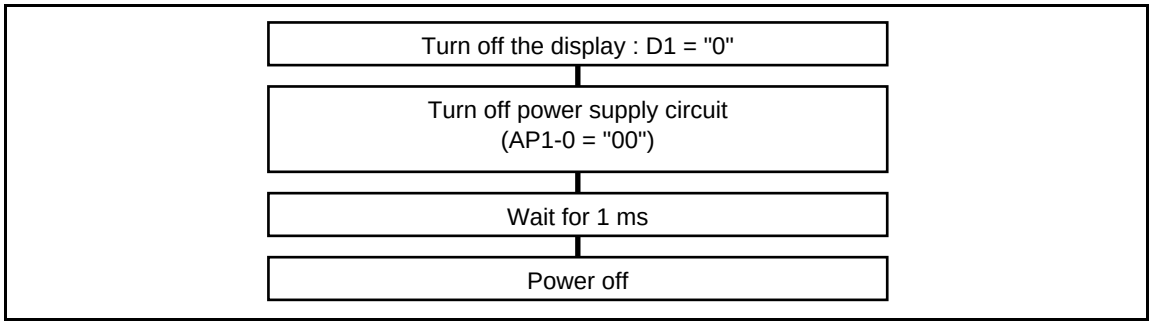
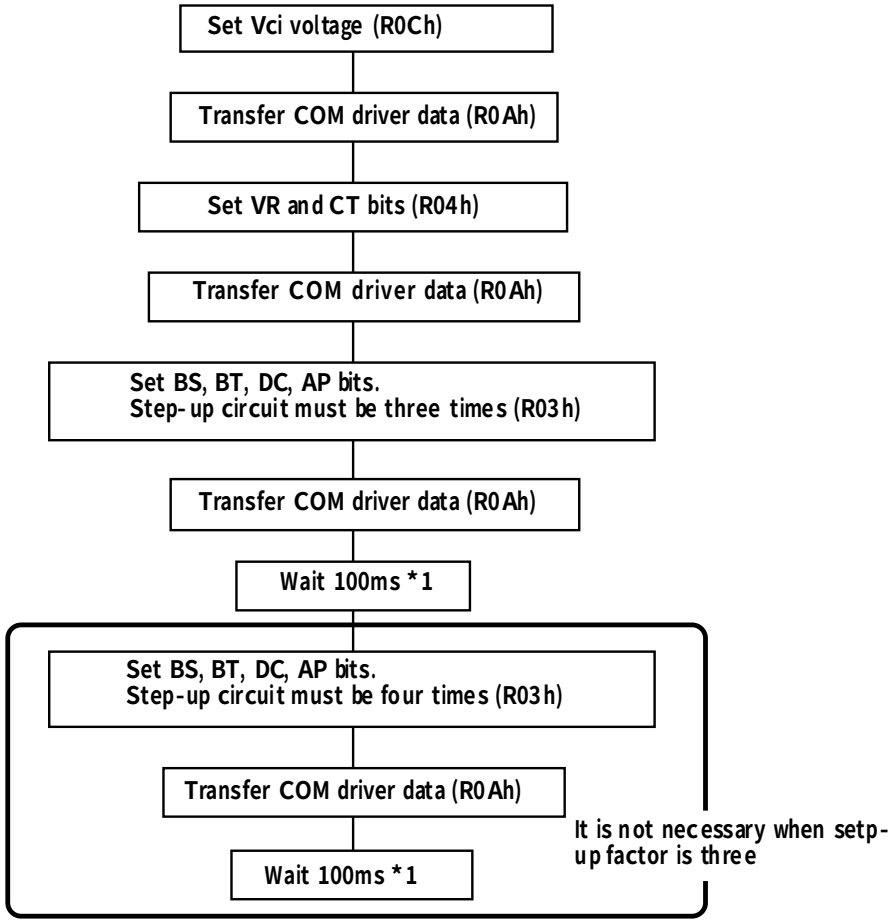


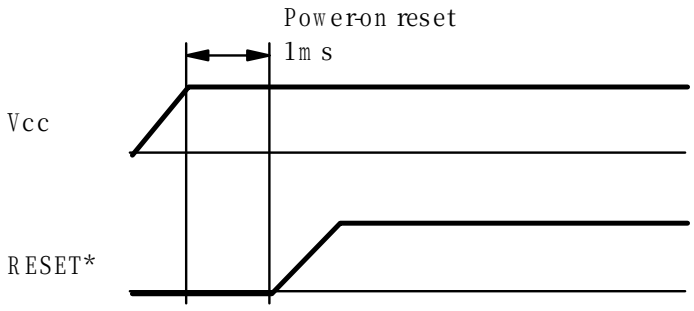
Figure 13 Power-off Sequence

Setting flow for the power circuit of HD66764



Wait until the power circuit becomes stable. It varies according to step-up factor, the value of step-up and stabilized condenser. Evaluate this period on yoursystem.

These register numbers are that of HD66763 or HD66765**.**



Example of register setting on power supply

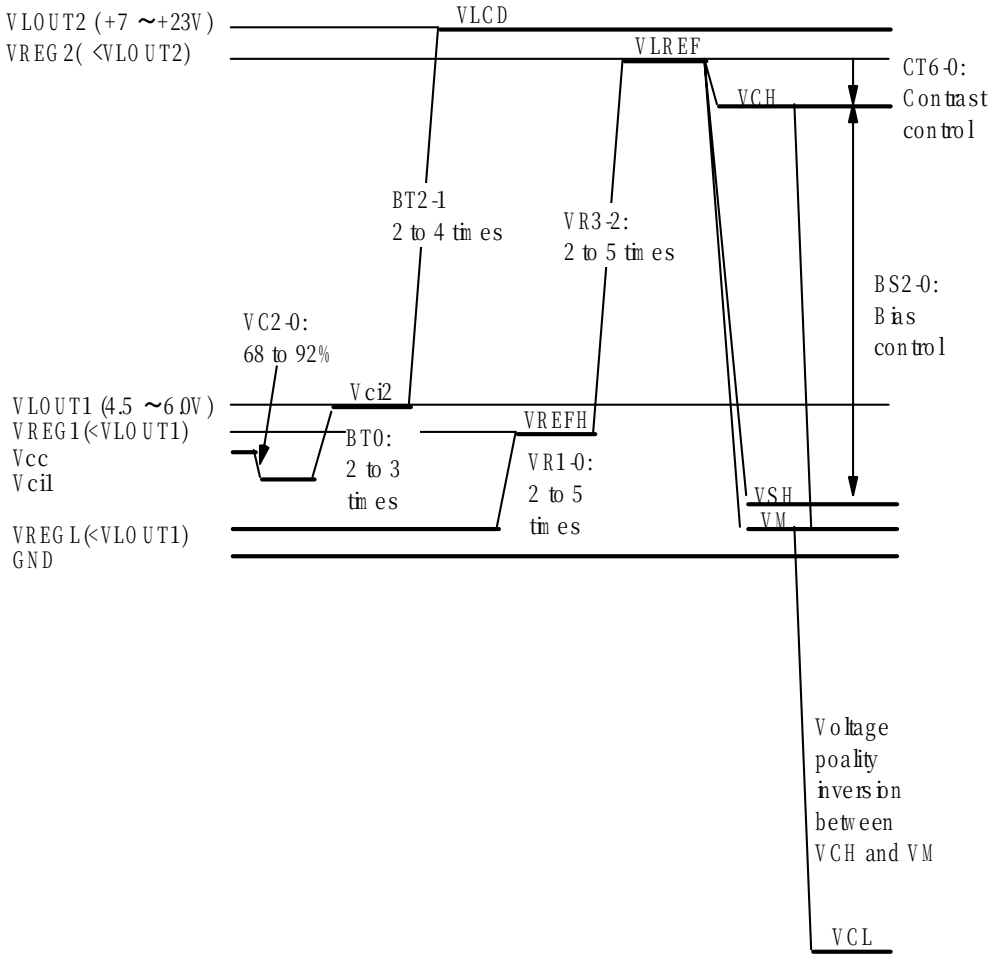
Examples of register setting values on power supply are described below.

Example 1 : 1/160 duty ratio, Vcc = 3.0V, VLCD = 18V
BS2-0 = H'0 : bias adjustment 1/12
BT3-0 = H'4 : step-up circuit 1 2 times, step-up circuit 2 4 times
DC2-0 = H'6 : step-up circuit 1 frequency DCCLK, step-up circuit 2 frequency DCCLK/4
AP1-0 = H'1 : low fixed current in the amplifier
VC2-0 = H'0 : Vci1 = 0.92 x Vcc = 2.75V
VR3-0 = H'A : VREG1 = 3 x VREGL, VREG2 = 5 x VREGH = 15 x VREGL = 18V
VREGL = 1.2V
CT6-0 : appropriate contrast setting values
D1 = H'1 : Dispaly on
CMS = H'0 : Scan direction from COM1 to COM160
SPT = H'0 : No screen-division
SS17 = H'00
SE17 = H'9F : Display area from COM1 to COM160

Example 2 : 1/160 duty ratio, Vcc = 2.4V, Vci = 2.8V, VLCD = 18V
BS2-0 = H'0 : bias adjustment 1/12
BT3-0 = H'4 : step-up circuit 1 2 times, step-up circuit 2 4 times
DC2-0 = H'6 : step-up circuit 1 frequency DCCLK, step-up circuit 2 frequency DCCLK/4
AP1-0 = H'1 : low fixed current in the amplifier
VC2-0 = H'4 : Vci regulator is off. Input external voltage to Vci
VR3-0 = H'A : VREG1 = 3 x VREGL, VREG2 = 5 x VREGH = 15 x VREGL = 18V
VREGL = 1.2V
CT6-0 : appropriate contrast setting values
D1= H'1 : Dispaly on
CMS = H'0 : Scan direction from COM1 to COM160
SPT = H'0 : No screen-division
SS17 = H'00
SE17 = H'9F : Display area from COM1 to COM160

Example 3 : Partial display, 1/24 duty ratio, Vcc = 2.4V, Vci = 2.8V, VLCD = 7V
BS2-0 = H'0 : bias adjustment 1/4
BT3-0 = H'0 : step-up circuit 1 2 times, step-up circuit 2 1.5 times
DC2-0 = H'6 : step-up circuit 1 frequency 2 x DCCLK, step-up circuit 2 frequency DCCLK/4
AP1-0 = H'1 : low fixed current in the amplifier
VC2-0 = H'4 : Vci regulator is off.
VR3-0 = H'2 : VREG1 = 3 x VREGL, VREG2 = 2 x VREGH = 6 x VREGL = 7.2V
VREGL = 1.2V
CT6-0 : appropriate contrast setting values
D1= H'1 : Dispaly on
CMS = H'0 : Scan direction from COM1 to COM24
SPT = H'0 : No screen-division
SS17= H'00
SE17= H'17 : Display area from COM1 to COM24

HD66764 power supply level correlation



Reset Function

The HD66764 is internally initialized by RESET input GND level. Instructions are not issued during the reset period. After power on, the reset must be held.

Instruction Set Initialization:

a. Power control 1 (BS2-0 = 000, BT3-0 = 0000, DC2–0 = 000, AP1–0 = 00, SLP = 0,)
b. Power control 2 (VC2-0 = 000)
c. Contrast adjustment (VR3-0 = 0000, CT6–0 = 0000000)
d. 1st screen division (D1 = 0, CMS = 0, SPT = 0, SE17-10 = 11111111, SS17-10 = 00000000)
e. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)

Output Pin Initialization:

LCD driver output pins (COM): Output GND level

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit	Vcc	-0.3 to +7.0	V	1
	LCD drive circuit	VLCD-VEE	-0.3 to +46	V	
Input voltage		VT1	-0.3 to Vcc + 0.3	V	1, 2
Operating temperature		topr	-40 to +85	°C	
Storage temperature		Tstg	-55 to +110	°C	

Notes: 1. Voltage from GND.
2. Applies to the CL1, FLM, M, CCS*, CDA, CCL, and VREGL pins.

Note: If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

Electrical Characteristics

DC Characteristics (VCC = 1.8 to 3.6 V, VLCD–VEE = 10 to 44 V, GND = 0 V, Ta = -40 to +85 C)[*1]

Item	Symbol	Test Condition	min.	typ.	max.	Unit	Notes
Input high voltage	VIH		0.8× Vcc	-	Vcc	V	2
Input low voltage	VIL		0	-	0.2× Vcc	V	2
Driver ON resistance	RON	VLCD-VEE = 40 V, Iload ± 100 μA	-	1.5	3.0	kΩ	3
VREG OUT voltage range	VREG	VREGH=VREG1	-3.0	0	3.0	%	4
Input leakage current	IIL	Vin=0 to VCC	-2.5	-	2.5	μA	2
Stanby voltage	Istb	Vcc=3.0V	-	0.1	5	μA	5
Consumption voltage	Iop	1/176 duty, frame frequency : 60 Hz, Vcc = 3 V,	-	250	450	μA	6

Notes: 1. For bare die and wafer products, guaranteed at 85°C.

2. Applies to the CL1, FLM, M, DISPTMG, CCS*, CCL, and CDA input pins.

3. Resistor value between the COM and V (VCH, VM, or VCL) pins when a load current flows on one pin of COM1 to COM176. This is specified under the following conditions:
   VCH = +21.5 V, VCL = -18.5 V, VM = (VCH+VCL)/2, Iload = ±100 μA
   The COM1 to COM176 pins other than the pin to be measured should be disconnected.

4. Applies to range of VREG2 OUT expectation value in the following conditions.
   Amplification circuit 1 : 4 times , Amplification circuit 2 : 4 times

5.Specified the following conditions for Vcc,Vci 1 pins.
   (1) CL1 = fixed GND , AP1-0 = (00)
   (2) CL1 = fixed GND , SLP = 0

6.Specified the following conditions for consumption voltage.
   VC2 - 0=(000) (Vci OUT= 0.92×Vcc) , step-up eight times (step-up circuit 1 : 2 times, step-up circuit 2 : 4 times)
   CT6 - 0 =(100 0000), VR3 - 0=(1010), AP1 - 0=(01)
   Vci out=Vci1,VLOUT1=Vci2,VLOUT2=VLCD,VREG2=VLREF,VREG1=VREGH, VREGL=1.1V

AC Characteristics (VCC = 1.8 to 3.6 V, VLCD-VEE = 10 to 44 V)

LCD control signal Timing

Item	Symbol	Pin	min.	typ.	max.	Unit	Notes
CL1 high-level width	tCWH	CL1	4.0	-	-	µs	
CL1 low-level width	tCWL	CL1	4.0	-	-	µs	
CL1 cycle time	tCYC	CL1	10	-	200	µs	
CL1 rise time	tr	CL1	-	-	100	ns	
CL1 fall time	tf	CL1	-	-	100	ns	
FLM setup time	tFS	FLM, CL1	3.0	-	-	µs	
FLM hold time	tFH	FLM, CL1	3.0	-	-	µs	

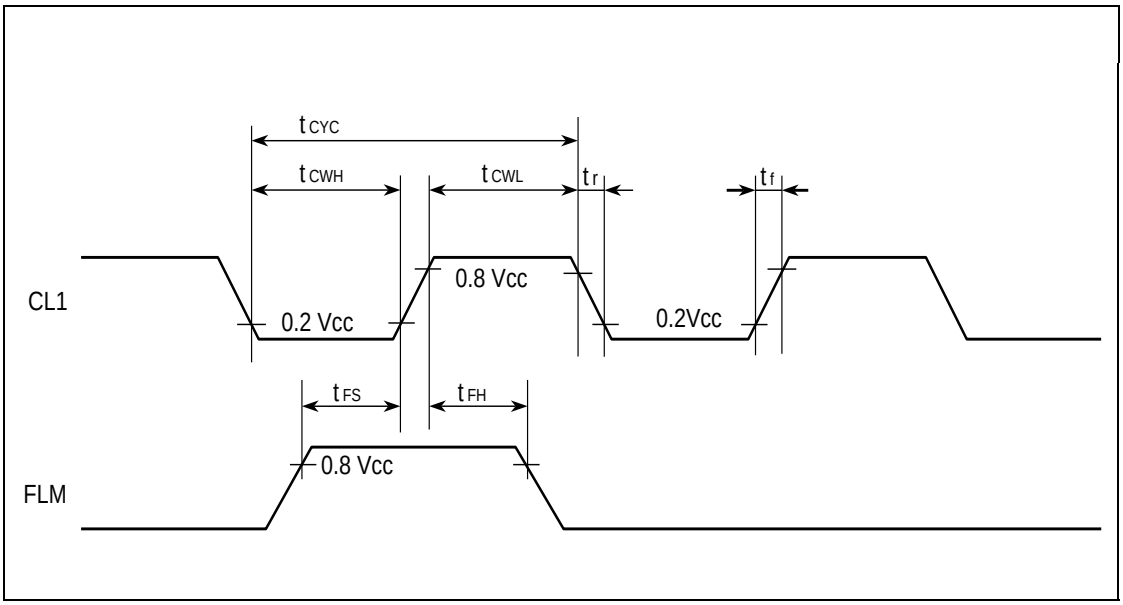


Figure 14 LCD control signal Timing

Common Serial Timing

Item	Symbol	Pin	min.	typ.	max.	Unit	Notes
CCL high-level width	tCLWH	CCL	1.0	-	-	µs	
CCL low-level width	tCLWL	CCL	1.0	-	-	µs	
CCL cycle time	tCYCC	CCL	2.5	-	10	µs	
CCL rise time	tr	CCL	-	-	100	ns	
CCL fall time	tf	CCL	-	-	100	ns	
CDA setup time	tCDS	CDA, CCL	0.5	-	-	µs	
CDA hold time	tCDH	CDA, CCL	0.5	-	-	µs	
CCS* setup time	tCSS	CCS*, CCL	2.0	-	-	µs	
CCS* hold time	tCSH	CCS*, CCL	2.0	-	-	µs	

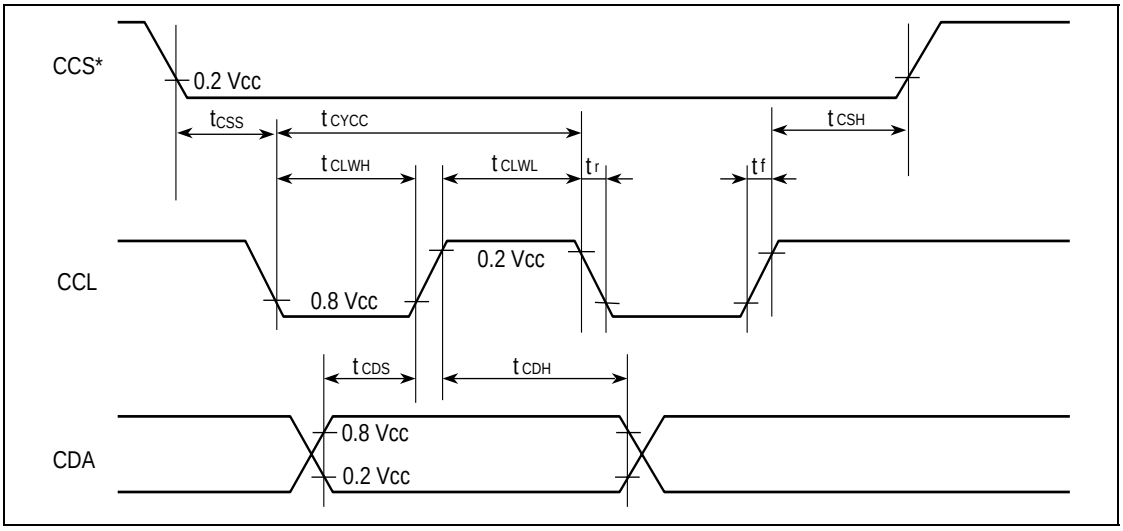
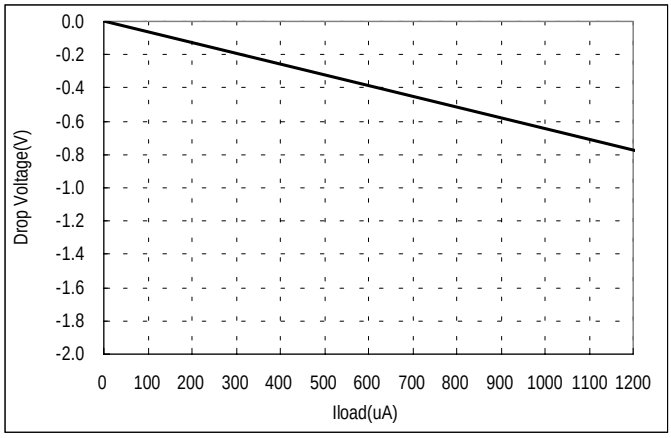


Figure 14 Common Serial Timing

Reference Data

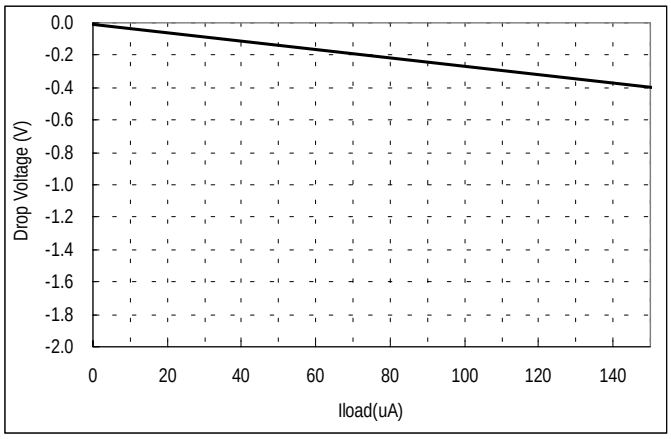
1) Step-up Circuit 1

Measurement condition
Step-up factor :Twice
DCCLK :13.09kHz
Step-up cycle : DCCLK
Temperature :25℃
Vci1 :3.0V



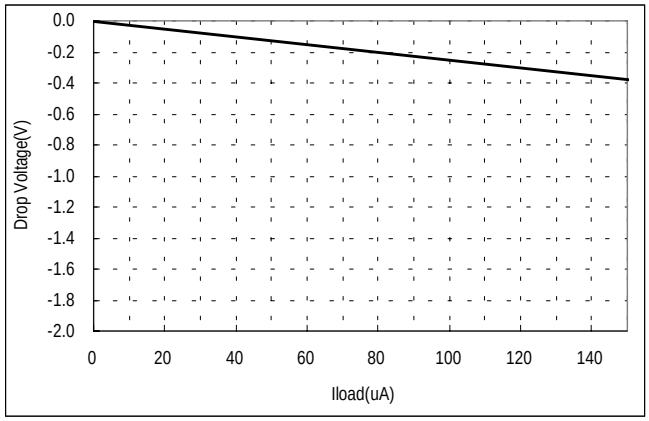
2) Polarity inversion circuit

Measurement condition
DCCLK :13.09kHz
Step-up cycle : DCCLK/ 4
Temperature :25℃
VCH :16V
VM : 0V

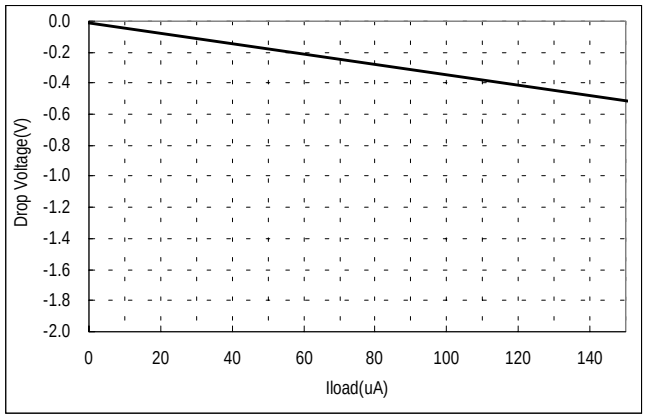


3) **Step-up Circuit 2**

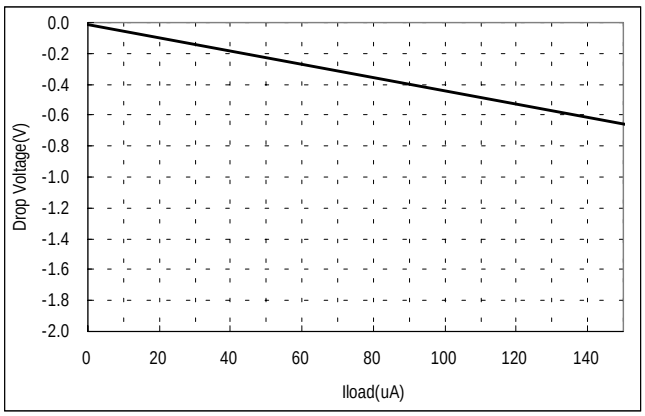
a) Measurement condition
Step-up factor :Twice
DCCLK :13.09kHz
Step-up cycle : DCCLK/4
Temperature :25℃
Vci2 :5.0V



b) Measurement condition
Step-up factor :3 times
DCCLK :13.09kHz
Step-up cycle : DCCLK/4
Temperature :25℃
Vci2 :5.0V

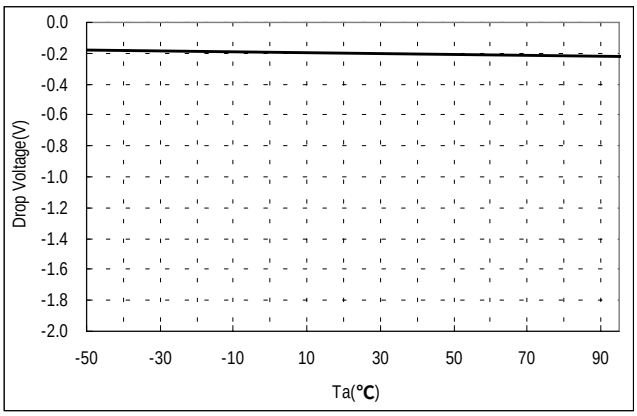


b) Measurement condition
Step-up factor :4 times
DCCLK :13.09kHz
Step-up cycle : DCCLK/4
Temperature :25℃
Vci2 :5.0V



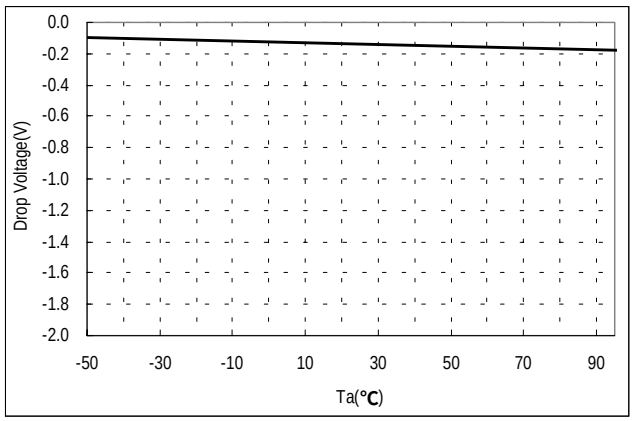
1) Step-up Circuit 1

Measurement condition
Step-up factor : Twice
DCCLK : 13.09kHz
Step-up cycle : DCCLK
Temperature : 25℃
Vci1 : 3.0V
Iload : 300 μA



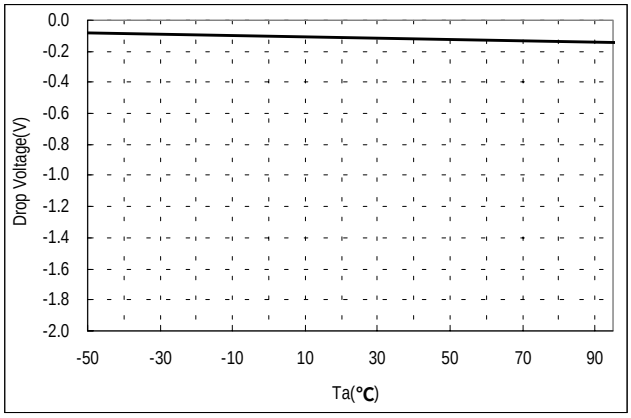
2) Polarity inversion circuit

Measurement condition
DCCLK : 13.09kHz
Step-up cycle : DCCLK/ 4
Temperature : 25℃
VCH : 16V
VM : 0V
Iload : 50 μA

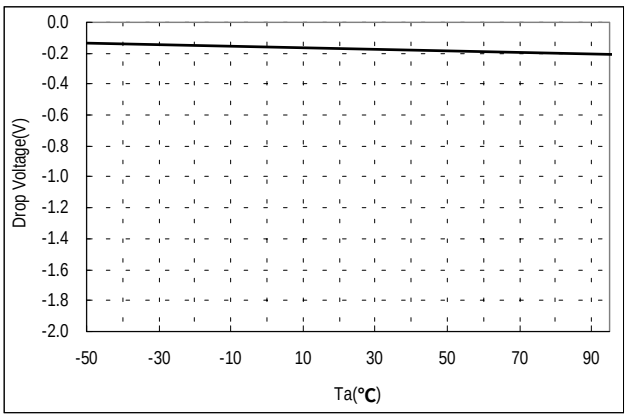


3) Step-up Circuit 2

a)Measurement condition
Step-up factor : Twice
DCCLK : 13.09kHz
Step-up cycle : DCCLK/4
Temperature : 25℃
Vci2 : 5.0V
Iload : 50 μ A



b)Measurement condition
Step-up factor : 3 times
DCCLK : 13.09kHz
Step-up cycle : DCCLK/4
Temperature : 25℃
Vci2 : 5.0V
Iload : 50 μ A



c)Measurement condition
Step-up factor : 4 times
DCCLK : 13.09kHz
Step-up cycle : DCCLK/4
Temperature : 25℃
Vci2 : 5.0V
Iload : 50 μ A