NIPPON PRECISION CIRCUITS LTD.

CMOS LSI SM5840JP/JS

Audio Multi-function Digital Filter

OVERVIEW

The SM5840JP/JS is an 8-times oversampling digital filter for digital audio, fabricated using NPC's Moly-Gate® CMOS process. It supports 18.9 and 37.8 kHz input sample rates for CDI replay, and 44.1 kHz input sample rate for CD-DA replay. The device clock can be constant at 16.9344 or 8.4672 MHz, independent of the sample rate. The SM5840JP/JS requires an external ADPCM-to-linear PCM decoder for ADPCM data replay in CDI systems.

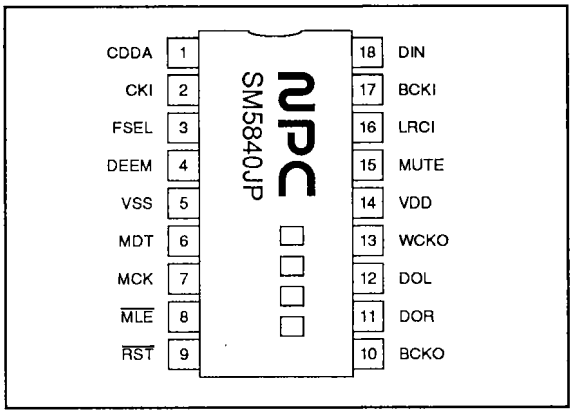
The SM5840JP/JS features selectable digital deemphasis, attenuation, mute and noise shaping functions. The serial data format consists of 16- or 18-bit input words and 16-, 18- or 20-bit output words in 2s complement form, supporting interface to a wide range of D/A converters. An independent serial control interface is provided to set mode control flags and signal attenuation.

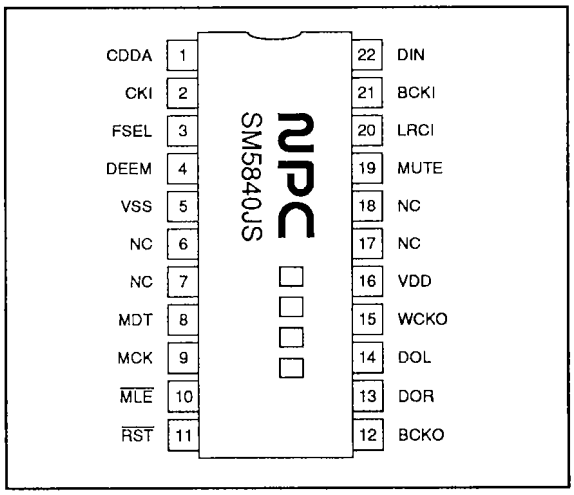
The SM5840JP/JS operates from a 5 V supply and is available in 18-pin plastic DIPs and 22-pin SOPs.

FEATURES

- Stereo 8-times oversampling digital filter
- Three-stage interpolation filters, consisting of 69-tap, 13-tap, and 9-tap FIR filters
- IIR deemphasis filter for accurate gain and phase response
- 19 × 14-bit multiplier
- 24-bit accumulator for increased resolution
- Digital attenuator and overflow limiter
- Within ± 0.03 dB passband ripple
- Greater than 55 dB stopband attenuation
- Linear phase (no group delay)
- 16- or 18-bit serial input data
- 16-, 18-, or 20-bit serial output data
- Stereo or bilingual mode output
- Switchable DC output offset
- TTL-compatible inputs and outputs
- Moly-Gate ® CMOS process
- Single 5 V supply
- 18-pin plastic DIPs and 22-pin SOPs

PINOUTS

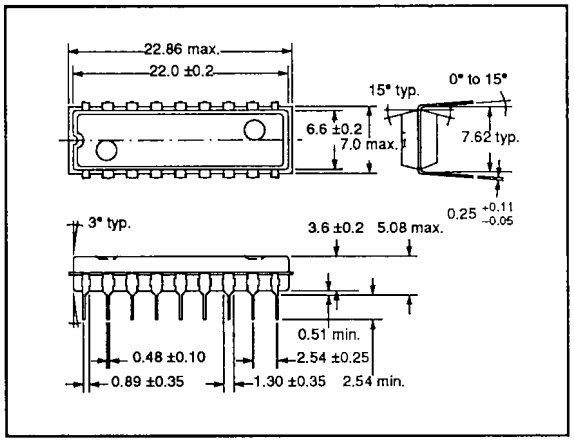




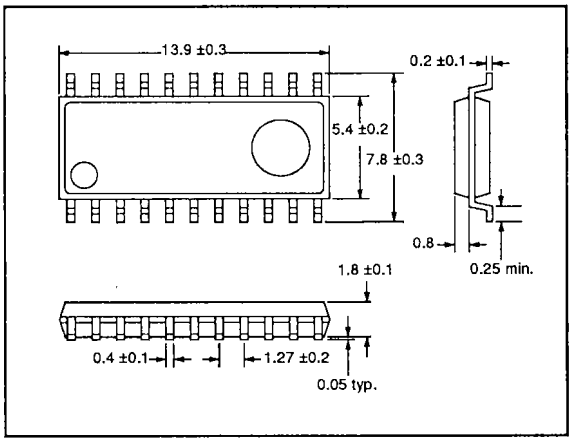
PACKAGE DIMENSIONS

Unit: mm

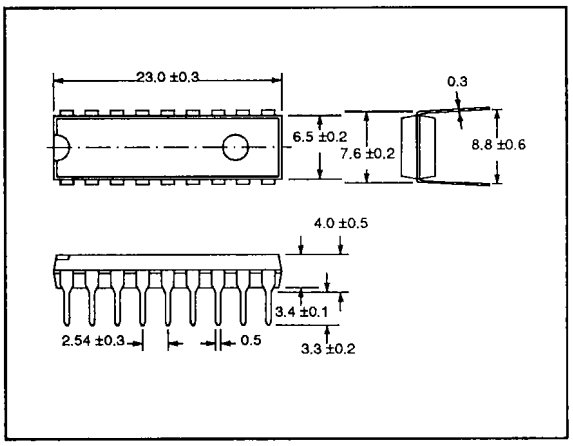
DIP18 Type A



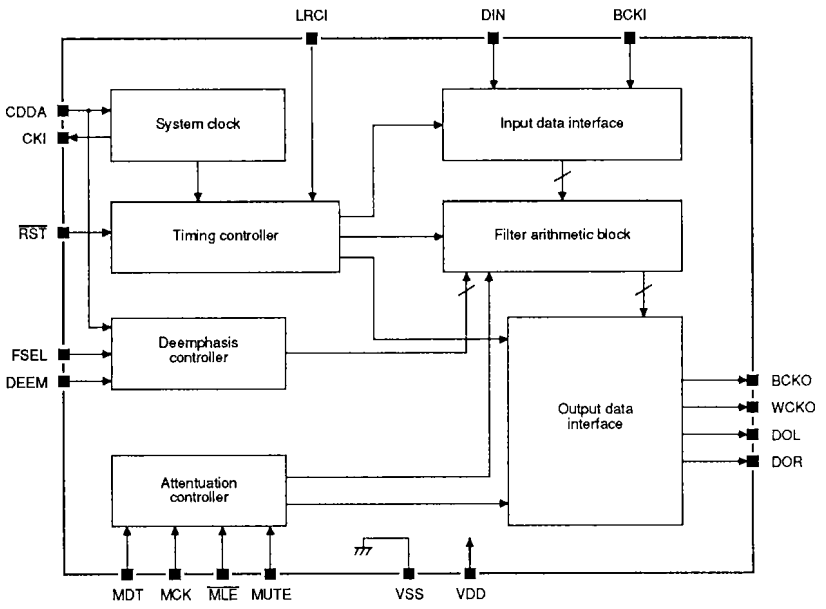
SOP22



DIP18 Type B



BLOCK DIAGRAM



PIN DESCRIPTION

Number		Name	Description
DIP	SOP		
1	1	CDDA	CD-DA or ADPCM selection. When HIGH, CD-DA is set at 44.1 kHz. When LOW, ADPCM is set at 37.8 or 18.9 kHz.
2	2	CKI	16.9344 or 8.4672 MHz system clock input
3	3	FSEL	ADPCM sample frequency select, when CD-DA is LOW. FSEL is HIGH for 37.8 kHz and LOW for 18.9 kHz.
4	4	DEEM	Deemphasis enable
5	5	VSS	Ground
–	6	NC	No connection
–	7	NC	No connection
6	8	MDT	Mode set data
7	9	MCK	Mode set clock
8	10	$\overline{\text{MLE}}$	Mode set latch enable
9	11	$\overline{\text{RST}}$	Device reset
10	12	BCKO	Output bit clock
11	13	DOR	Right-channel data output
12	14	DOL	Left-channel data output
13	15	WCKO	Output word clock
14	16	VDD	5 V supply
–	17	NC	No connection
–	18	NC	No connection
15	19	MUTE	Soft mute enable
16	20	LRCI	Input word clock
17	21	BCKI	Input bit clock
18	22	DIN	Input data

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_I	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	250	mW
Operating temperature range	T_{opr}	–20 to 80	deg. C
Storage temperature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{SLD}	255	deg. C
Soldering time	t_{SLD}	10	S

Recommended Operating Conditions

V_{SS} = 0 V, T_a = 25 deg. C

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5.0	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

DC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −20 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current	I_{DD}	V_{DD} = 5.0 V, f_{CI} = 20.0 MHz, CDDA is LOW. FSEL is HIGH.	–	–	40	mA
FSEL, DEEM, CKI and MUTE LOW-level input voltage	V_{IL1}		–	–	0.3V_{DD}	V
FSEL, DEEM, CKI and MUTE HIGH-level input voltage	V_{IH1}		0.7V_{DD}	–	–	V
BCKI, CDDA, DIN, LRCI, MCK, MDT, $\overline{MLE}$ AND $\overline{RST}$ LOW-level input voltage	V_{IL2}		–	–	0.5	V
BCKI, CDDA, DIN, LRCI, MCK, MDT, $\overline{MLE}$ AND $\overline{RST}$ HIGH-level input voltage	V_{IH2}		2.4	–	–	V
Clock input voltage	V_{INAC}	AC-coupled, sine-wave input	0.3V_{DD}	–	–	V_{P-P}
DOL, DOR, BCKO and WCKO LOW-level output voltage	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
DOL, DOR, BCKO and WCKO HIGH-level output voltage	V_{OH}	I_{OH} = −0.4 mA	2.5	–	–	V
CKI LOW-level input leakage current	I_{LL1}	V_I = 0 V	–	10	20	µA
CKI HIGH-level input leakage current	I_{LH1}	V_I = V_{DD}	–	10	20	µA
FSEL, DEEM and MUTE LOW-level input leakage current	I_{LL2}	V_I = 0 V	–	–	1.0	µA
FSEL, DEEM, MUTE, LRCI, DIN, BCKI, CDDA, MDT, MCK, $\overline{MLE}$ and $\overline{RST}$ HIGH-level input leakage current	I_{LH2}	V_I = V_{DD}	–	–	1.0	µA
LRCI, DIN, BCKI, CDDA, MDT, MCK, $\overline{MLE}$ and $\overline{RST}$ input current	I_{IL}	V_I = 0 V	–	10	20	µA

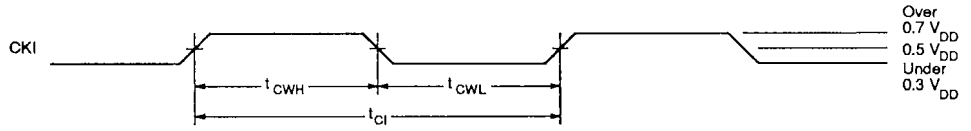
AC Electrical Characteristics

External Clock

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −20 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
LOW-level clock pulsewidth	t_{CWL}	CKSL is LOW.	23	–	250	ns
		CKSL is HIGH.	45	–	250	
HIGH-level clock pulsewidth	t_{CWH}	CKSL is LOW.	23	–	250	ns
		CKSL is HIGH.	45	–	250	
Clock pulse period	t_{CI}	CKSL is LOW.	50	–	500	ns
		CKSL is HIGH.	100	–	500	

External clock timing waveform

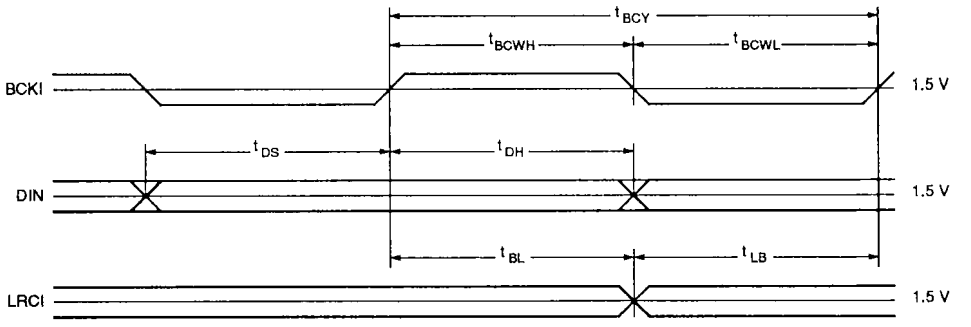


BCKI, DIN, LRCI Input Timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = −20 to 80 deg. C

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI pulse period	t_{BCY}	100	–	–	ns
DIN setup time	t_{DS}	50	–	–	ns
DIN hold time	t_{DH}	50	–	–	ns
Last BCKI falling edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns

BCKI, DIN, LRCI input timing waveform



MDT, MCK, $\overline{\text{MLE}}$ Input Timing

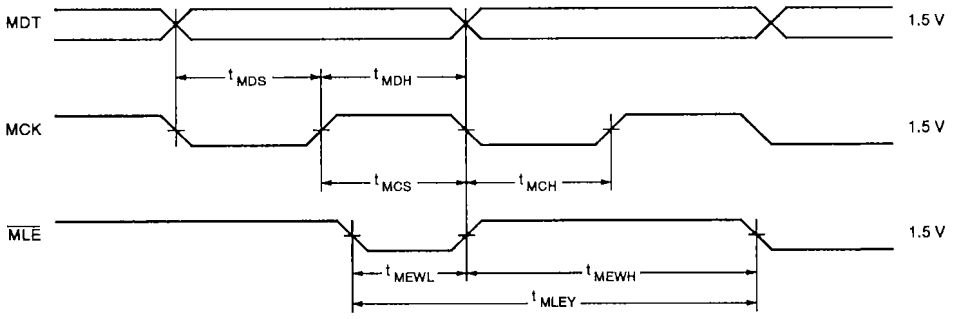
V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C

Parameter	Symbol	Rating			Unit
		min	typ	max	
MDT setup time	t_{MDS}	20	–	–	ns
MDT hold time	t_{MDH}	20	–	–	ns
$\overline{\text{MLE}}$ setup time	t_{MCS}	40	–	–	ns
$\overline{\text{MLE}}$ hold time	t_{MCH}	20	–	–	ns
$\overline{\text{MLE}}$ LOW-level period	t_{MEWL}	20	–	–	ns
$\overline{\text{MLE}}$ HIGH-level period	t_{MEWH}	20	–	–	ns
$\overline{\text{MLE}}$ pulse-to-pulse separation time. See note.	t_{MLEY}	$6T_{SYS}$	–	–	–

Note

T_{SYS} is the system clock period. For TCDDA (CDDA OR FCDDA) = HIGH, T_{SYS} = 1/384fs. For TCDDA (CDDA OR FCDDA) = LOW, T_{SYS} = 1/448fs.

MDT, MCK, $\overline{\text{MLE}}$ input timing waveform



DEEM, MUTE Control Input Timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C

Parameter	Symbol	Rating			Unit
		min	typ	max	
DEEM and MUTE rise time	t_r	–	–	100	ns
DEEM and MUTE fall time	t_f	–	–	100	ns

Note

Rise times and fall times are measured between 10% and 90% of V_{DD}.

Output Timing

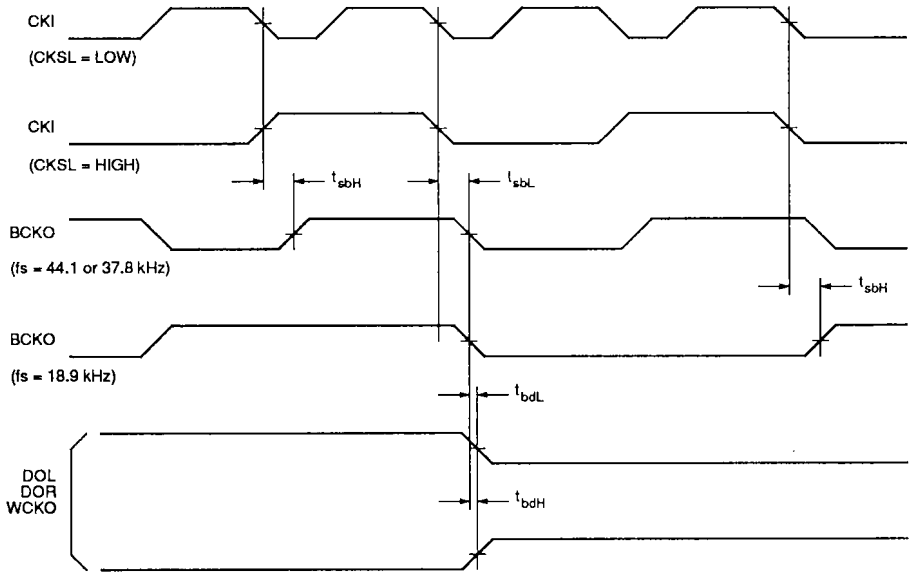
V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 80 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CKI falling edge to BCKO falling edge	t_{sbL}	fs = 44.1 or 37.8 kHz	10	–	60	ns
		fs = 18.9 kHz	15	–	70	
CKI falling edge to BCKO rising edge	t_{sbH}	fs = 44.1 or 37.8 kHz	10	–	60	ns
		fs = 18.9 kHz	15	–	70	
BCKO falling edge to DOL, DOR or WCKO falling edge	t_{bdL}		0	–	20	ns
BCKO falling edge to DOL, DOR or WCKO rising edge	t_{bdH}		0	–	20	ns
$\overline{RST}$ rising edge to DOL or DOR rising edge	t_{rdL}		–	–	40	ns
$\overline{RST}$ falling edge to DOL or DOR falling edge	t_{rdH}		–	–	40	ns

Note

All measurements with 15 pF capacitive load

Output timing waveform

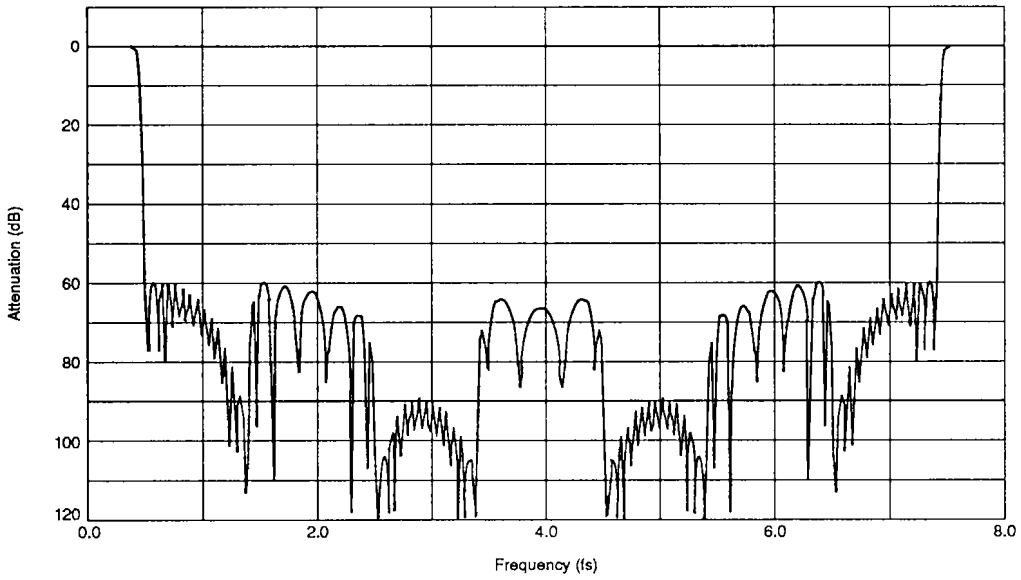


Filter Characteristics

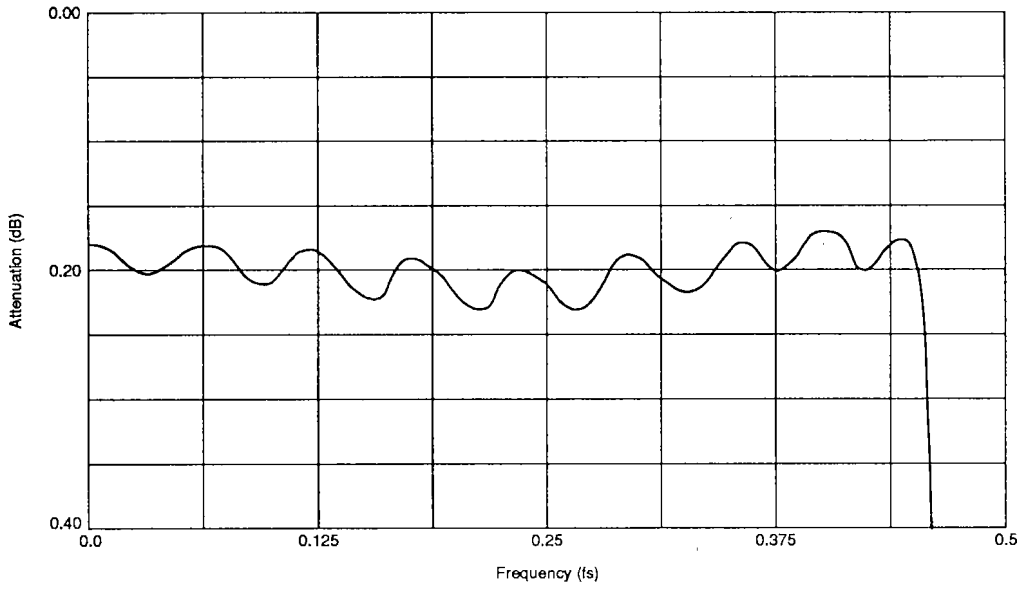
8-times oversampling mode

Parameter	Rating
Passband	0 to 0.4535fs
Stopband	0.5465fs to 7.4535fs
Passband attenuation level	0.20 ±0.03 dB
Stopband attenuation	> 55 dB
Group delay time	Constant

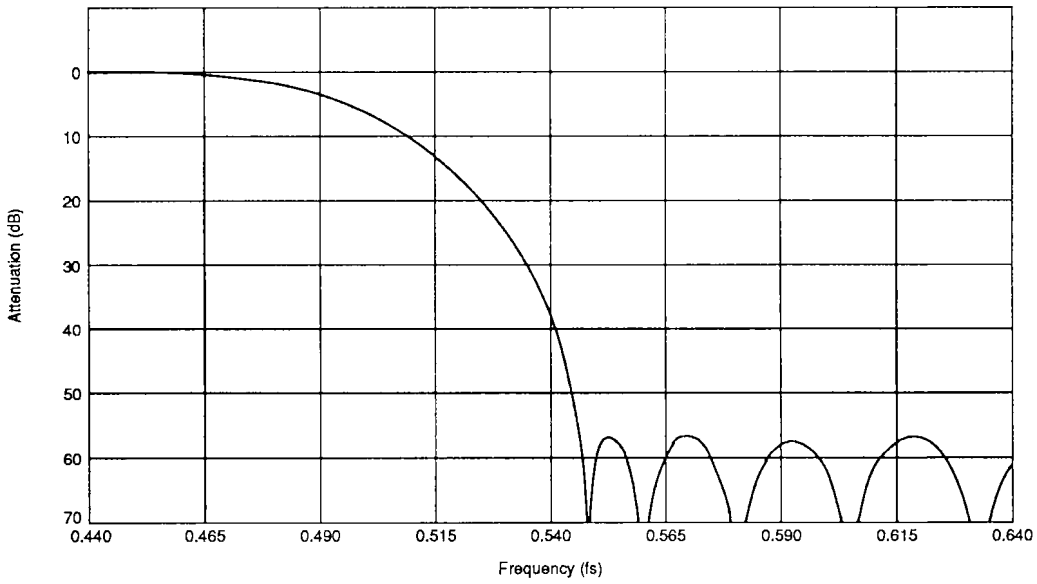
Frequency characteristic without deemphasis



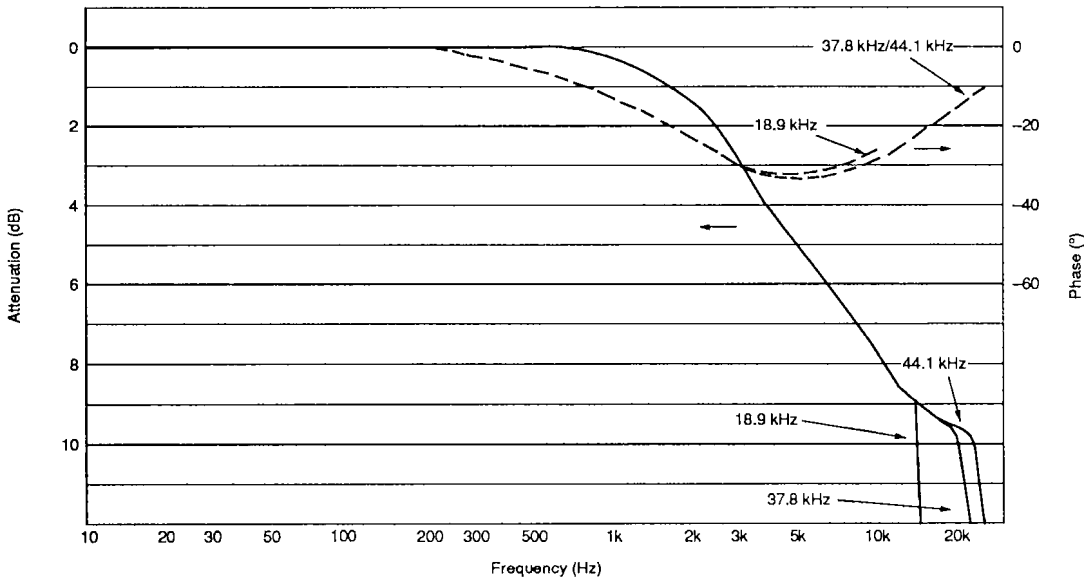
Passband characteristic without deemphasis



Transition characteristic without deemphasis

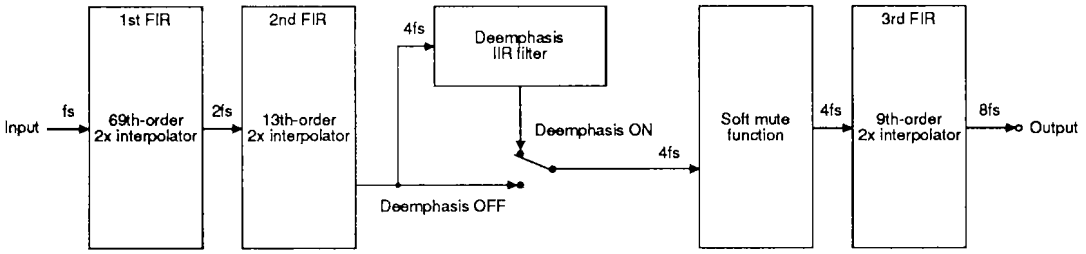


Passband characteristic with deemphasis



FUNCTIONAL DESCRIPTION

SM5840JP/JS Arithmetic Block



The SM5840JP/JS performs oversampling using a multi-stage FIR interpolation filter. Each filter stage interpolates the signal by a factor of two. The overall interpolation factor of the device, therefore, is equal to eight. Sampling noise components are attenuated by the interpolation filter to greater than 55 dB in the 0.5465fs to 7.4535fs stopband.

Mode Flags

The operation of the SM5840JP/JS can be configured by a number of control pins and mode flags. The mode flags are set using the microcontroller serial interface (pins MDT, MCK and $\overline{\text{MLE}}$). Table 1 lists the various configurable functions and the relevant control pins and mode flags. For those functions that can be controlled in several ways, the effective setting of the control flags is the logical OR of the control pin and mode flag values as listed below.

- TCDDA = CDDA OR FCDDA
- TFSEL = FSEL OR FFSEL
- TDEEM = DEEM OR FDEEM
- TMUTE = MUTE OR FMUTE

If using the microcontroller interface to configure the SM5840JP/JS, set the CDDA, FSEL, DEEM and MUTE pins LOW. If not using the microcontroller interface, the FCDDA, FFSEL, FDEEM and FMUTE flags can be left at their initialized setting (LOW). The control pins then control the relevant functions.

Table 1. SM5840JP/JS function configurations

Function	Control pin (default setting)	Interface flag
CD-DA or ADPCM select	CDDA	FCDDA
Deemphasis enable	DEEM	FDEEM
Sample rate select (fs)	CDDA, FSEL	FCDDA, FFSEL
Mute enable	MUTE	FMUTE
Attenuation	(No attenuation)	7 bits, a1 to a7
Bilingual select	(LR stereo)	BILL, BIRR
System clock select	(16.9344 MHz)	CKSL
LRCI polarity	(Left/right channel = HIGH/LOW)	LRPL
Input word length	(16 bits)	IW18
Output word length	(18 bits)	OW16, OW20
Output DC offset	(Off)	OFST

Microcontroller Interface

A microcontroller can configure the SM5840JP/JS through the MDT (data), MCK (clock) and $\overline{\text{MLE}}$ (latch enable) pins. Data on MDT is shifted into an internal, 8-bit shift register on the rising edge of MCK. Therefore, MDT should change state on the falling edge of MCK. The data in the shift register is latched into the control flag register on the rising edge of $\overline{\text{MLE}}$. The first one or two bits of the eight input bits select the register into which the data is latched. If the first bit is binary 0, the following seven bits are latched into the attenuator coefficient register, as shown in figure 1. Otherwise, the second bit selects one of the two groups of mode flags as shown in figures 2 and 3.

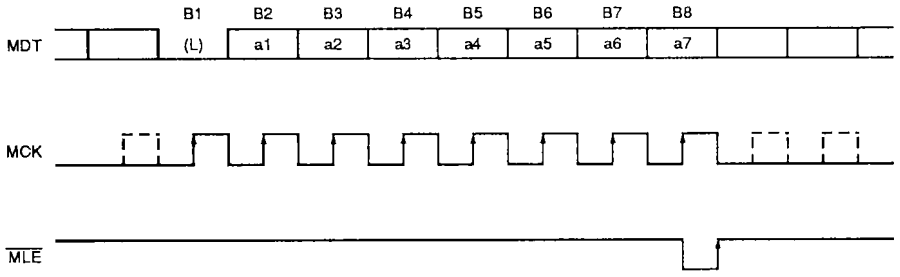


Figure 1. Attenuator flag settings

Note
Dotted lines indicate optional clock pulses.

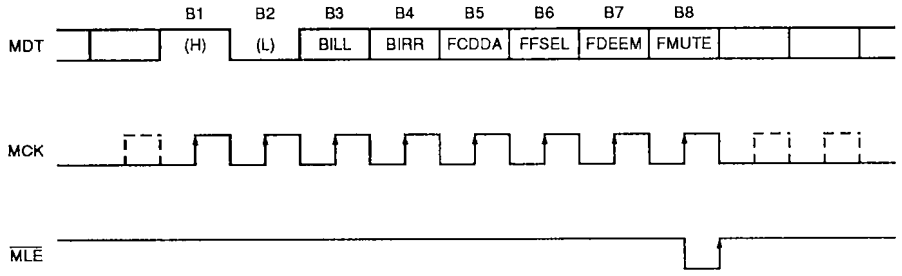


Figure 2. Mode flag settings, group 1

Note
Dotted lines indicate optional clock pulses.

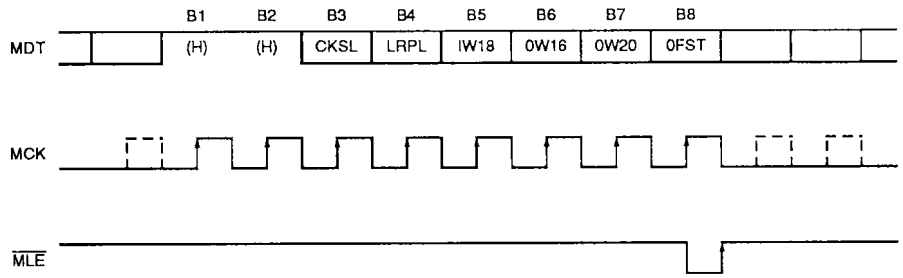


Figure 3. Mode flag settings, group 2

Note
Dotted lines indicate optional clock pulses.

Table 2 gives group 1 mode flag information. Additional logic truth tables related to these mode flags are shown in tables 3 and 6.

Table 2. Mode flags, group 1

Bit	Flag	Function	Selection	Default
3	BILL	Bilingual output select	See table 3.	BILL = LOW, BIRR = LOW, Stereo
4	BIRR			
5	FCDDA	CDDA or ADPCM select	When TCDDA is LOW, ADPCM is 37.8 or 18.9 kHz. When TCDDA is HIGH, CDDA is 44.1 kHz.	FCDDA = LOW
6	FFSEL	Sample rate select	See table 7.	FFSEL = LOW
7	FDEEM	Deemphasis enable	Deemphasis is OFF when TDEEM is LOW. Deemphasis is ON when TDEEM is HIGH.	FDEEM = LOW
8	FMUTE	Soft mute enable	Mute is OFF when TMUTE is LOW. MUTE is ON when TMUTE is HIGH.	FMUTE = LOW

Table 3. Bilingual output logic truth table

BILL	BIRR	Function or mode selected
LOW	LOW	Stereo
LOW	HIGH	Right/right
HIGH	LOW	Left/left
HIGH	HIGH	Invalid setting

Table 4 gives group 2 mode flag information. Table 5 gives output word length logic.

Table 4. Mode flags, group 2

Bit	Flag	Function	Selection	Default
3	CKSL	Clock frequency selection	When CKSL is LOW, 16.9344 MHz. When CKSL is HIGH, 8.4672 MHz.	CKSL = LOW (16.9344 MHz)
4	LRPL	LRCI polarity	When LRPL is LOW, left/right = HIGH/LOW. When LRPL is HIGH, left/right = LOW/HIGH.	LRPL = LOW (left/right = HIGH/LOW)
5	IW18	Input word length selection	16-bit when IW18 is LOW. 18-bit when IW18 is HIGH.	IW18 = LOW (16 bits)
6	OW16	Output word length selection	See table 6.	OW16 = LOW, OW20 = LOW, (18-bit)
7	OW20			
8	OFST	Output DC offset enable	DC offset OFF when OFST is LOW. DC offset ON when OFST is HIGH.	OFST = LOW (OFF)

Table 5. Output word length truth table

OW16	OW20	Output word length
LOW	LOW	18-bit
LOW	HIGH	20-bit
HIGH	LOW	16-bit
HIGH	HIGH	18-bit

Digital Deemphasis

The deemphasis filter is in cascade with the oversampling filters. It is implemented as an IIR filter, and reproduces the deemphasis gain and phase characteristics more faithfully than conventional analog deemphasis filters. Deemphasis is enabled with the TDEEM flag set HIGH. For TDEEM LOW, deemphasis is disabled.

The deemphasis filter coefficients are selected by the TCDDA and TFSEL flags to match the selected sample rate, as shown in table 6.

Table 6. Filter coefficients selection logic

TCDDA	TFSEL	Sample rate	Noise shaping
LOW	LOW	18.9 kHz	ON
LOW	HIGH	37.8 kHz	ON
HIGH	LOW	44.1 kHz	OFF
HIGH	HIGH	44.1 kHz	ON

Attenuation Set Data

Both channels are attenuated by an amount set by the value in the attenuation register. The attenuation is given by

$$\text{Attenuation} = 20 \log_{10}(1 - \text{DATT}/127) \text{ dB}$$

where DATT is the value of the register. Note that a value of 127 gives infinite attenuation, where the output is muted. The register is set to 0 (no attenuation) on reset.

When the attenuation register is changed, the attenuation does not change instantly, but ramps to the new attenuation setting. This prevents unwanted spurious response in the audio output. A temporary register is used to store the current attenuation setting. The attenuation register can be changed again before the attenuation setting is reached. Figure 4 shows attenuation setting data.

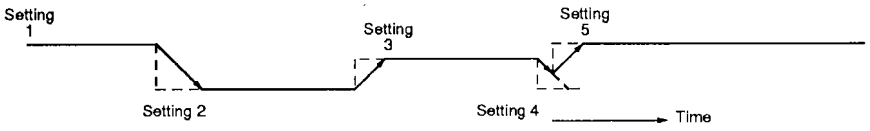


Figure 4. Changing attenuation

Soft Mute

If soft muting is turned ON (by setting the FMUTE flag or the MUTE pin HIGH), the temporary attenuation register is set to 127, causing the attenuation to ramp smoothly to infinity. When muting is released, the attenuation coefficient ramps back to the value in the attenuation register. The final attenuation will be either the attenuation before mute was applied or a new value if the attenuation register was written while MUTE was set.

The time taken to increase attenuation from zero to inifinity is 1024/fs. This corresponds to approximately 23.2 ms at a 44.1 kHz input sample rate.

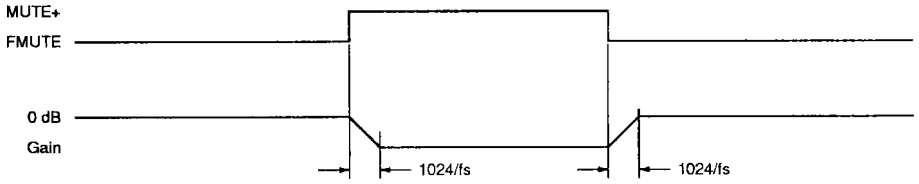


Figure 5. Soft mute timing characteristics

System Clock

The system clock is input on the CKI pin. It can be selected to be either 16.9344 MHz or 8.4672 MHz by the CKSL flag. Because the inverter in the CKI input has a feedback resistor, the clock input can either be DC-coupled or AC-coupled.

If the microcontroller interface is not used, the system clock must be 16.9344 MHz. Setting the CKSL flag HIGH using the microcontroller interface selects an 8.4672 MHz clock. Table 7 shows the clock frequency relative to the sample rate for various sample rate and clock selections.

Table 7. Clock settings

CKSL	TCDDA	TFSEL	Sample rate, fs	Clock frequency, f_{CLK}	
LOW	LOW	LOW	37.8 kHz	448fs	16.9344 MHz
	LOW	HIGH	18.9 kHz	896fs	
	HIGH	×	44.1 kHz	384fs	
HIGH	LOW	LOW	37.8 kHz	224fs	8.4672 MHz
	LOW	HIGH	18.9 kHz	448fs	
	HIGH	×	44.1 kHz	192fs	

Note
× = don't care

Audio Data Input

The bit-serial audio input data is in 16- or 18-bit, 2s complement, msb-first format. The input word length is selected by the IW18 flag.

The data is input on the DIN pin. Each bit is shifted into an input data shift register on the rising edge of the BCKI bit clock. The contents of the shift registers are latched into the input registers on alternate transitions of the word clock LRCI. If the LRPL flag is LOW, the left-channel data is shifted in while LRCI is HIGH and the right-channel data is shifted in while LRCI is LOW. The reverse takes place if LRPL is LOW.

The timing of the input stage is independent of the timing of the arithmetic circuitry. Hence, the phase relationship between the BCKI and LRCI clocks and the system clock does not affect functional operation, provided that the phase relationship remains constant (that is, the frequency ratio of the clocks is constant). This ensures that a certain amount of jitter in the input clock does not affect output signal timing.

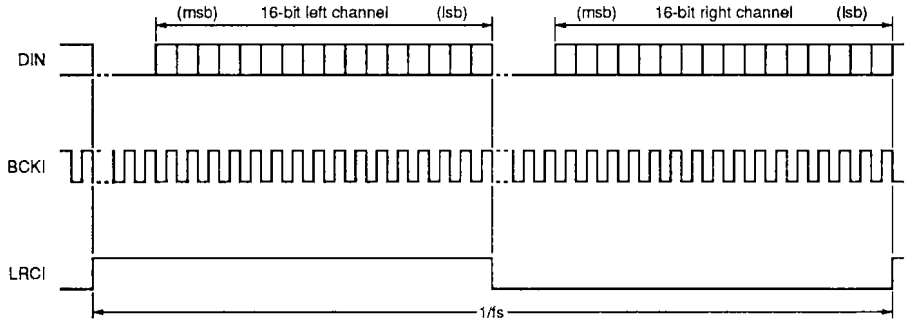


Figure 6. Audio data input timing (LRPL = LOW)

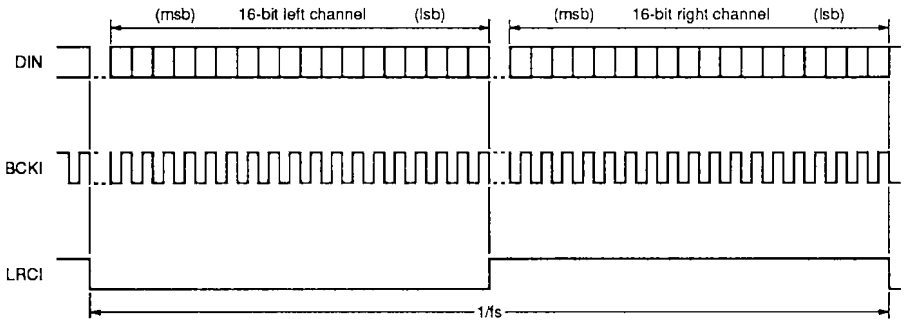


Figure 7. Audio data input timing (LRPL = HIGH)

Data Output

The audio output data is in bit-serial, 2s complement, msb-first format. The output word length is 16-, 18- or 20-bit, as selected by the OW16 and OW20 flags.

The first-order noise shaper circuit follows the filtering circuits. It reduces the quantization for 16- and 18-bit output word lengths to the same level as unprocessed 18- and 20-bit word lengths. Note that the noise shaper does not operate if TCDDA is HIGH and TFSEL is LOW.

Output DC Offset

A constant DC offset of approximately 0.8% is added to the filter output if the OFST flag is set. This reduces D/A converter zero-crossing noise for small output signals. The offset amounts are for 16-bit output, 512 × lsb; for 18-bit output, 2047 × lsb; for 20-bit output, 8188 × lsb.

Bilingual Output

The SM5840JP/JS can be set to output only one of the input channels on both output channels. This is commonly used for selecting one language or the other from bilingual program material. Both output channels carry the left-channel input if the BILL flag is set, or the right-channel input if the BIRR flag is set. The outputs are conventional stereo if neither flag is set.

Output Timing

The BCKO output carries the output bit clock, generated within the SM5840JP/JS. The data outputs, DOL and DOR, change on the falling edge of BCKO. The bit clock rate and number of bit periods per output word depend on the setting of TCDDA, as shown in table 8.

Figures 8 and 9 show the output timing for both settings of TCDDA. Clock and data pulses for bits 17 and 18, shown as dotted lines, are present in 18-bit output mode. Clock and data pulses for bits 17 to 20 are present in 20-bit output mode.

Table 8. Output timing

Parameter	TCDDA = HIGH	TCDDA = LOW
Output bit clock rate, t_B	1/192fs	1/224fs
Bit periods per word, t_{DW}	$24t_B$	$28t_B$

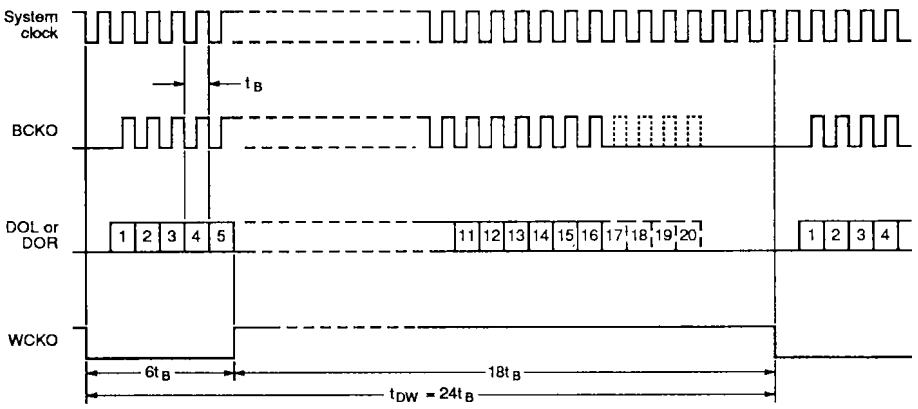


Figure 8. HIGH-level TCDDA output timing

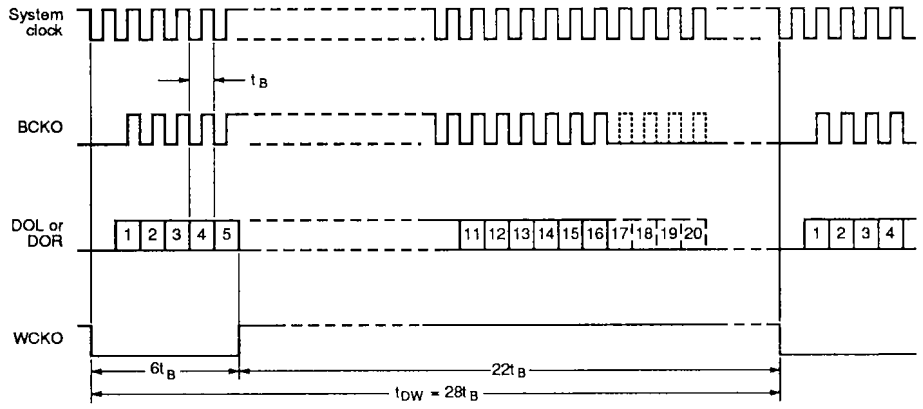


Figure 9. LOW-level TCDDA output timing

System Reset

The SM5840JP/JS must be reset following power-on by applying a LOW-level pulse to the $\overline{RST}$ pin. On the first rising edge of LRCI after $\overline{RST}$ is released, the following actions take place:

- All mode flags are reset to logic 0. The corresponding modes are shown in tables 2 and 3.
- The attenuator register is set to zero (no attenuation is applied to the signal).
- The arithmetic and output timing counters are reset.

A power-on reset can be effected either by a signal from the controlling microprocessor or by connecting a capacitor of approximately 300 pF between $\overline{RST}$ and VSS. Note that, in either case, CKI and LRCI must stabilize before $\overline{RST}$ goes HIGH. A larger capacitor can be used to ensure that this is the case.

The SM5840JP/JS automatically resets its internal timing counters whenever the TCDDA or LRPL flags change, so a device reset is not required. Because of the phase independence of the different internal clocks, the device does not need to be reset after the TFSEL or CKSL flags change or after the LRCI or CKI input clocks change.

The device must be reset in the following cases:

1. If CKI halts for 10 µs or more.
2. If the CDDA or FSEL flags change, or the LRCI or CKI signals change. Note that the timing relationship established between LRCI and WCKO after a reset must be maintained and all flags must be set back to their desired status.

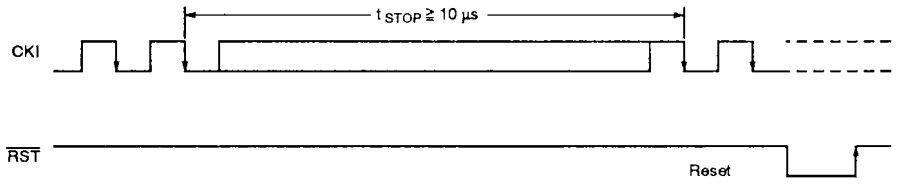


Figure 10. Reset after CKI halt

When $\overline{RST}$ goes LOW, the DOL and DOR outputs immediately go LOW. The BCKO and WCKO outputs do not stop. See figure 11.

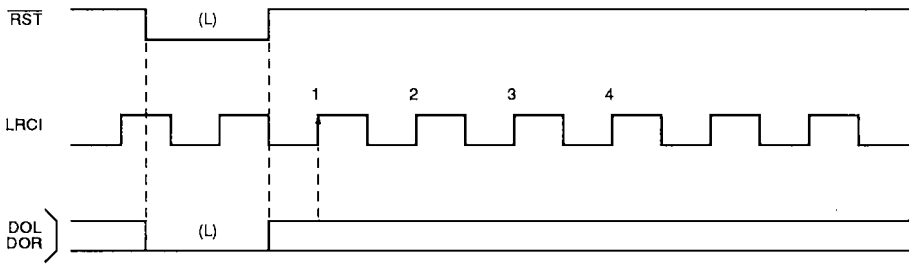
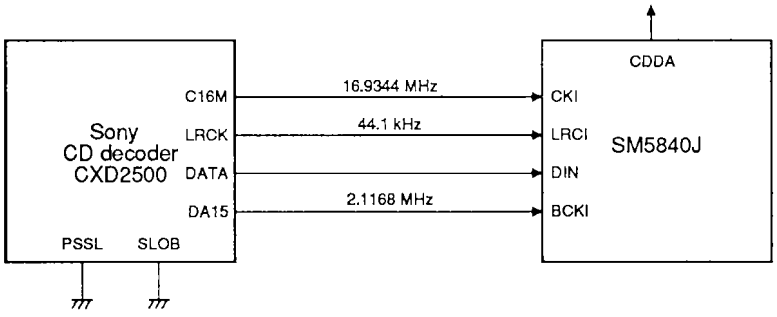


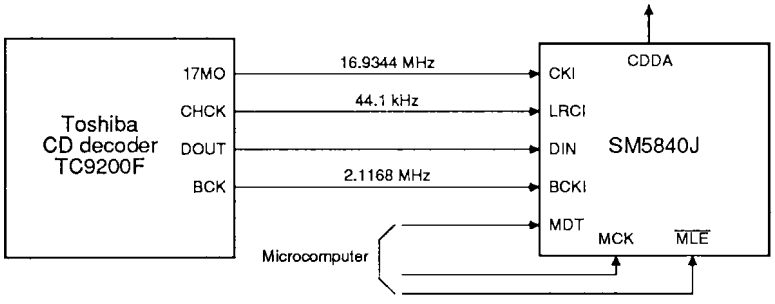
Figure 11. Output timing on reset

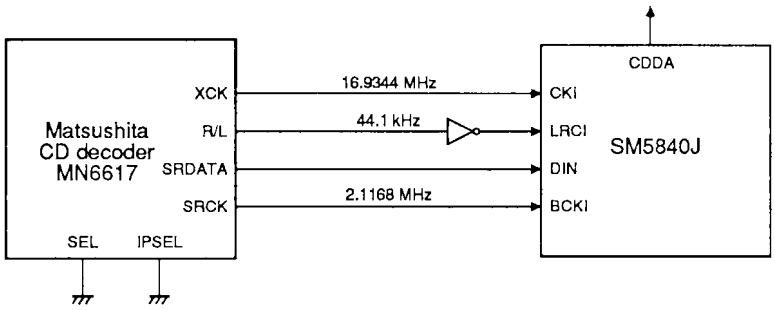
APPLICATION CIRCUITS

These circuits show signal formats and interconnection only. The system designer must also consider timing relationships.

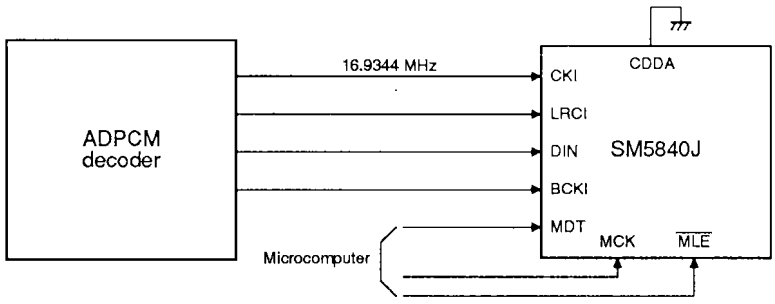
CD-DA Interface Examples



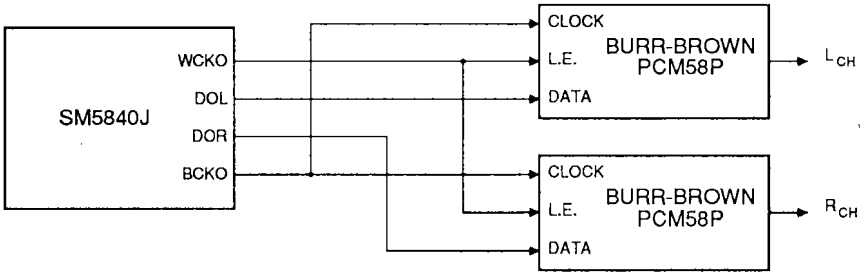




ADPCM Decoder Interface



18-bit 2 × DAC Interface



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