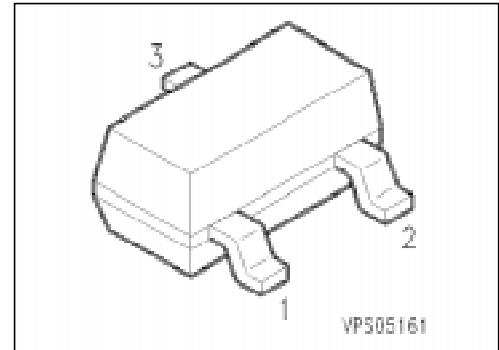


NPN Silicon Switching Transistor

SMBT 4124

- High current gain: 0.1 mA to 100 mA
- Low collector-emitter saturation voltage



Type	Marking	Ordering Code (tape and reel)	Pin Configuration			Package ¹⁾
			1	2	3	
SMBT 4124	sZC	Q68000-A8316	B	E	C	SOT-23

Maximum Ratings

Parameter	Symbol	Values	Unit
Collector-emitter voltage	V_{CE0}	25	V
Collector-base voltage	V_{CB0}	30	
Emitter-base voltage	V_{EB0}	5	
Collector current	I_C	200	mA
Total power dissipation, $T_s = 69\text{ °C}$	P_{tot}	330	mW
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	- 65 ... + 150	

Thermal Resistance

Junction - ambient ²⁾	$R_{th\ JA}$	≤ 315	K/W
Junction - soldering point	$R_{th\ JS}$	≤ 245	

¹⁾ For detailed information see chapter Package Outlines.

²⁾ Package mounted on epoxy pcb 40 mm × 40 mm × 1.5 mm/6 cm² Cu.

Electrical Characteristics

at $T_A = 25\text{ °C}$, unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

DC characteristics

Collector-emitter breakdown voltage $I_C = 1\text{ mA}$	$V_{(BR)CE0}$	25	–	–	V
Collector-base breakdown voltage $I_C = 10\text{ }\mu\text{A}$	$V_{(BR)CB0}$	30	–	–	
Emitter-base breakdown voltage $I_E = 10\text{ }\mu\text{A}$	$V_{(BR)EB0}$	5	–	–	
Collector-base cutoff current $V_{CB} = 20\text{ V}, I_E = 0$	I_{CB0}	–	–	50	nA
Emitter-base cutoff current $V_{EB} = 3\text{ V}, I_C = 0$	I_{EB0}	–	–	50	
DC current gain $I_C = 2\text{ mA}, V_{CE} = 1\text{ V}$ $I_C = 50\text{ mA}, V_{CE} = 1\text{ V}$	h_{FE}	120 60	– –	360 –	–
Collector-emitter saturation voltage ¹⁾ $I_C = 50\text{ mA}, I_B = 5\text{ mA}$	V_{CEsat}	–	–	0.3	V
Base-emitter saturation voltage ¹⁾ $I_C = 50\text{ mA}, I_B = 5\text{ mA}$	V_{BEsat}	–	–	0.95	

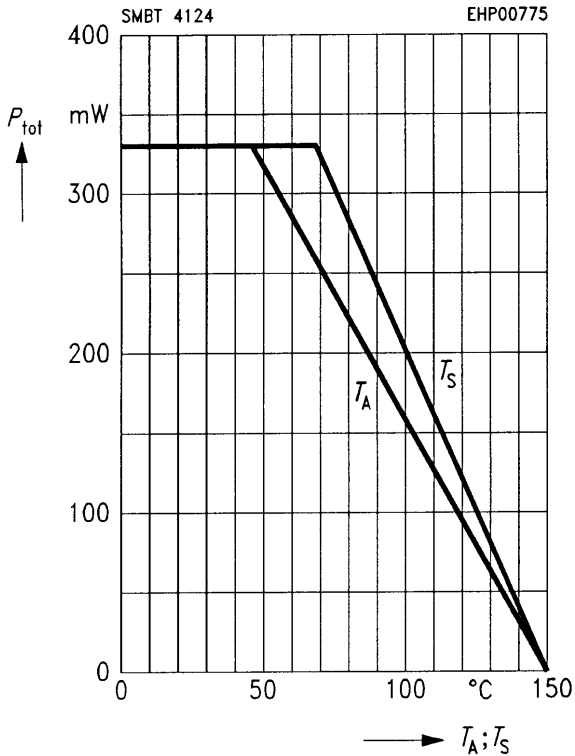
AC characteristics

Transition frequency $I_C = 10\text{ mA}, V_{CE} = 20\text{ V}, f = 100\text{ MHz}$	f_T	300	–	–	MHz
Output capacitance $V_{CB} = 5\text{ V}, f = 1\text{ MHz}$	C_{obo}	–	–	4	pF
Input capacitance $V_{EB} = 0.5\text{ V}, f = 1\text{ MHz}$	C_{ibo}	–	–	8	
Small-signal current gain $I_C = 1\text{ mA}, V_{CE} = 5\text{ V}, f = 1\text{ kHz}$	h_{te}	120	–	480	–
Noise figure $I_C = 0.1\text{ mA}, V_{CE} = 5\text{ V}, f = 10\text{ Hz to }15\text{ kHz}$ $R_S = 1\text{ k}\Omega$	NF	–	–	5	dB

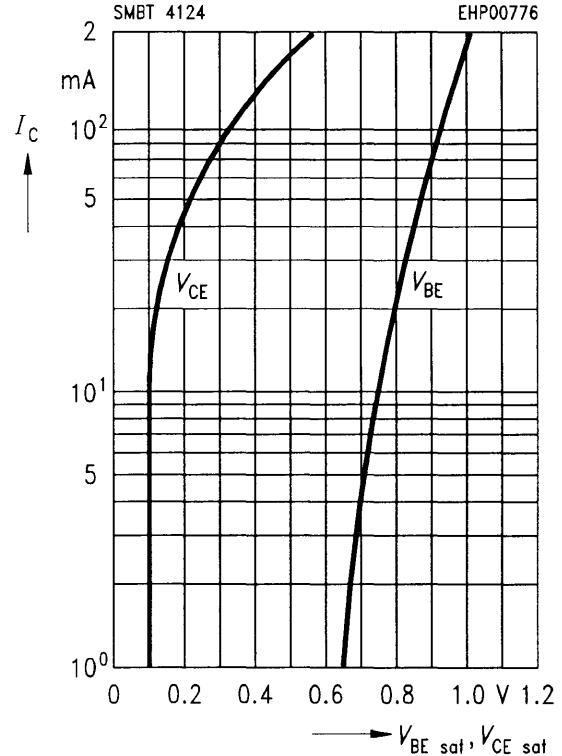
¹⁾ Pulse test conditions: $t \leq 300\text{ }\mu\text{s}, D \leq 2\%$.

Total power dissipation $P_{tot} = f(T_A^*; T_S)$

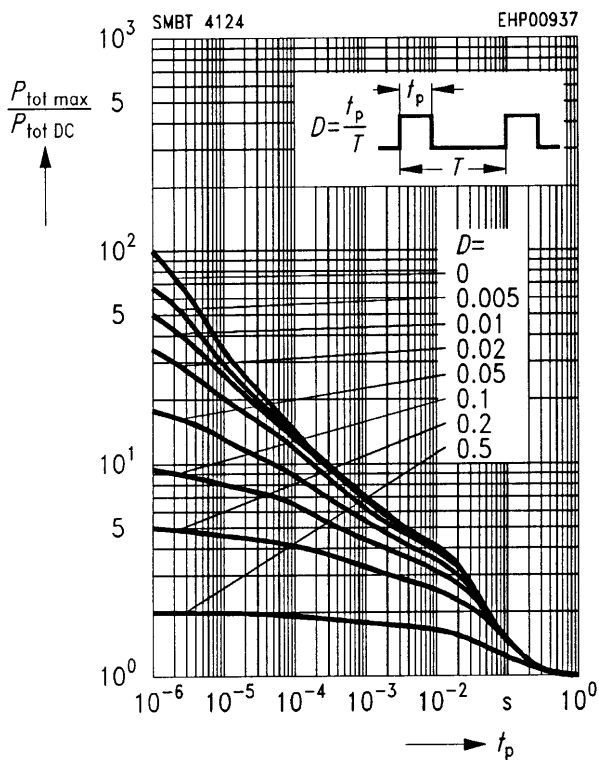
* Package mounted on epoxy



Saturation voltage $I_C = f(V_{BE sat}, V_{CE sat})$

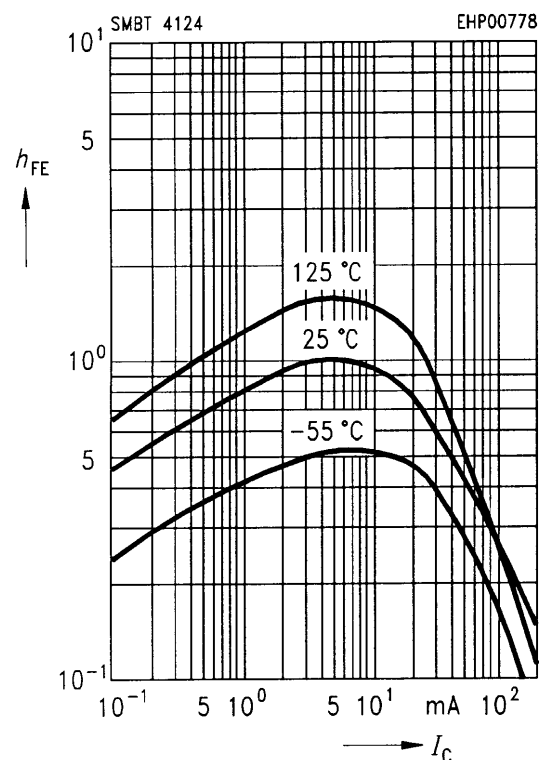


Permissible pulse load $P_{tot max} / P_{tot DC} = f(t_p)$



DC current gain $h_{FE} = f(I_C)$

$V_{CE} = 10 V$, normalized



Small-signal current gain $h_{fe} = f(I_C)$

$V_{CE} = 10 \text{ V}, f = 1 \text{ MHz}$

