

## Preliminary Data Sheet VSC7940

SONET/SDH 3.125Gb/s  
Laser Diode Driver with Automatic Power Control

### Features

- Power Supply: 5V  $\pm$ 5%
- DC-Coupled to Laser Diode
- Programmable Modulation Current: 5mA to 100mA
- Programmable Bias Current: 1mA to 100mA
- Enable/Disable Control
- Automatic Optical Average Power Control
- Modulation and Bias Current Monitors

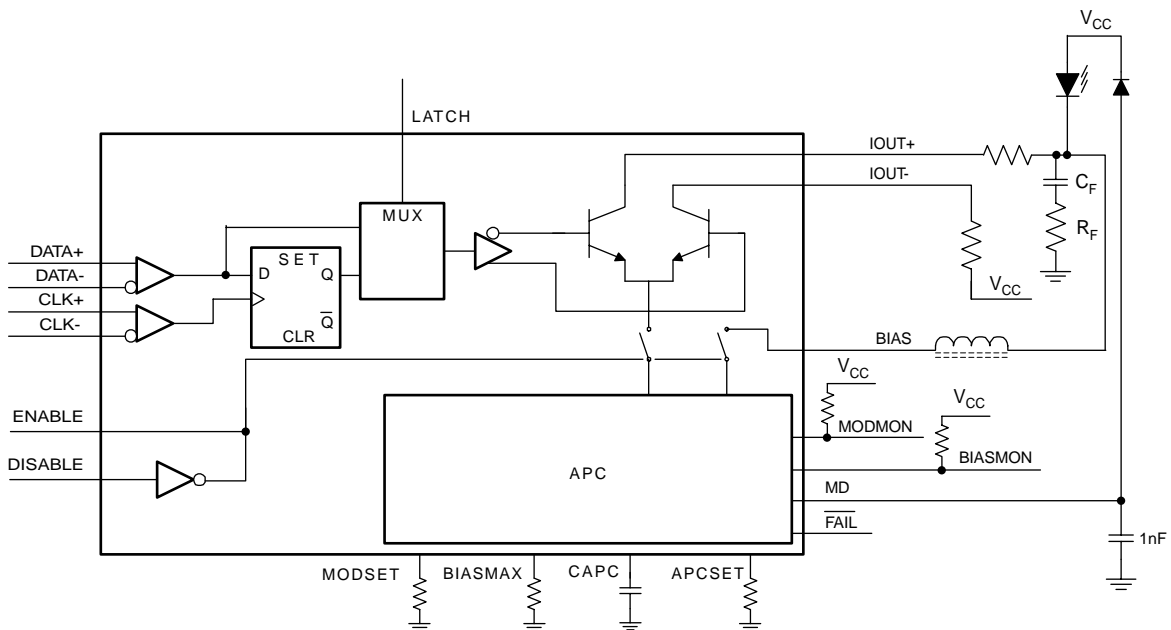
### Applications

- SONET/SDH at 622Mb/s, 1.244Gb/s, 2.488Gb/s, 3.125Gb/s
- Full-Speed Fibre Channel (1.062Gb/s)

### General Description

The VSC7940 is a single 5V supply laser diode driver specially designed for SONET/SDH applications up to 3.125Gb/s. External resistors set a wide range of bias and modulation currents for driving the laser. Data and clock inputs accept differential PECL signals. The Automatic Power Control (APC) loop maintains a constant average optical power over temperature and lifetime. The dominant pole of the APC loop can be controlled with an external capacitor. Other features include enable/disable control, programmable slow-start circuit to set laser turn-on delay, and failure-monitor output to indicate when the APC loop is unable to maintain the average optical power. The VSC7940 is available in die form or in a 32-pin TQFP package.

### Block Diagram



## Electrical Characteristics

**Table 1: AC Specifications**

AC specifications are guaranteed by design and characterization. Typical values are for 5V operation.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t <sub>SU</sub>	Input Latch Setup Time	100			ps	LATCH=high
t <sub>H</sub>	Input Latch Hold Time	100			ps	LATCH=high
	Enable/Start-up Delay		250		ns	
t <sub>R</sub>	Output Rise Time		TBD	TBD	ps	20% to 80%
t <sub>F</sub>	Output Fall Time		TBD	TBD	ps	20% to 80%
PWD	Pulse Width Distortion		10	50	ps	See Notes 1, 2
CID <sub>MAX</sub>	Maximum Consecutive Identical Digits	80			bits	
t <sub>J</sub>	Jitter Generation		7	20	ps <sub>p-p</sub>	Jitter BW=12kHz to 20MHz, 0-1 pattern.

NOTES: (1) Measured with 622Mb/s 0-1 pattern, LATCH=high. (2) PWD = (wider pulse - narrower pulse) / 2.

**Table 2: DC Specifications**

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V <sub>SS</sub>	Power Supply Voltage	4.75	5.0	5.25	V	
I <sub>CC</sub>	Power Supply Current		TBD	45	mA	R <sub>MODSET</sub> =7.3kΩ R <sub>BIASMAX</sub> =4.8kΩ I <sub>BIAS</sub> and I <sub>MOD</sub> excluded, V <sub>CC</sub> =5V
I <sub>BIAS</sub>	Bias Current Range	1		100	mA	Voltage at BIAS pin=(V <sub>CC</sub> -1.6)
I <sub>BIAS-OFF</sub>	Bias Off Current			100	μA	ENABLE=low or DISABLE=high <sup>(1)</sup>
S <sub>BIAS</sub>	Bias Current Stability		230		ppm/°C	APC open loop. I <sub>BIAS</sub> =100mA
			900			APC open loop. I <sub>BIAS</sub> =1mA
	Bias Current Absolute Accuracy		±15		%	Refers to part-to-part variation
VR <sub>MD</sub>	Monitor Diode Reverse Bias Voltage	1.5			V	
I <sub>MD</sub>	Monitor Diode Reverse Current Range	18		1000	μA	
	Monitor Diode Bias Setpoint Stability		-480	-50	ppm/°C	I <sub>MD</sub> =1mA <sup>(2)</sup>
				90		I <sub>MD</sub> =18μA <sup>(2)</sup>
	Monitor Diode Bias Absolute Accuracy	-15		15	%	Refers to part-to-part variation
I <sub>MOD</sub>	Modulation Current Range	5		100	mA	
I <sub>MOD-OFF</sub>	Modulation Off Current			200	μA	ENABLE=low or DISABLE=high <sup>(1)</sup>
	Modulation Current Absolute Accuracy		±15		%	See Note 2

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Symbol	Parameter	Min	Typ	Max	Units	Conditions
	Modulation Current Stability	-480	-50	480	ppm/°C	$I_{MOD}=60mA$
			250			$I_{MOD}=5mA$
$A_{BIAS}$	BIASMON to $I_{BIAS}$ Gain		37			$I_{BIAS}/I_{BIASMON}$
$A_{MOD}$	MODMON to $I_{MON}$ Gain		29			$I_{MOD}/I_{MODMON}$

NOTES: (1) Both  $I_{BIAS}$  and  $I_{MOD}$  will turn off if any of the current set pins are grounded. (2) Assumes laser diode to monitor diode transfer function does not change with temperature.

**Table 3: PECL and TTL/CMOS Input/Output Specifications**

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{ID}$	Differential Input Voltage	100		1600	mV <sub>p-p</sub>	(DATA+)-(DATA-)
$V_{ICM}$	Common-Mode Input Voltage	$V_{CC} - 1.49$	$V_{CC} - 1.32$	$V_{CC} - V_{ID}/4$	V	PECL-compatible
$I_{IN}$	Clock and Data Input Current	-1		10	mA	
$V_{IH}$	TTL Input High Voltage (ENABLE, LATCH)	2.0			V	
$V_{IL}$	TTL Input Low Voltage (ENABLE, LATCH)			0.8	V	
	TTL Output High Voltage ( $\overline{FAIL}$ )	2.4	$V_{CC} - 0.3$	$V_{CC}$	V	Sourcing 50 $\mu$ A
	TTL Output Low Voltage ( $\overline{FAIL}$ )	0.1		0.44	V	Sinking 100 $\mu$ A

### Absolute Maximum Ratings<sup>(1)</sup>

Power Supply Voltage ( $V_{CC}$ ).....	-0.5V to +7V
Current into BIAS.....	-20mA to +150mA
Current into OUT+, OUT-.....	TBD
Current into MD.....	-5mA to +5mA
Current into $\overline{FAIL}$ .....	-10mA to 30mA
Voltage at DATA+, DATA-, CLK+, CLK-, ENABLE, LATCH.....	-0.5V to ( $V_{CC} + 0.5V$ )
Voltage at APCFILT, MODSET, BIASMAX, APCSET, MD, $\overline{FAIL}$ .....	-0.5V to +3.0V
Voltage at OUT+, OUT-.....	-0.5V to ( $V_{CC} + 1.5V$ )
Voltage at BIAS.....	-0.5V to ( $V_{CC} + 0.5V$ )
Continuous Power Dissipation ( $T_A = +85^\circ C$ , TQFP derate 20.8mW/°C above +85°C).....	1350mW
Operating Junction Temperature Range.....	-55°C to +150°C
Storage Temperature Range.....	-65°C to +165°C

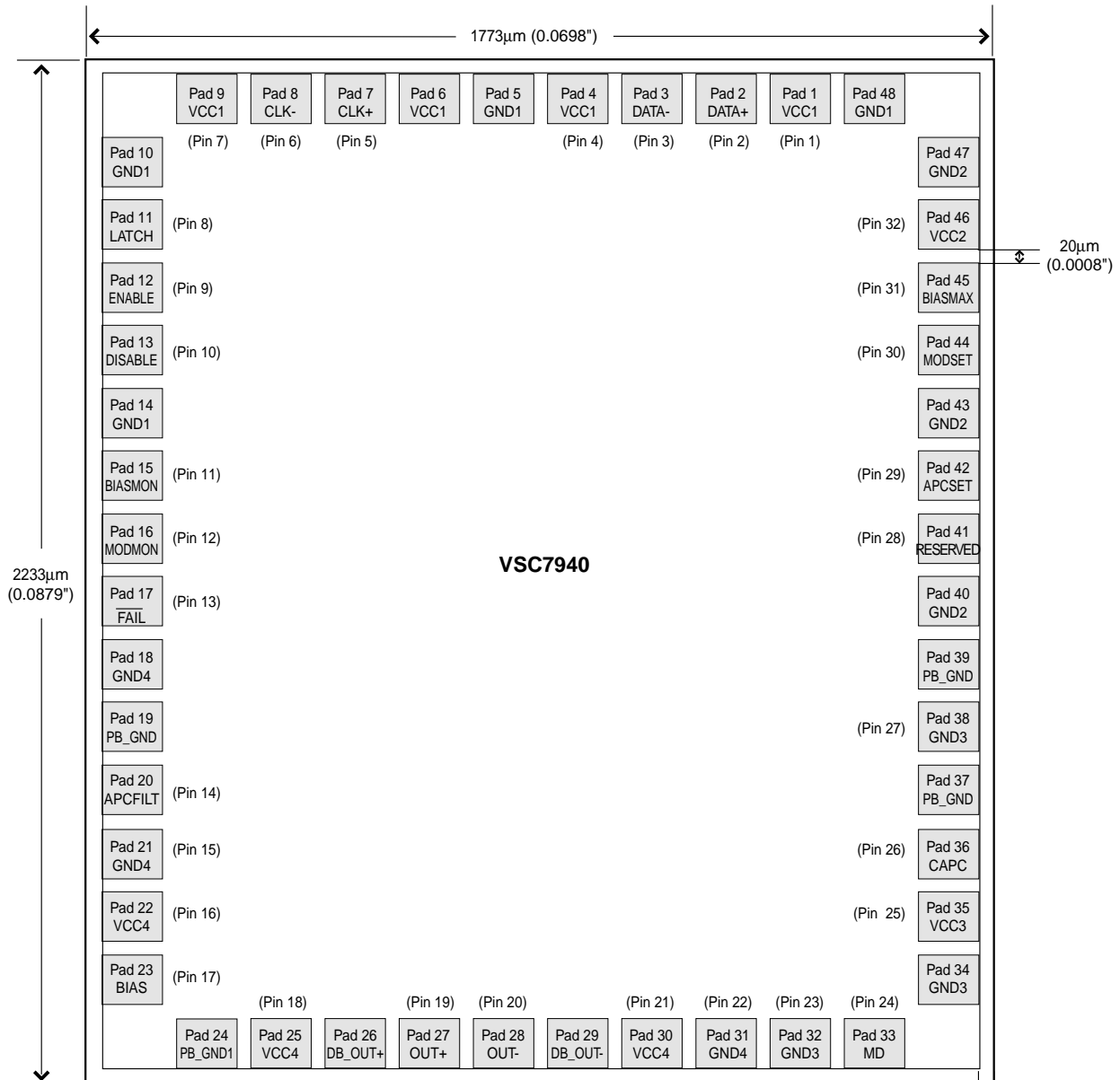
NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

### Recommended Operating Conditions

Positive Voltage Rail ( $V_{CC}$ ).....	+5V
Negative Voltage Rail (GND).....	0V
Ambient Temperature Range ( $T_A$ ).....	-40°C to +85°C

## Bare Die Pad Descriptions

Figure 1: Pad Assignments



Die Size: 1773µm x 2233µm (0.0698" x 0.0879")  
 Die Thickness: 625µm (0.0246")  
 Pad Pitch: 115µm (0.0045")  
 Pad to Pad Clearance: 20µm (0.0008")  
 Pad Passivation Opening: 95µm x 95µm (0.0037" x 0.0037")

75µm  
(0.0030")

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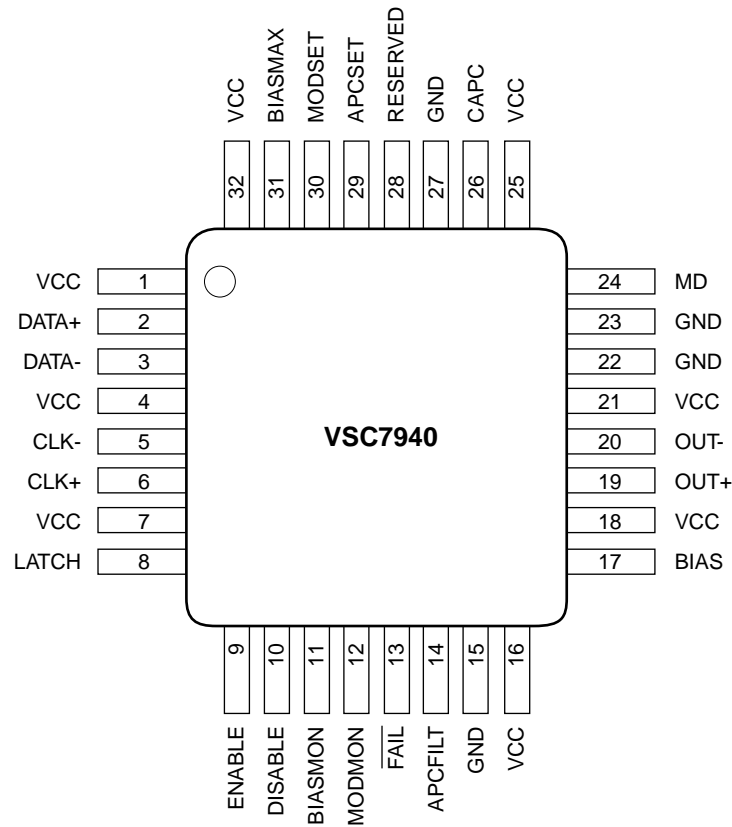
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**Table 4: Pad Coordinates**

Signal Name	Pad No.	Coordinates ( $\mu\text{m}$ )		Signal Name	Pad No.	Coordinates ( $\mu\text{m}$ )	
		X	Y			X	Y
VCC1	1 (Pin 1)	1211.025	1995.05	VCC4	25 (Pin 18)	406.025	80.95
DATA+	2 (Pin 2)	1096.025	1995.05	DB_OUT+	26	521.025	80.95
DATA-	3 (Pin 3)	981.025	1995.05	OUT+	27 (Pin 19)	636.025	80.95
VCC1	4 (Pin 4)	866.025	1995.05	OUT-	28 (Pin 20)	751.025	80.95
GND1	5	751.025	1995.05	DB_OUT-	29	866.025	80.95
VCC1	6	636.025	1995.05	VCC4	30 (Pin 21)	981.025	80.95
CLK+	7 (Pin 5)	521.025	1995.05	GND4	31 (Pin 22)	1096.025	80.95
CLK-	8 (Pin 6)	406.025	1995.05	GND3	32 (Pin 23)	1211.025	80.95
VCC1	9 (Pin 7)	291.025	1995.05	MD	33 (Pin 24)	1326.025	80.95
GND1	10	80.95	1784.975	GND3	34	1535.05	289.975
LATCH	11 (Pin 8)	80.95	1669.975	VCC3	35 (Pin 25)	1535.05	404.975
ENABLE	12 (Pin 9)	80.95	1554.975	CAPC	36 (Pin 26)	1535.05	519.975
DISABLE	13 (Pin 10)	80.95	1439.975	PB_GND	37	1535.05	634.975
GND1	14	80.95	1324.975	GND3	38 (Pin 27)	1535.05	749.975
BIASMON	15 (Pin 11)	80.95	1209.975	PB_GND	39	1535.05	864.975
MODMON	16 (Pin 12)	80.95	1094.975	GND2	40	1535.05	979.975
FAIL	17 (Pin 13)	80.95	979.975	RESERVED	41 (Pin 28)	1535.05	1094.975
GND4	18	80.95	864.975	APCSET	42 (Pin 29)	1535.05	1209.975
PB_GND	19	80.95	749.975	GND2	43	1535.05	1324.975
APCFILT	20 (Pin 14)	80.95	634.975	MODSET	44 (Pin 30)	1535.05	1439.975
GND4	21 (Pin 15)	80.95	519.975	BIASMAX	45 (Pin 31)	1535.05	1554.975
VCC4	22 (Pin 16)	80.95	404.975	VCC2	46 (Pin 32)	1535.05	1669.975
BIAS	23 (Pin 17)	80.95	289.975	GND2	47	1535.05	1784.975
PB_GND	24	291.025	80.95	GND1	48	1336.025	1995.05

## Package Pin Description

Figure 2: Pin Diagram



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**Table 5: Pin Identifications**

<i>Pin Name</i>	<i>Pin Number</i>	<i>Description</i>
GND	10, 15, 22, 23, 27	Ground
V <sub>CC</sub>	1, 4, 7, 16, 18, 21, 25, 32	Power Supply
DATA+	2	Positive Data Input (PECL)
DATA-	3	Negative Data Input (PECL)
CLK+	5	Positive Clock Input (PECL). Connect to V <sub>CC</sub> if LATCH function is not used.
CLK-	6	Negative Clock Input (PECL). Leave unconnected if LATCH function is not used.
LATCH	8	Latch Input (TTL/CMOS). Connect to V <sub>CC</sub> for data retiming and GND for direct data.
ENABLE	9	Enable Input (TTL/CMOS). If used, connect DISABLE to GND. Connect to V <sub>CC</sub> for normal operation and GND to disable laser bias and modulation currents.
DISABLE	10	Disable Input (TTL/CMOS). If used, leave ENABLE pin floating. Connect to GND for normal operation and V <sub>CC</sub> to disable laser bias and modulation currents.
BIASMON	11	Bias Current Monitor. Sink current source that is proportional to the laser bias current.
MODMON	12	Modulation Current Monitor. Sink current source that is proportional to the laser modulation current.
FAIL	13	Output (TTL/CMOS). When low, indicates APC failure.
APCFILT	14	No effect on device operation.
BIAS	17	Laser Bias Current Output
OUT+	19	Positive Modulation-Current Output. I <sub>MOD</sub> flows when input data is high.
OUT-	20	Negative Modulation-Current Output. I <sub>MOD</sub> flows when input data is low.
MD	24	Monitor Diode Input. Connect to monitor photodiode anode. Connect capacitor to GND to filter high-speed AC monitor photocurrent.
CAPC	26	Capacitor to GND sets dominant pole of the APC feedback loop.
RESERVED	28	Do not connect.
APCSET	29	Resistor to GND sets desired average optical power. If APC is not used, connect 100kΩ resistor to GND.
MODSET	30	Connect resistor to GND to set desired modulation current.
BIASMAX	31	Connect resistor to GND to set maximum bias current. The APC function can subtract from this value, but cannot add to it.

## Detailed Description

The VSC7940 is a high-speed laser driver with Automatic Power Control. The device is designed to operate up to 3.125Gb/s with a 5V supply. The data and clock inputs support PECL inputs as well as other inputs that meet the common-mode voltage and differential voltage swing specifications. The differential pair output stage is capable of sinking up to 100mA into the laser with typical rise and fall times of 60ps. The VSC7940 is designed to be DC-coupled. The key features of the VSC7940 are its Automatic Power Control, low power supply current, and fast rise and fall times. The VSC7938 and VSC7939 are similar Vitesse laser drivers designed for 60mA maximum output modulation currents. These laser drivers may be powered from a 3.3V or 5V supply and may be AC- or DC-coupled to the laser diode. The VSC7939 is available in the same 32-pin TQFP package as the VSC7940. The VSC7938 is available in a 48-pin TQFP package.

### Automatic Power Control

To ensure constant average optical power, the VSC7940 utilizes an Automatic Power Control (APC) loop. A photodiode mounted in the laser package provides optical feedback to compensate for changes in average laser output power due to changes that affect laser performance such as temperature and laser lifetime. The laser bias current is adjusted by the APC loop according to the reference current set at APCSET by an external resistor. An external capacitor at CAPC controls the time constant for the APC feedback loop. The recommended value for CAPC is 0.1 $\mu$ F. This value reduces pattern-dependent jitter associated with the APC feedback loop and guarantees stability. Because the APC loop noise is internally filtered, APCFILT is not internally connected and does not need to be connected to any external components. The device's performance will not be affected if a capacitor is connected to APCFILT. If the APC loop cannot adjust the bias current to track the desired monitor current, FAIL is set low.

The device may be operated with or without APC. To utilize APC, a capacitor must be connected at CAPC (0.1 $\mu$ F) and a resistor must be connected at APCSET to set the average optical power. For open-loop operation (no APC), a 100k $\Omega$  resistor should be connected between APCSET and GND. CAPC has no effect on open-loop operation. In both modes of operation, resistors to ground should be placed at BIASMAY and MODSET to set the bias and modulation currents.

### Data Retiming

The VSC7940 provides inputs for differential PECL clock signals for data retiming to minimize jitter at high speeds. To incorporate this function, LATCH should be connected to V<sub>CC</sub>. If this function is unused, CLK+ should be connected to V<sub>CC</sub>, CLK- should be left unconnected, and LATCH should be connected to GND.

### Short-Circuit Protection

If BIASMAY or MODSET are shorted to ground, the output modulation and bias currents will be turned off.

### Modulation and Bias Current Monitors

The VSC7940 provides monitoring of the modulation and bias currents via BIASMAY and MODMON. These pins sink a current proportional to the actual modulation and bias currents. MODMON sinks approximately 1/29th of the amount of modulation current and BIASMAY sink approximately 1/37th of the amount of the bias current. These pins should be tied through a pull-up resistor to V<sub>CC</sub>. The resistors must be chosen such that the voltage at MODMON is greater than V<sub>CC</sub> - 1.0V and the voltage at BIASMAY is greater than V<sub>CC</sub> - 1.6V.



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#### Enable/Disable

Two pins are provided to allow either ENABLE or DISABLE control. If ENABLE is used, connect DISABLE to ground. If DISABLE is used, leave ENABLE floating. Both modulation and bias currents are turned off when ENABLE is low or DISABLE is high. Typically, ENABLE or DISABLE responds to within approximately 250ns.

#### Controlling the Modulation Current

The output modulation current may be determined from the following equation where  $P_{p-p}$  is the peak-to-peak optical power,  $P_{AVE}$  is the average power,  $r_e$  is the extinction ratio, and  $\eta$  is the laser slope efficiency:

$$I_{MOD} = P_{p-p} / \eta = 2 * P_{AVE} * (r_e - 1) / (r_e + 1) / \eta$$

A resistor at MODSET controls the output bias current. Graphs of  $I_{MODSET}$  vs.  $R_{MODSET}$  in *Typical Operating Characteristics* describe the relationship between the resistor at MODSET and the output modulation current at 25°C. After determining the desired output modulation current, use the graph to determine the appropriate resistor value at MODSET.

#### Controlling the Bias Current

A resistor at BIASMAX should be used to control the output bias current. Graphs of  $I_{BIASMAX}$  vs.  $R_{BIASMAX}$  in *Typical Operating Characteristics* describe the relationship between the resistor at BIASMAX and the output bias current at 25°C. If the APC is not used, the appropriate resistor value at BIASMAX is determined by first selecting the desired output bias current, and then using the graph to determine the appropriate resistor value at BIASMAX. When using APC, BIASMAX sets the maximum allowed bias current. After determining the maximum end-of-life bias current at 85°C for the laser, refer to the graph of  $I_{BIASMAX}$  vs.  $R_{BIASMAX}$  in *Typical Operating Characteristics* to select the appropriate resistor value.

#### Controlling the APC Loop

To select the resistor at APCSET, use the graph of  $I_{MD}$  vs.  $R_{APCSET}$  in *Typical Operating Characteristics*. The graph relates the desired monitor current to the appropriate resistance value at APCSET.  $I_{MD}$  may be calculated from the desired optical average power,  $P_{AVE}$ , and the laser-to-monitor transfer,  $\rho_{MON}$ , for a specific laser using the following equation:

$$I_{MD} = P_{AVE} * \rho_{MON}$$

#### Laser Diode Interface

An RC shunt network should be placed at the laser output interface. The sum of the resistor placed at the output and the laser diode resistance should be 25Ω. For example, if the laser diode has a resistance of 5Ω, a 20Ω resistor should be placed in series with the laser. For optimal performance, a bypass capacitor should be placed close to the laser anode.

A “snubber network” consisting of a capacitor  $C_F$  and resistor  $R_F$  should be placed at the laser output to minimize reflections from the laser (see Block Diagram). Suggested values for these components are 80Ω and 2pF, respectively, however, these values should be adjusted until an optical output waveform is obtained.

### Reducing Pattern-Dependent Jitter

Three design values significantly affect pattern-dependent jitter; the capacitor at CAPC, the pull-up inductor at the output ( $L_P$ ), and the AC-coupling capacitor at the output ( $C_D$ ). As previously stated, the recommended value for the capacitor at CAPC is 0.1 $\mu$ F. This results in a 10kHz loop bandwidth which makes the pattern-dependent jitter from the APC loop negligible.

For 2.5Gb/s data rates, the recommended value for  $C_D$  is 0.056 $\mu$ F. The time constant at the output is dominated by  $L_P$ . The variation in the peak voltage should be less than 12% of the average voltage over the maximum consecutive identical digit (CID) period. The following equation approximates this time constant for a CID period,  $t$ , of 100UI = 40ns:

$$\tau_{LP} = -t / \ln(1-12\%) = 7.8t = L_P / 25\Omega$$

Therefore, the inductor  $L_P$  should be a 7.8 $\mu$ H SMD ferrite bead inductor for this case.

### Input/Output Considerations

Although the VSC7940 is PECL-compatible, this is not required to drive the device. The inputs must only meet the common-mode voltage and differential voltage swing specifications.

### Power Consumption

The following equation provides the device supply current ( $I_S$ ) in terms of quiescent current ( $I_Q$ ), modulation current ( $I_{MOD}$ ), and bias current ( $I_{BIAS}$ ):

$$I_S = 19\text{mA} + 0.4 * I_{MOD} + 0.16 * I_{BIAS}$$

This equation may be used to determine the estimated power dissipation:

$$P_{DIS} = V_{CC} * I_S$$

For example, if the device were operated at 5V with a 30mA modulation current and a 10mA bias current, the supply current would be:

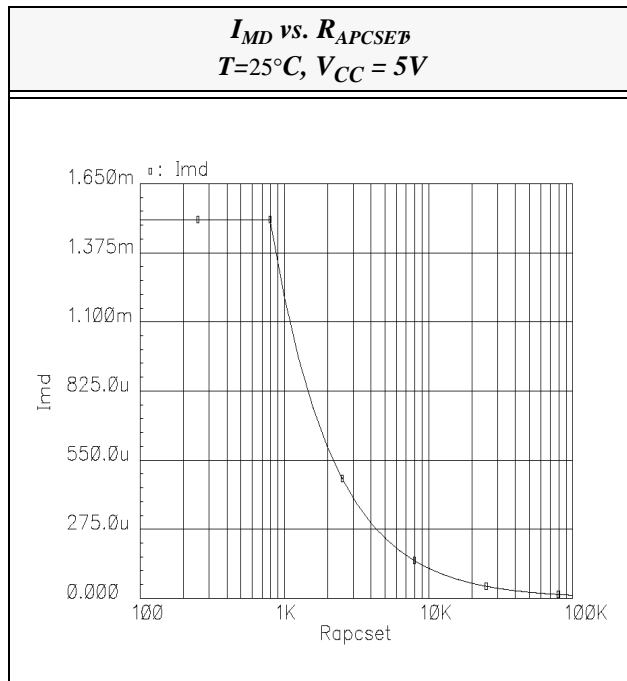
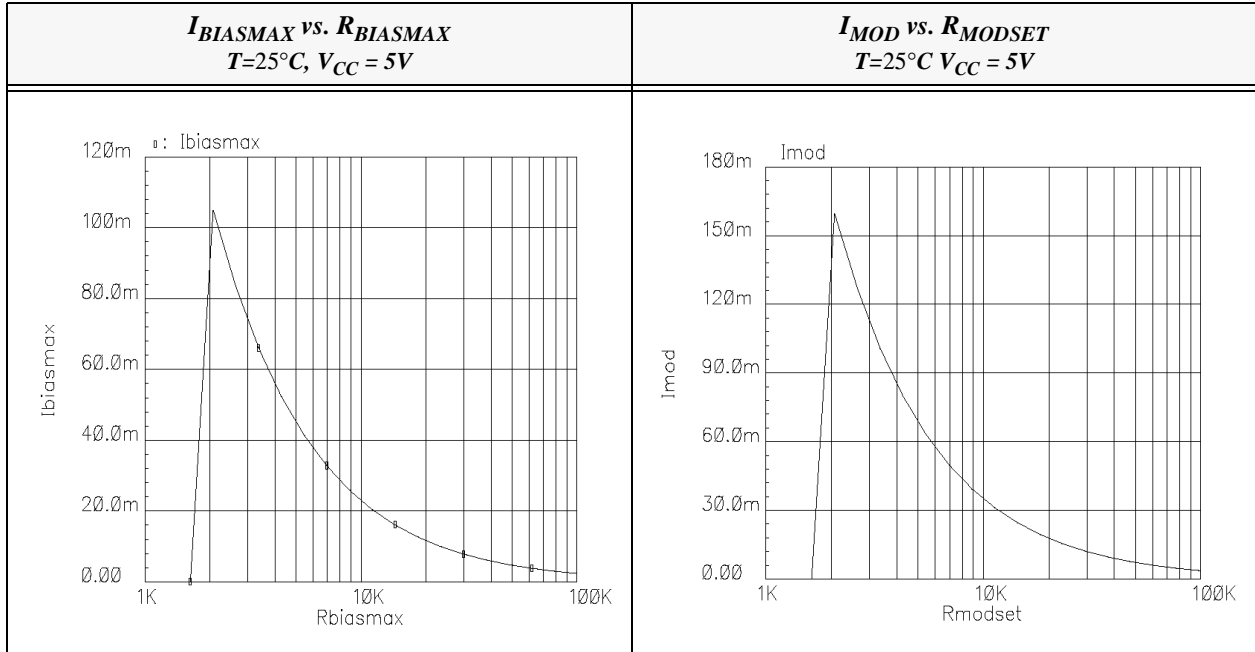
$$I_S = 19\text{mA} + 0.4 * 30\text{mA} + 0.16 * 10\text{mA} = 33\text{mA}$$

This corresponds to a power dissipation of 5V \* 33mA = 165mW.P

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**Typical Operating Characteristics**



## Applications Information

The following is a typical design example for the VSC7940 assuming 5V operation with APC.

### Select a Laser

The Table 8 provides specifications for a typical communication-grade laser capable of operating at 2.5Gb/s.

**Table 6: Typical Laser Characteristics**

Symbol	Parameter	Value	Units
$\lambda$	Wavelength	1310	nm
$P_{AVE}$	Average Optical Output Power	6	mW
$I_{th}$	Threshold Current	6	mA
$\rho_{MON}$	Laser to Monitor Transfer	0.04	mA/mW
$\eta$	Laser Slope Efficiency	0.4	mW/mA
$T_C$	Operating Temperature Range	-40 to +85	°C

### Select Resistor for APCSET

The monitor diode current is estimated by  $I_{MD} = P_{AVE} * \rho_{MON} = 6mW * 0.04mA/mW = 0.24mA$ . The  $I_{MD}$  vs.  $R_{APCSET}$  in *Typical Operating Characteristics* shows the resistor at APCSET should be 5k $\Omega$ .

### Select Resistor for MODSET

To ensure some minimum extinction ratio over temperature and lifetime, assume an optimal extinction ratio of 20 (13dB) at 25°C. The modulation current may be calculated from the following equation:

$$I_{MOD} = P_{p-p} / \eta = 2 * P_{AVE} * (r_e - 1) / (r_e + 1) / \eta = 2 * 6mA * (20 - 1) / (20 + 1) / 0.4 = 27.1mA$$

The graph of  $I_{MODSET}$  vs.  $R_{MODSET}$  in *Typical Operating Characteristics* shows the resistor for MODSET should be 8.5k $\Omega$ .

### Select Resistor for BIASMAX

The maximum threshold current at +85°C and end of life must be determined. A graph of a typical laser's  $I_{th}$  versus  $T_C$  reveals a maximum threshold current of 30mA at 85°C. Therefore, the maximum bias can be approximated by:

$$I_{BIASMAX} = I_{TH-MAX} + I_{MOD} / 2 = 30mA + 27.1mA / 2 = 43.6mA$$

The graph of  $I_{BIASMAX}$  vs.  $R_{BIASMAX}$  in *Typical Operating Characteristics* shows the resistor for BIASMAX should be 5k $\Omega$ .

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#### Select Resistors for MODMON and BIASMON

Assuming the modulation and bias currents never exceed 120mA, the following equations provide values for the resistor at MODMON,  $R_{MODMON}$ , and the resistor at BIASMON,  $R_{BIASMON}$ :

$$R_{MODMON} = 1V * 28 / 120mA = 233\Omega$$

$$R_{BIASMON} = 1.6V * 35 / 120mA = 467\Omega$$

Standard values for these values are  $R_{MODMON} = 232\Omega$  and  $R_{BIASMON} = 464\Omega$ . A voltage of 4.8V at MODMON would indicate a modulation current of:

$$I_{MOD} = (5.2V - 4.8V) * 28 / 232mA = 48mA$$

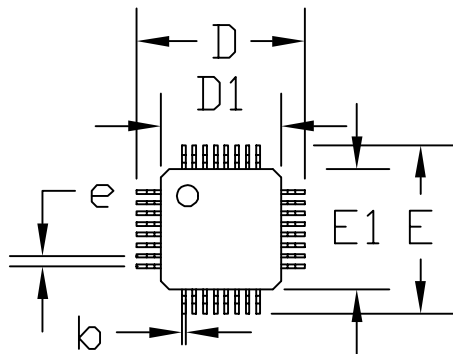
#### Wire Bonding

For best performance, gold ball-bonding techniques are recommended. Wedge bonding is not recommended. For best performance and to minimize inductance keep wire bond lengths short.

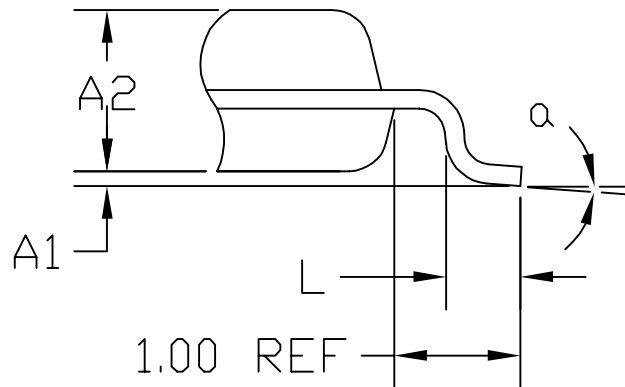
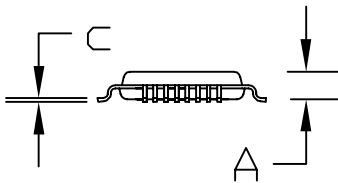
#### PCB Layout Guidelines

Use high frequency PCB layout techniques with solid ground planes to minimize crosstalk and EMI. Keep high speed traces as short as possible for signal integrity. The output traces to the laser diode must be short to minimize inductance. Short output traces will provide best performance.

## Package Information - 32 Pin TQFP



SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
	TQFP		
	MIN.	NOM.	MAX.
A	<del>1.20</del>	<del>1.20</del>	1.20
A1	0.05	<del>0.05</del>	0.15
A2	0.95	1.00	1.05
D	7.00 BSC.		
D1	5.00 BSC.		
E	7.00 BSC.		
E1	5.00 BSC.		
L	0.45	0.60	0.75
N	32		
e	0.50 BSC.		
b	0.17	0.22	0.27
c	0.09	<del>0.09</del>	0.20
a	0	<del>0.05</del>	7



1. All dimensioning and tolerancing conform to ANSI Y14.5-1982
2. Controlling dimension: millimeter
3. This outline conforms to JEDEC Publication 95 Registration MS-026

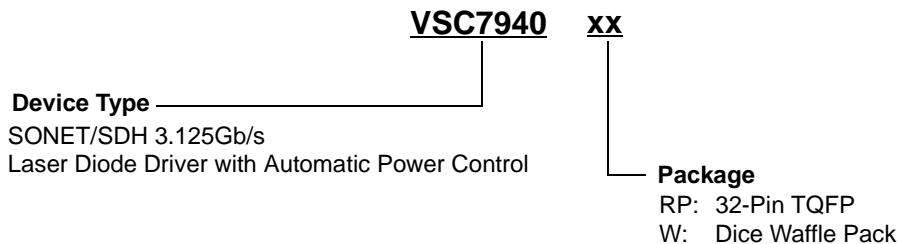
## Preliminary Data Sheet

### VSC7940

SONET/SDH 3.125Gb/s  
Laser Diode Driver with Automatic Power Control

### Ordering Information

The order number for this product is formed by a combination of the device type and package type.



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SONET/SDH 3.125Gb/s  
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**Preliminary Data Sheet**  
**VSC7940**

