# XC25BS5 Series

TOREX

*PLL Clock Generator ICs with Built-In Divider/Multiplier Circuits (For Low Frequency range)*



**◆CMOS Low Power Consumption**
**◆Input Frequency : 12KHz to 35MHz**
**◆Divider Ratio : 1, 3 ~ 2047 divisions (laser trimming)**
**◆Multiplier Ratio : 6 ~ 2047 multiplications (laser trimming)**
**◆Comparative Frequency : 12KHz ~ 500KHz**
**◆Output Frequency : 3MHz ~ 30MHz**
**◆Mini Mold SOT-26 Package**

## ■Applications

●Crystal Oscillation Modules
●Personal Computers
●PDAs
●Portable Audio Systems
●Various System Clocks

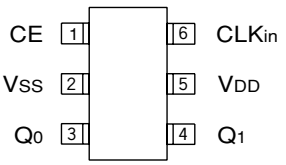
## ■General Description

The XC25BS5 series are high frequency, low power consumption PLL clock generator ICs with divider circuit & multiplier PLL circuit.
Laser trimming gives the option of being able to select from divider ratios (M) of 1,3 to 2047 and multiplier ratios (N) of 6 to 2047.
Output frequency (Q0) is equal to reference oscillation (fCLKin) multiplied by N/M, within a range of 3MHz to 30MHz. Q1 output is selectable from input reference frequency (f0), input reference frequency/2 (f0/2), ground (GND), and comparative frequency (f0/M). Further, comparative frequencies, within a range of 12KHz to 500KHz, can be obtained by dividing the reference oscillation. By halting operation via the CE pin, consumption current can be controlled and output will be one of high-impedance.

## ■Features

**Output Frequency** : 3MHz ~ 30MHz (Q0=fCLKin × N/M)
**Reference Oscillation (fCLKin)**
: 12KHz ~ 35MHz
**Divider Ratio (M)** : Selectable from divisions of 1, 3 ~ 2047
**Multiplier Ratio (N)** : Selectable from multiplications of 6 ~ 2047
**Output** : 3-State
Q1 output selectable from input reference oscillation, input reference oscillation/2, GND, comparative frequency.
**Operating Voltage Range** : 2.97V ~ 5.5V
**Low Power Consumption**
: CMOS (stand-by function included)*1
**Ultra Small Package** : SOT-26 mini mold
*1 High output impedance during standby

## ■Pin Configuration




SOT-26
(TOP VIEW)

## ■ Pin Assignment

| PIN NUMBER | PIN NAME | FUNCTION |
|---|---|---|
| 1 | CE | Chip Enable |
| 2 | VSS | GND |
| 3 | Q0 | PLL Output |
| 4 | Q1 | Reference Oscillation, Reference Oscillation/2, GND, or Comparative Frequency Output |
| 5 | VDD | Power Supply |
| 6 | CLKin | Reference Clock Input |

## ■Function List

●CE, Q0/Q1 Pin Function

| C E | FUNCTION |
|---|---|
| "H" | Q0, Q1clock output |
| "L" | Standby. Ouput pin = high impedance |
| Open | Standby. Ouput pin = high impedance<br>(VSS pin pull down due to IC's internal resistor) |

"H" = High level
"L" = Low level

## ■Product Classification

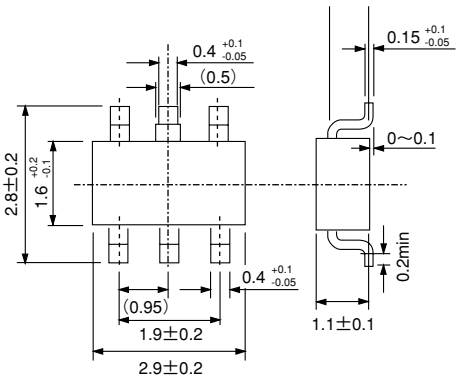
●Ordering Information

XC25BS5 ①②③④⑤

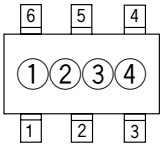
| DESTINATION | DESCRIPTION |
|---|---|
| ①②③ | Denotes Product Number<br>(Based on internal standards)<br><br>e.g. Product Number 001 → ①②③ = 001 |
| ④ | Package<br>M : SOT-26 |
| ⑤ | Device Orientation<br>R : Embossed Tape : Standard Feed<br>L : Embossed Tape : Reverse Feed |

## ■Packaging Information

●SOT-26



## ■Marking




SOT-26
(TOP VIEW)

①Represents the Series name

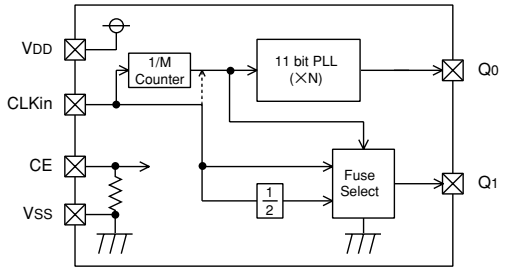
| MARK |
|---|
| 5 |

②③Represents the second and third figure of the Product Number.

| MARK | |
|---|---|
| ② | ③ |
| 0 | 7 |

④Represents the Assembly Lot No.
(Based on internal standards)

## ■Block Diagram




## ■Absolute Maximum Ratings

Ta = 25℃

| PARAMETER | SYMBOL | CONDITIONS | UNITS |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | $V_{SS}$-0.3～$V_{SS}$+7.0 | V |
| CLKin Pin Voltage | $V_{CK}$ | $V_{SS}$-0.3～$V_{DD}$+0.3 | V |
| CE Pin Voltage | $V_{CE}$ | $V_{SS}$-0.3～$V_{DD}$+0.3 | V |
| Q0 Pin Voltage | $V_{Q0}$ | $V_{SS}$-0.3～$V_{DD}$+0.3 | V |
| Q1 Pin Voltage | $V_{Q1}$ | $V_{SS}$-0.3～$V_{DD}$+0.3 | V |
| Q0 Output Current | $I_{Q0}$ | ± 50 | mA |
| Q0 Output Current | $I_{Q1}$ | ± 50 | mA |
| Power Dissipation | PD | 150 | mW |
| Ambient Temp. | Topr | - 30～ +80 | ℃ |
| Storage Temp. | Tstg | - 40～ +125 | ℃ |

## ■ Frequency Configuration : Example 1

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Input Frequency | f CLKin | 11.0000 | - | 16.9344 | MHz |
| Multiplier/Divider Ratio | N/M | - | 1.594 | - | - |
| PLL Output Frequency | $fQ_0$ | 17.5383 | - | 27.0000 | MHz |
| Q1 Output Frequency | $Q_1$ | GND | | | - |

1

### ●Electrical Characteristics (DC)

fCLKin = 16.9344MHz, Multiplier/Divider Ratio = 1.594, Ta = 25°C, No Load

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.97 | 3.3 | 3.63 | V |
| Input Voltage "High" | $V_{IH}$ | | 2.7 | - | - | V |
| Input Voltage "Low" | $V_{IL}$ | | - | - | 0.6 | V |
| Input Current "High" | $I_{IH}$ | $V_{CK}$ = 3.3V | - | - | 3.0 | μA |
| Input Current "Low" | $I_{IL}$ | $V_{CK}$ = 0V | -3.0 | - | - | μA |
| Output Voltage "High" | $V_{OH}$ | $V_{DD}$ = 2.97V,$I_{OH}$ = -8mA | 2.5 | - | - | V |
| Output Voltage "Low" | $V_{OL}$ | $V_{DD}$ = 2.97V,$I_{OL}$ = 8mA | - | - | 0.4 | V |
| Supply Current 1 | $I_{DD1}$ | CE = 3.3V | - | 3.0 | 6.0 | mA |
| Supply Current 2 | $I_{DD2}$ | CE = 0V | - | - | 5.0 | μA |
| CE "High" Voltage | $V_{CEH}$ | | 2.7 | - | - | V |
| CE "Low" Voltage | $V_{CEL}$ | | - | - | 0.45 | V |
| CE Pull down Resistance 1 | Rp1 | CE = 3.3V | 0.5 | 1.5 | 2.5 | MΩ |
| CE Pull down Resistance 2 | Rp2 | CE = 0.3V | 20.0 | 50.0 | 80.0 | KΩ |

### ●Electrical Characteristics (AC)

fCLKin=16.9344MHz, Multiplier/Divider Ratio=1.594, Ta=25°C, CL=15pF

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output Rise Time | $T_{TLH}$ | $V_{DD}$=3.3V(20% to 80%)*2 | - | 5.0 | - | ns |
| Output Fall Time | $T_{THL}$ | $V_{DD}$=3.3V(20% to 80%)*2 | - | 5.0 | - | ns |
| Duty Ratio | DUTY | | 40 | 50 | 60 | % |
| Output Start Time | Ton | *2 | - | - | 20 | ms |
| PLL Output Jitter | Tj | 1σ *2 | - | 40 | - | ps |

*2 R&D guarantee

## ■ Frequency Configuration : Example 2

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Input Frequency | f CLKin | 52.0000 | - | 78.0000 | kHz |
| Multiplier/Divider Ratio | N/M | - | 256.000 | - | - |
| PLL Output Frequency | $fQ_0$ | 13.312 | - | 19.968 | MHz |
| Q1 Output Frequency | $Q_1$ | GND | | | - |



●Electrical Characteristics (DC)

fCLKin=78kHz, Multiplier/Divider Ratio=256, Ta=25°C, No Load

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.97 | 3.3 | 3.63 | V |
| Input Voltage "High" | $V_{IH}$ | | 2.7 | - | - | V |
| Input Voltage "Low" | $V_{IL}$ | | - | - | 0.6 | V |
| Input Current "High" | $I_{IH}$ | $V_{CK}$=3.3V | - | - | 3.0 | μA |
| Input Current "Low" | $I_{IL}$ | $V_{CK}$=0V | - 3.0 | - | - | μA |
| Output Voltage "High" | $V_{OH}$ | $V_{DD}$=2.97V,$I_{OH}$= - 8mA | 2.5 | - | - | V |
| Output Voltage "Low" | $V_{OL}$ | $V_{DD}$=2.97V,$I_{OL}$=8mA | - | - | 0.4 | V |
| Supply Current 1 | $I_{DD1}$ | CE=3.3V | - | 2.0 | 4.0 | mA |
| Supply Current 2 | $I_{DD2}$ | CE=0V | - | - | 5.0 | μA |
| CE "High" Voltage | $V_{CEH}$ | | 2.7 | - | - | V |
| CE "Low" Voltage | $V_{CEL}$ | | - | - | 0.45 | V |
| CE Pull down Resistance 1 | Rp1 | CE=3.3V | 0.5 | 1.5 | 2.5 | MΩ |
| CE Pull down Resistance 2 | Rp2 | CE=0.3V | 20.0 | 50.0 | 80.0 | KΩ |

●Electrical Characteristics (AC)

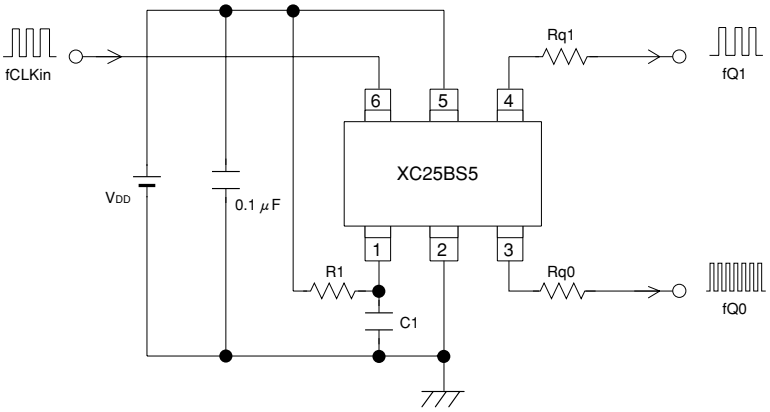
fCLKin=78KHz, Multiplier/Divider Ratio=256, Ta=25°C, CL=15pF

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| Output Rise Time | $T_{TLH}$ | $V_{DD}$=3.3V(20% to 80%)*2 | - | 5.0 | - | ns |
| Output Fall Time | $T_{THL}$ | $V_{DD}$=3.3V(20% to 80%)*2 | - | 5.0 | - | ns |
| Duty Ratio | DUTY | | 40 | 50 | 60 | % |
| Output Start Time | Ton | *2 | - | - | 20 | ms |
| PLL Output Jitter | Tj | 1σ *2 | - | 20 | - | ps |

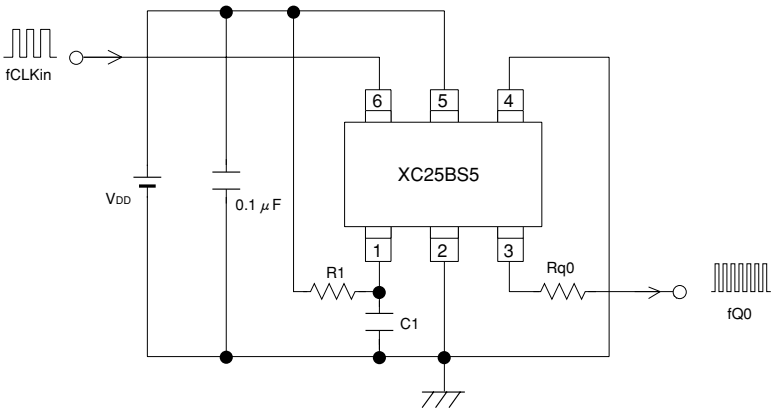
*2 R&D guarantee

## ■Typical Application Circuits

① Q1 Pin - reference oscillation, reference oscillation/2, comparative frequency.




② Q1 Pin - GND

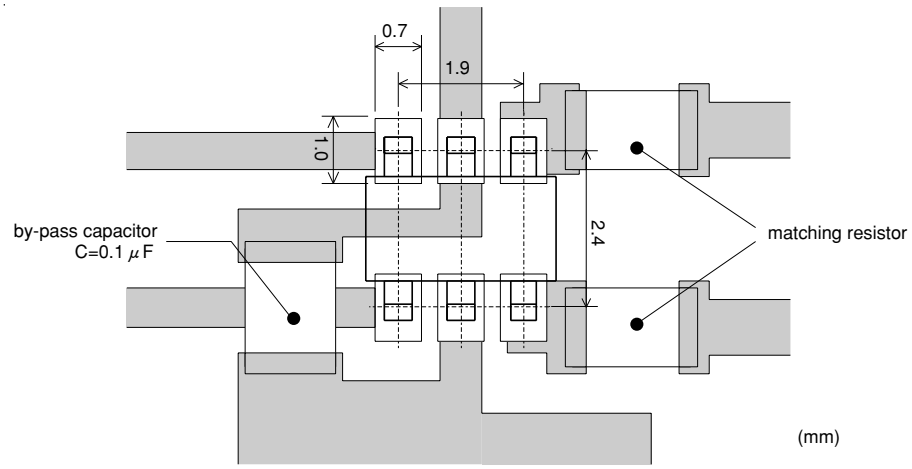



## ■Note:

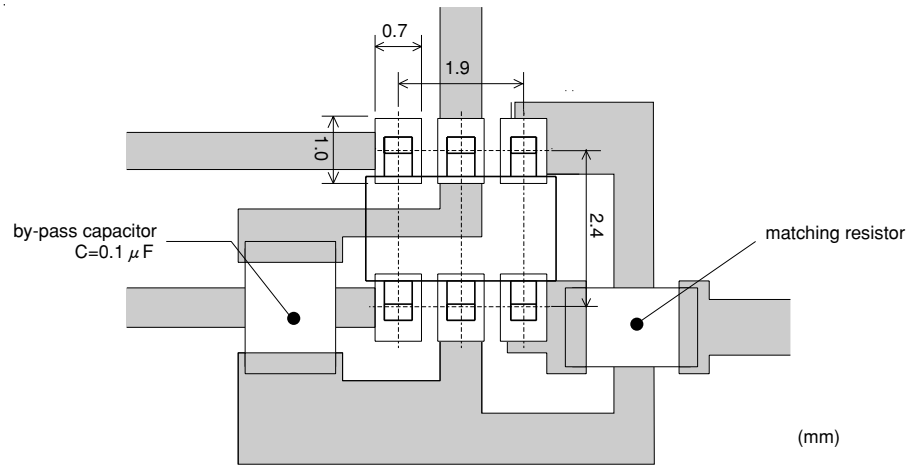
(1) Please insert a by-pass capacitor of 0.1μF.
(2) Rq0 and Rq1 are matching resistors. Their use is recommended in order to counter unwanted radiations.
(3) Please place a by-pass capacitor and matching resistors as close to the IC as possible. It may be that the output cannot be locked if the by-pass capacitor is not close enough to the IC. Further, there is a possibility of unwanted radiation occurance between the resistor and the IC pin if the matching resistor is not close enough to the IC.
(4) When selecting GND for the Q1 pin, although the output of Q1 pin is GND level, it is also recommended that the Q1 pin is connected to GND pattern on the PCB.
(5) When the CE pin is not controlled by external signals, it is recommended that a time constant circuit of R1=1kΩ × C0.1μF be added for stability.
(6) With this IC, output is achieved by dividing and multiplying the reference oscillation by means of the PLL circuit. In cases where this output is further used as a reference oscillation of another PLL circuit, it may be that the final output signal's jitter increases, so all necessary precautions should be taken to avoid this.
(7) It is recommended that a low noise power supply, such as a series regulator, be used for the supply voltage. Using a power supply such as a switching regulator might lead to a larger jitter which in turn may lead to an inability to lock due to the ripple of the switching regulator.

## ■Reference Land Pattern

① Q1 Pin - reference oscillation, reference oscillation/2, comparative frequency.

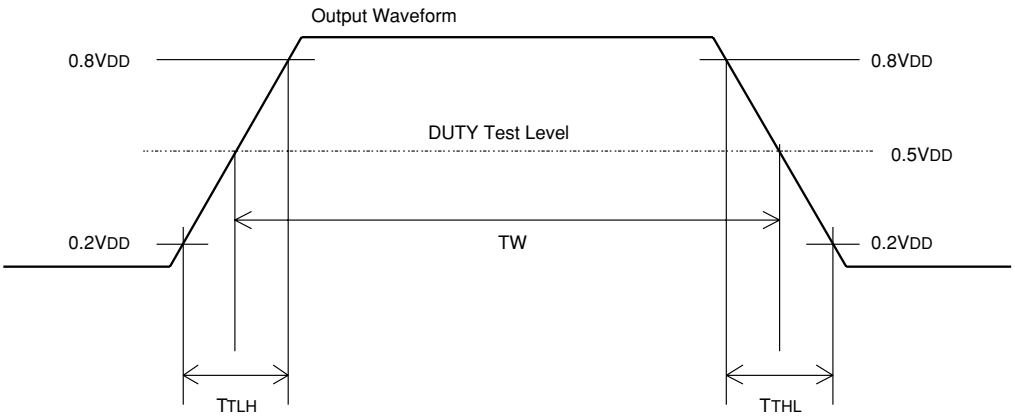



② Q1 Pin - GND

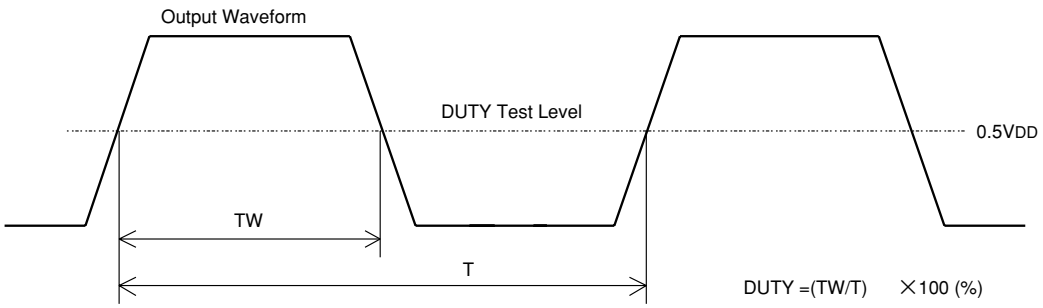


## ■AC Characteristic Waveforms

1) Output Rise Time / Output Fall Time




2) Duty Ratio




3) Output Start Time