LapCoder™ UR5HCFJ8
Low-Power Keyboard Encoder for Portable Systems

HID & SYSTEM MANAGEMENT PRODUCTS, KEYCODER™ FAMILY

DESCRIPTION

The LapCoder™ is a versatile, low-power keyboard encoder for portable systems. The UR5HCFJ8 provides two bi-directional channels for communication with a BIOS-compatible system as well as any optional keyboard-compatible devices, such as a 101/102 desktop keyboard.

The UR5HCFJ8 fully supports the IBM standard keyboard communication protocol; each key press generates one of the scan codes designated in the IBM Technical Reference Manuals. The keyboard encoder handles the scanning, debounce, and encoding of 82 keys organized on an 8x16 matrix and supports embedded numeric keypad functions as well as alternate scan codes for specific keys, so that a keyboard with only 82 keys is able to emulate the functionality of a 101/102 keyboard.

In addition to the system's keyboard communication port the UR5HCFJ8 provides a fully functional keyboard input port that can be used by a standard 82/101/102 keyboard or another 8042-compatible device, such as an external numeric keypad, an OCR, or a bar-code reader. Input from both the matrix and the external device is multiplexed and presented to the system as if it were coming from a single source.

The features of UR5HCFJ8 make it ideal for use in PC/AT/PS/2 laptop/notebook designs that utilize the Fujitsu FKB7211 low-profile, full-travel membrane keyboard.

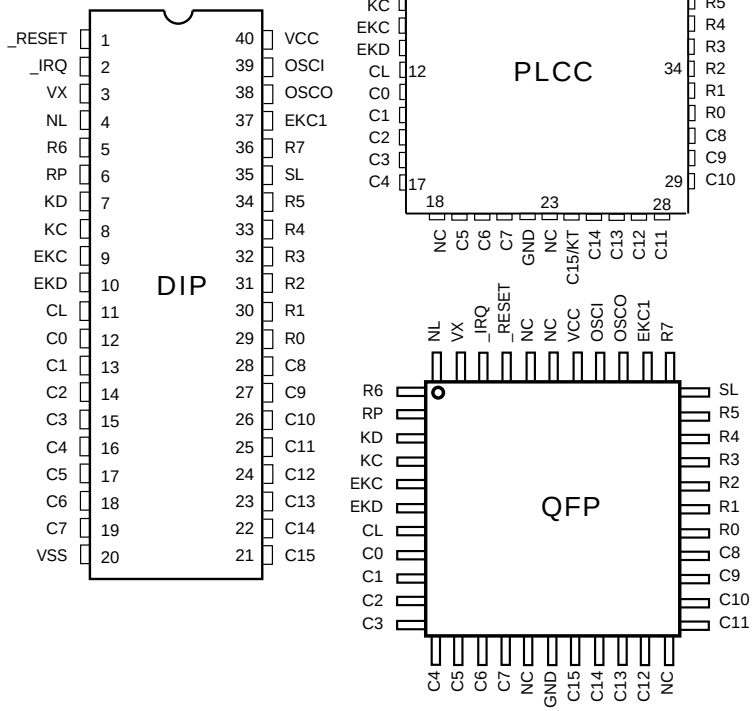
FEATURES

- Interfaces the Fujitsu FKB7211 or other similar laptop/notebook keyboards to a BIOS-compatible systems
- AT / PS/2-compatible
- Interfaces an external keyboard / keypad or other 8042-compatible devices
- Low-power, single IC suitable for 3V battery-operated systems
- Implements all functions of an 101/102 keyboard with only 82-keys
- Available in DIP, PLCC and Quad Flat packages
- Custom versions available in small or large quantities

APPLICATIONS

- Laptop/Notebook
- Portable Equipment
- Industrial Keyboards
- POS Terminals
- Public Information Kiosks

PIN DESCRIPTIONS

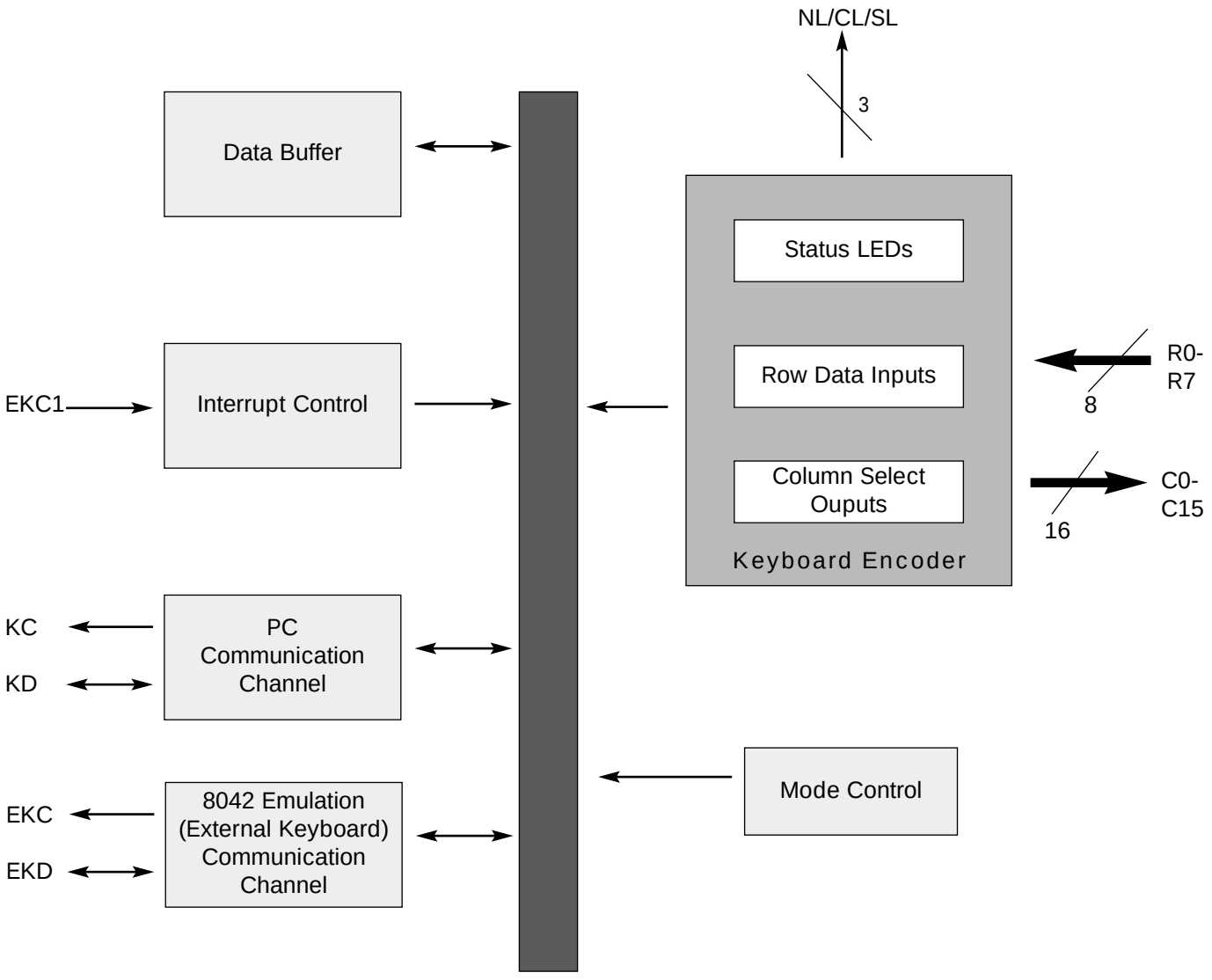


LapCoder is a trademark of Semtech Corp. All other trademarks belong to their respective companies.

ORDERING CODE

Package options	Pitch In mm's	TA = -40°C to +85°C
40-pin Plastic DIP	2 54 mm	UR5HCFJ8-P
44-pin, Plastic PLCC	1.27 mm	UR5HCFJ8-FN
44-pin, Plastic QFP	0.8 mm	UR5HCFJ8-FB

FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

The UR5HCFJ8 consists functionally of six major sections (see Functional Diagram, previous page). These are the Keyboard Encoder, the Mode Control Unit, the PC Communication Channel, the Data Buffer, the Interrupt Control and the 8042 Emulation Channel. All sections communicate with each other and operate concurrently.

KEYBOARD ENCODER

The controller continuously scans a keyboard organized as an 8 row by 16 column matrix for a maximum of 128 keys. Smaller-size keyboards are supported provided that all unused row lines are pulled to Vcc.

The IC selects 1 of the 16 column lines (C0-C15) every 512 mS and then reads the row data lines (R0-R7). A key closure is detected as a 0 in the corresponding position of the matrix. A complete scan cycle for the entire keyboard takes approximately 9.2 mS. Each key found pressed is debounced for a period of 20 mS. Once the key is verified, the corresponding key code(s) are loaded into the transmit buffer of the PC Communication Channel.

Switch Matrix Encoding

Each matrix location is programmed to represent either a single key or a key combination of the IBM 101/102 standard keyboard.

Scan Code Table Sets

The UR5HCFJ8 supports all three scan code table sets. Scan Code Sets 1 and 2 are the default sets for AT/PS/2 systems. Scan Code Table Set 3 allows the user to program individual key attributes such as Make/Break and Typematic or Single-Touch Action. For more information, refer to the IBM Technical Reference Manuals.

PIN DEFINITIONS

Mnemonic	DIP	PLCC	QFP	Type	Name and Function
VCC	40	44	38	I	Power Supply: +5V
VSS	20	22	17	I	Ground
OSCI	39	43	37	I	Oscillator input
OSCO	38	42	36	O	Oscillator output
_RESET	1	1	41	I	Reset: Apply 0V to provide orderly start-up
EKC1	37	41	35		External Keyboard Clock 1: Connects to external keyboard Clock Line and is used to generate an interupt for every Clock Line transition.
VX	3	4	43	I	Tie to Vcc
VXA		3		I	Tie to Vcc
RP	6	7	2	I	Reserved: Ties to Vcc
KC	8	9	4	I/O	Keyboard Clock: Connects to PC keyboard port clock line
KD	7	8	3	I/O	Keyboard Data: Connects to PC port data line
EKD	10	11	6	I/O	External Keyboard Data: Connects to external keyboard Data Lne
ECK	9	10	5	I/O	External Keyboard Clock: Connects to external keyboard Clock Line
_IQR	2	2	42	I	Interrupt Line: Reserved for low-power applications
R0-R5	29-34	32-37	27-32	I	Row Data Inputs
R6	5	6	1	I	
R7	36	39	34	I	
C0-C7	12-19	13-17	8-15	O	Column Select Outputs: Selects 1 of 16 columns
		19-21		O	
C8-C15	28-21	31-24	26-23	O	
			21-18	O	
CL	11	12	7	O	Caps Lock LED
NL	4	5	44	O	Num Lock LED
SL	35	38	33	O	Scroll Lock LED
NC		18	16,22		No Connects: These pins are unused.
		23,40	39,40		

Note: An underscore before a pin mnemonic denotes an active low signal.

Copyright Semtech, 1997-2001

KEYBOARD ENCODER, (CON'T)

Embedded Numeric Keypad

The UR5HCFJ8 implements an embedded numeric keypad. The Numeric Keypad Function is invoked by pressing the Num Lock Key.

FN Key

A special FN Key has been implemented to perform the following functions while it is held pressed:

- Function Key F1 becomes F11
- Function Key F2 becomes F12
- Ctrl Left Key becomes Ctrl Right
- Alt Left Key becomes Alt Right

If Num Lock is set:

- Embedded numeric keypad keys become regular keys.

If Num Lock is not set:

- Embedded numeric keypad keys provide the same codes as a numeric keypad when the Num Lock is not set (Arrow Keys, PgUp, PgDn, etc.)

Status LED indicators

The controller provides interfacing for three LED shift status indicators. All three pins are active low to indicate the status of the host system (Num Lock, Caps Lock and Scroll Lock). They are set by the system (AT/PS/2 protocol).

MODE CONTROL

Operating modes are defined by the logic level of the mode pin in the Mode Control Unit.

N-Key Rollover

In this mode, the code(s) corresponding to each key press are transmitted to the host system as soon as that key is debounced, independently of the release of other keys. If a key is defined to be Typematic, the corresponding code(s) will be transmitted while that key is held pressed. When the key is released, the corresponding break code(s) are then transmitted to the host system. If the released key happens to be the most recently pressed, then Typematic Action is terminated. There is no limitation to the number of keys that can be held pressed at the same time. However, two or more key closures, occurring within a time interval of less than 5 mS, will set an error flag and will not be processed. This procedure protects against the effects of accidental key presses.

"Ghost" Keys

In any scanned contact switch matrix, whenever three keys defining a rectangle on the switch matrix are held pressed at the same time, a fourth key positioned on the fourth corner of the rectangle is sensed as being pressed. This is known as the "ghost" or "phantom" key problem. Although the problem cannot be totally eliminated without using external hardware, there are methods to neutralize its negative effects for most practical applications. Keys that are intended to be used in combinations or are likely to be pressed at the same time by a fast typist (i.e., keys located in adjacent positions on the keyboard) should be placed in the same row or column of the matrix, whenever possible. Shift keys (Shift, Alt, Ctrl) should not reside in the same row (or column) with any other keys.

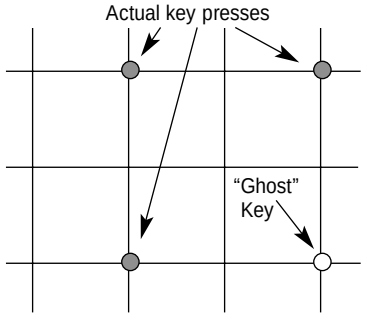


Figure 1: "Ghost" or "Phantom" Key Problem

The UR5HCFJ8 has built-in mechanisms to detect the presence of "ghost" keys, thus eliminating the necessity of external hardware.

Copyright Semtech, 1997-2001

SPECIAL HANDLING

Hot Plug-Ins of External Device

The UR5HCFJ8 will detect the presence of an external device. If an external keyboard or other device was not connected during power-on and is connected at a later time, the encoder will proceed with the normal reset routine in order to properly initialize the external keyboard. After communication has been established, the encoder will continue to check for the presence of the external keyboard. While the external device is connected, the encoder will not enter the sleep mode. If the device is disconnected at a later time, the encoder will become aware of it. If a subsequent connection takes place, the controller will reinitiate a reset sequence. This unique feature allows the user to connect or disconnect an external device at any time without having to reset the system.

Shift Status LEDs

Shift Status LEDs (Num Lock, Caps Lock and Scroll Lock) indicate the status of the system and are controlled by commands sent from the system. Set/Reset Status Indicator commands from the system will be executed both by the external keyboard and the scanned matrix. For example, if the user presses the Caps Lock Key on either keyboard, the Caps Lock LED will be affected in both keyboards. The LED status indicators are properly set after every new connection of an external keyboard.

PC COMMUNICATION

The UR5HCFJ8 implements all the standard functions of communication with a BIOS-compatible PC/XT or AT/PS/2 host system. Two lines, KC and KD, provide bi-directional clock and data signals. In addition, the UR5HCFJ8 supports all commands from and to the system, as described in the IBM Technical Reference Manuals.

The following table shows the commands that the system may send and their values in hex.

Command	Hex Value
Set/Reset Status Indicators	ED
Echo	EE
Invalid Command	EF
Select Alternate Scan Codes	F0
Invalid Command	F1
Read ID	F2
Set Typematic Rate/Delay	F3
Enable	F4
Default Disable	F5
Set Default	F6
Set All Keys	
■ Typematic	F7
■ Make/Break	F8
■ Make	F9
■ Typematic/Make/Break	FA
Set Key Type	
■ Typematic	FB
■ Make/Break	FC
■ Make	FD
Resend	FE
Reset	FF

Table 2: Keyboard Commands from the System (AT/PS/2 protocol)

These commands are supported in the AT/PS/2 protocol and can be sent to the keyboard at any time.The following table shows the commands that the keyboard may send to the system.

Command	Hex Value
Key Detection Error/Overrun	00*
Keyboard ID	83AB
BAT Completion Code	AA
BAT Failure Code	FC
Echo	EE
Acknowledge (Ack)	FA
Resend	FE
Key Detection Error/Overrun	FF**

*Code Sets 2 and 3
**Code Set 1

Table 3: Keyboard Commands to the System (AT/PS/2 protocol)

8042 Emulation Channel

The UR5HCFJ8 fully emulates a system's keyboard port, available to a standard 82/101/102 external keyboard or other 8042-compatible device. Communication with a keyboard-compatible device is accomplished by clock and data lines via EKC and EKD pins, respectively. A third pin, EKC1, connects to the Clock Line and interrupts the controller whenever the external device initiates a communication session. When power is first applied, the controller proceeds with the standard reset sequence with the external device. Data and commands initiated from the external device are buffered in the controller's FIFO along with data from the scanned matrix, and then are presented to the system as if they were coming from a single source. After they are acknowledged, commands and data from the system are transmitted to the external device.

Copyright Semtech, 1997-2001

KEY MAP FOR FKB7211 (UR5HCFJ8)

Columns (C0–C13)

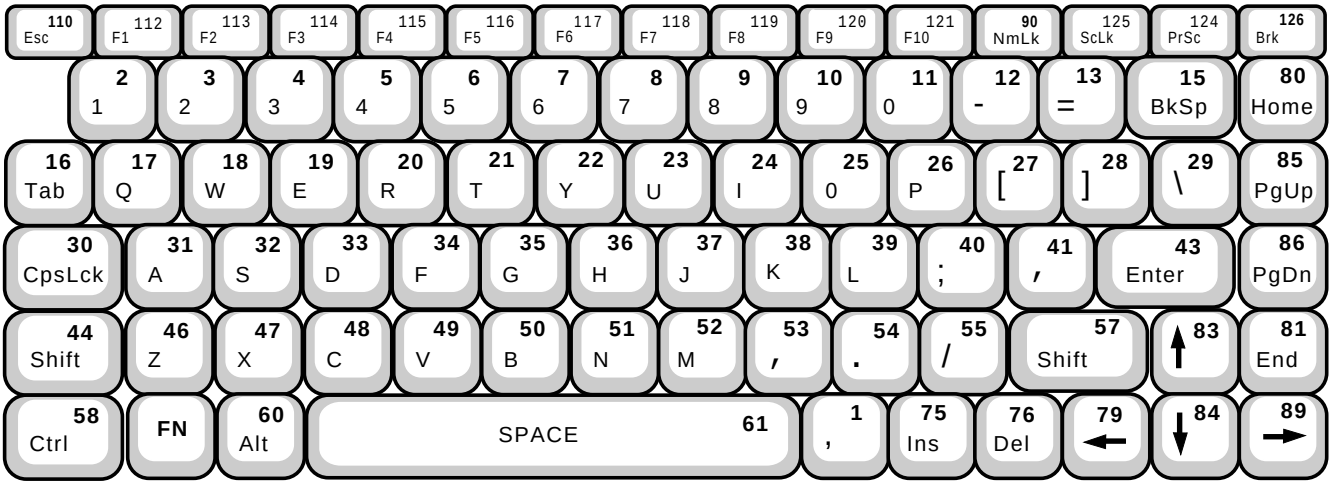
Rows (R0–R7)

0	1	2	3	4	5	6	7	8	9	10	11	12	13
LCtrl*	Esc	Tab	Fn	LAlt*	Space		` (BkQt)	Insert	Delete	ArrLft	ArrDn	LShift	ArrRt
	F1*	Z			X	C		. (per) Pad .	/ Pad /		ArrUp	RShift	End
	1	CapLk			V	B	N	M Pad 0	, (com)	, (appos)	Enter		PgDn
	F2	A			S	D	F	J Pad 1	K Pad 2	L Pad 3	; Pad +		PgUp
	2	3			4	T	Y	U Pad 4	I Pad 5	O Pad 6	P Pad -		BkSpc
	F4	F5			F6	F7	F8	F9	F10	NumLk	ScrLk		PrtScr
	F3	% 5			6	7 Pad 7	8 Pad 8	9 Pad 9	0 Pad *	- (dash)	=		Pause
	Q	W			E	R	G	H	[	]	\		Home

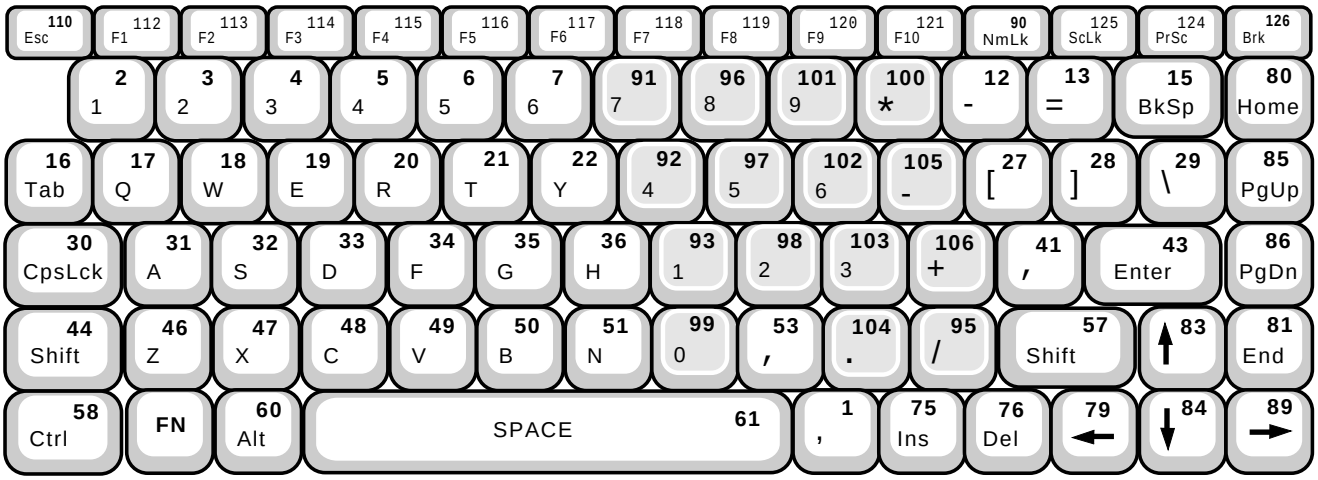
KEYBOARD LAYOUTS (US ENGLISH)

Depending on the status of the Num Lock and the FN Key, the UR5HCFJ8 implements one of four keyboard layouts. (Key numbering of a standard 101/102 keyboard is shown.)

Layout A (Default layout)



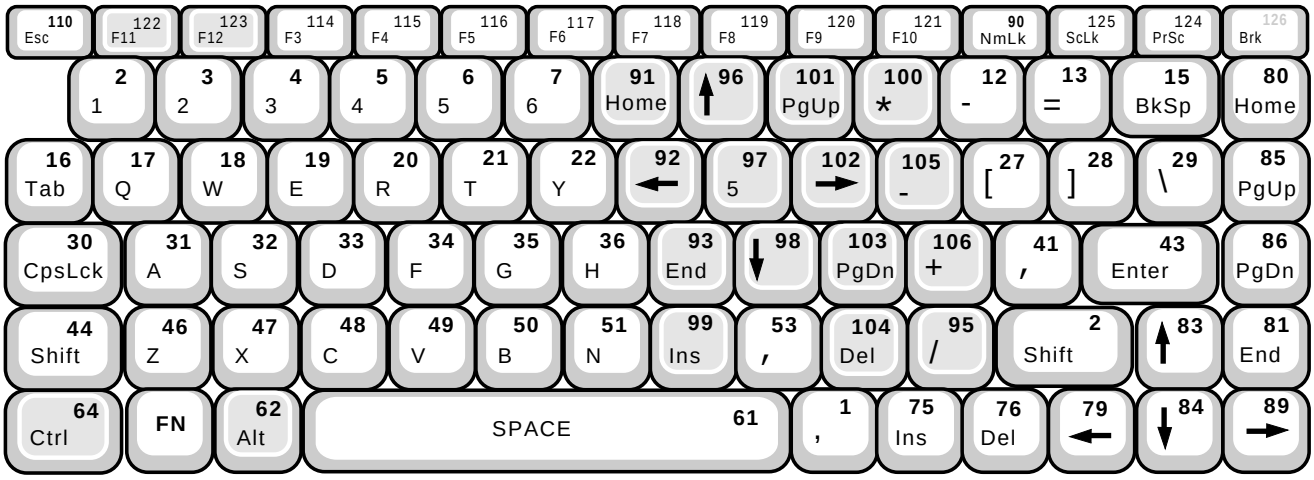
Layout B (Num Lock is set)



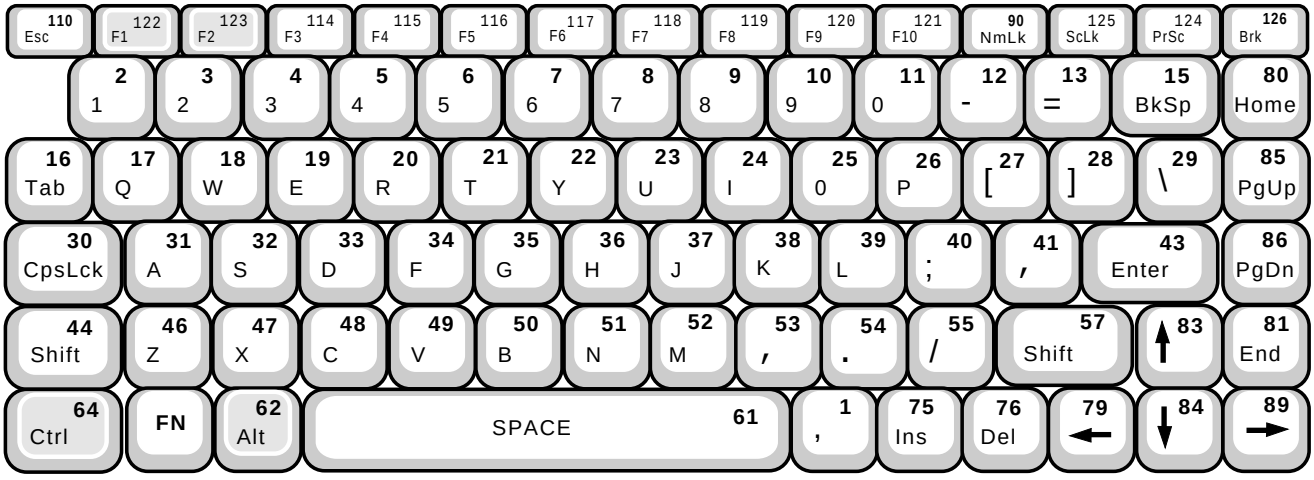
KEYBOARD LAYOUTS (US ENGLISH)

Depending on the status of the Num Lock and the FN Key, the LapCoder™ implements one of four keyboard layouts. (Key numbering of a standard 101/102 keyboard is shown.)

Layout C (FN key pressed)



Layout D (Num Lock set and FN key pressed)



IMPLEMENTATION NOTES FOR THE UR5HCFJ8

The following notes pertain to the suggested schematics found on the next pages.

The Built-in Oscillator on the UR5HCFJ8 requires the attachment of the 4.00 MHz Ceramic Resonators with built-in Load Capacitors.. You can use either an AVX, part number PBRC-1.00 BR; or a Murata part number CSTCC4.00MG ceramic resonator.

It may also be possible to operate with the 4.00 MHz Crystal, albeit with reduced performance. Due to their high Q, the Crystal oscillator circuits start-up slowly. Since the LapCoder™ constantly switches the clock on and off, it is important that the Ceramic Resonator is used (it starts up much quicker than the Crystal). Resonators are also less expensive than Crystals.

Also, if Crystal is attached, two Load Capacitors (33pF to 47pF) should be added, a Capacitor between each side of the Crystal and ground.

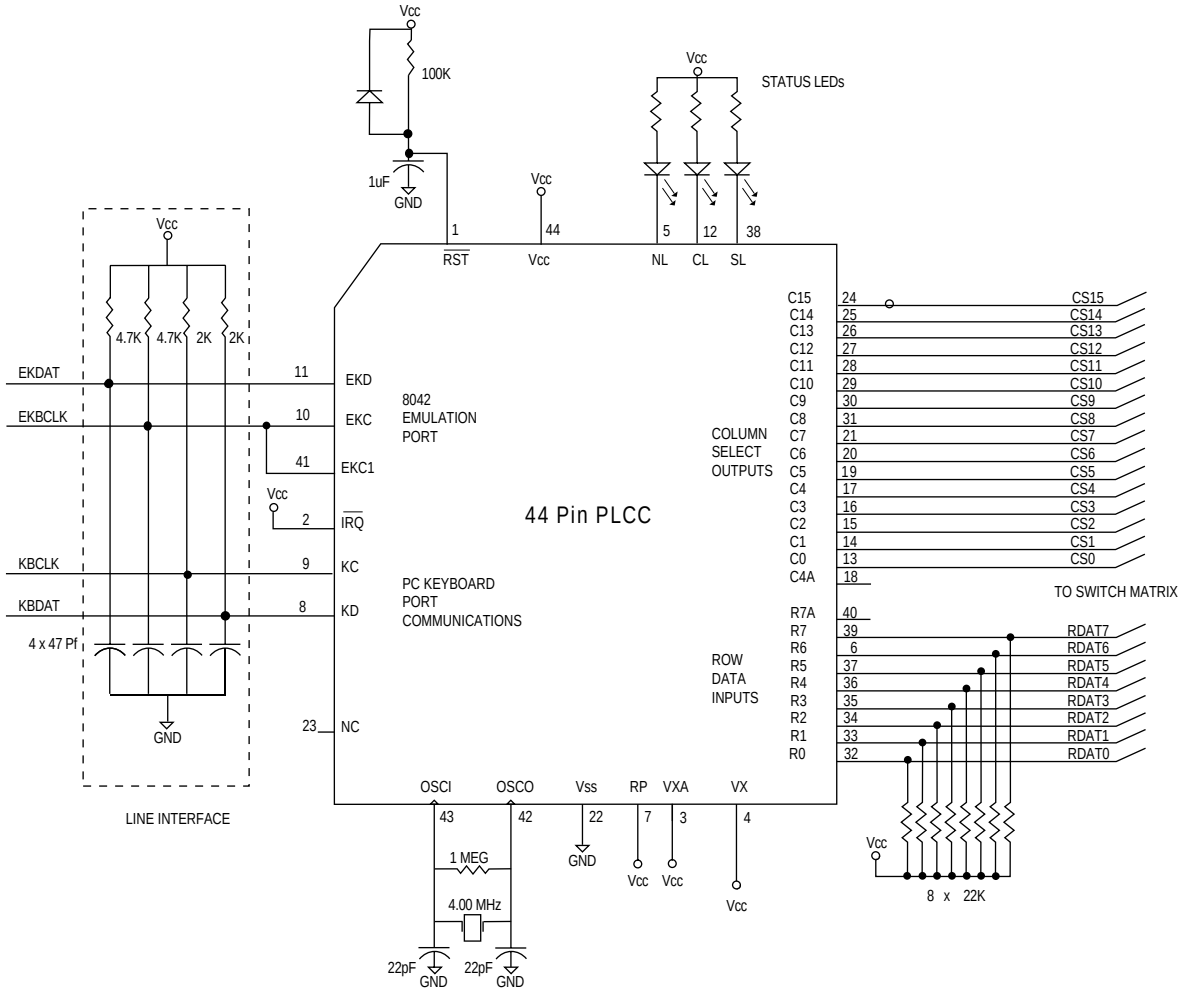
In both cases, using Ceramic Resonator with built-in Load Capacitors, or Crystal with external Load Capacitors, a feedback Resistor of 1 Meg should be connected between OSCin and OSCout.

Troubleshoot the circuit by looking at the Output pin of the Oscillator. If the voltage it half-way between Supply and Ground (while the Oscillator should be running) --- the problem is with the Load Caps / Crystal. If the voltage it all the way at Supply or Ground (while the Oscillator should be running) --- there are shorts on the PCB.

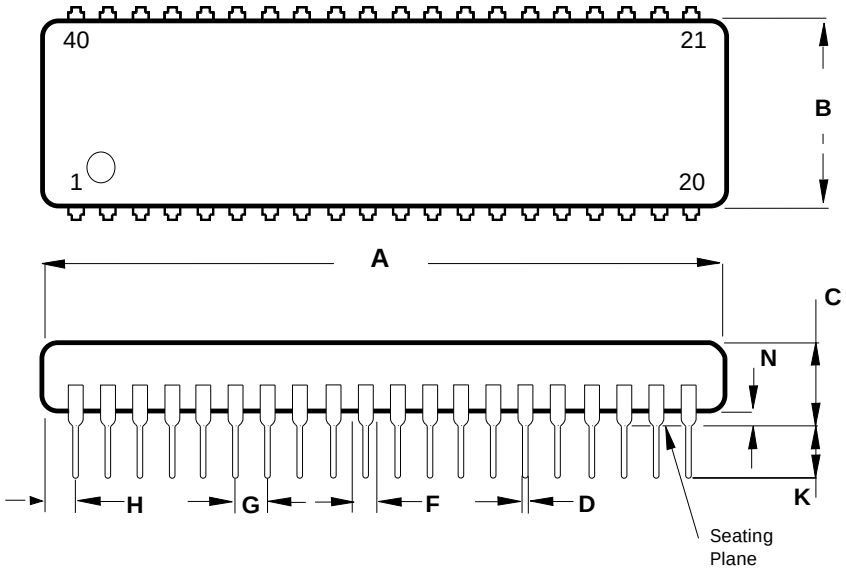
NOTE: when the Oscillator is intentionally turned OFF, the voltage on the Output pin of the Oscillator is High (at the Supply rail).

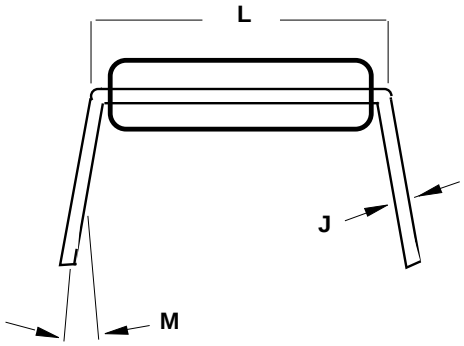
Copyright Semtech, 1997-2001

SUGGESTED INTERFACING FOR THE LAPCODER™ UR5HCFJ8



MECHANICALS FOR THE UR5HCFJ8-P



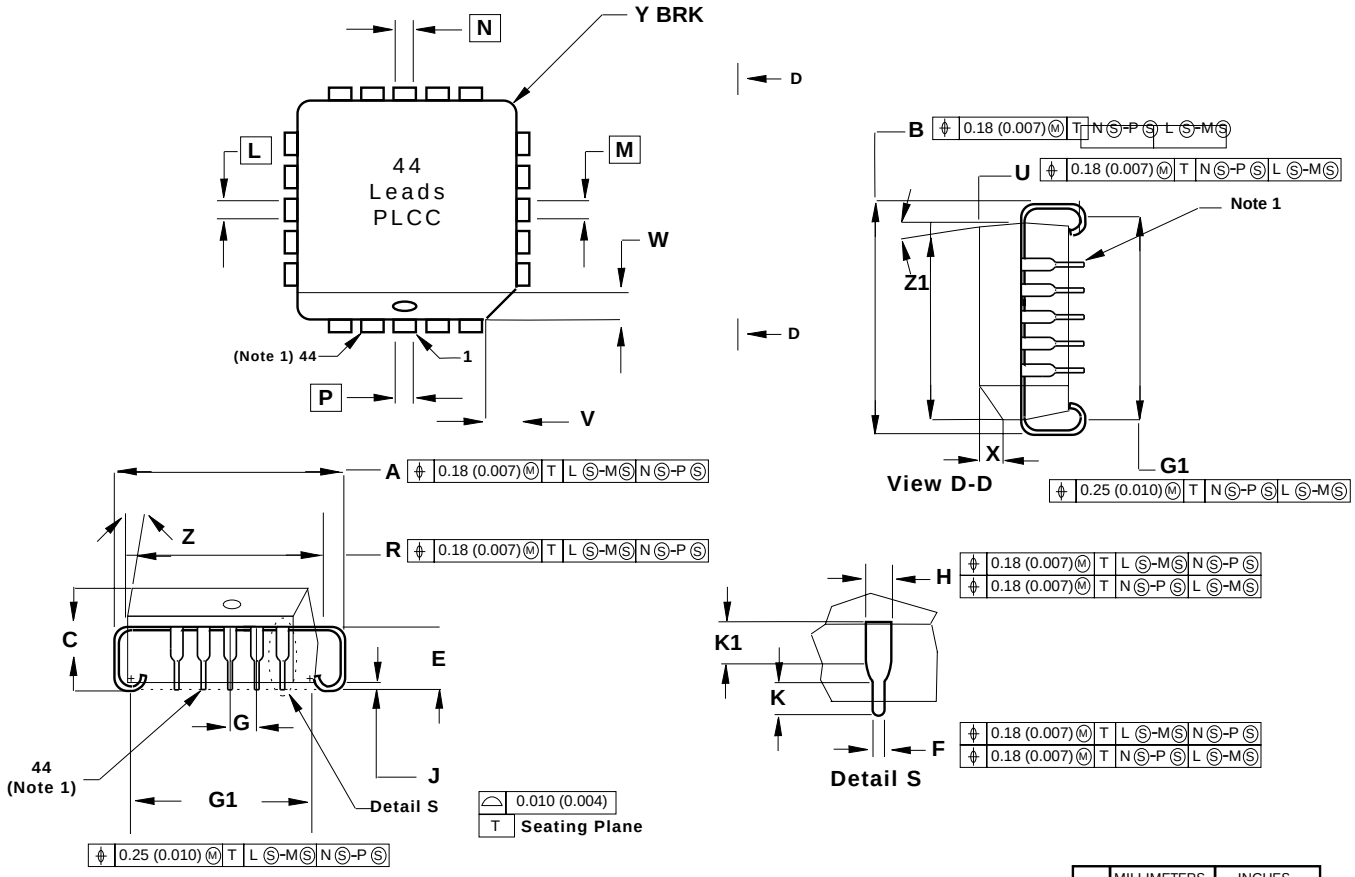


Notes:
1. Positional tolerance of leads (D) shall be within 0.25 mm (0.010) at maximum material condition, in relation to the seating plane and each other.
2. Diminsion L is to the center of the leads when the leads are formed parallel.
3. Dimension B does not include mold flash.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.015	0.135
L	15.24 BSC		0.600 BSC	
M	0^{0}	15^{0}	0^{0}	15^{0}
N	0.51	1.02	0.020	0.040

Copyright Semtech, 1997-2001

MECHANICALS FOR THE UR5HCFJ8-FN

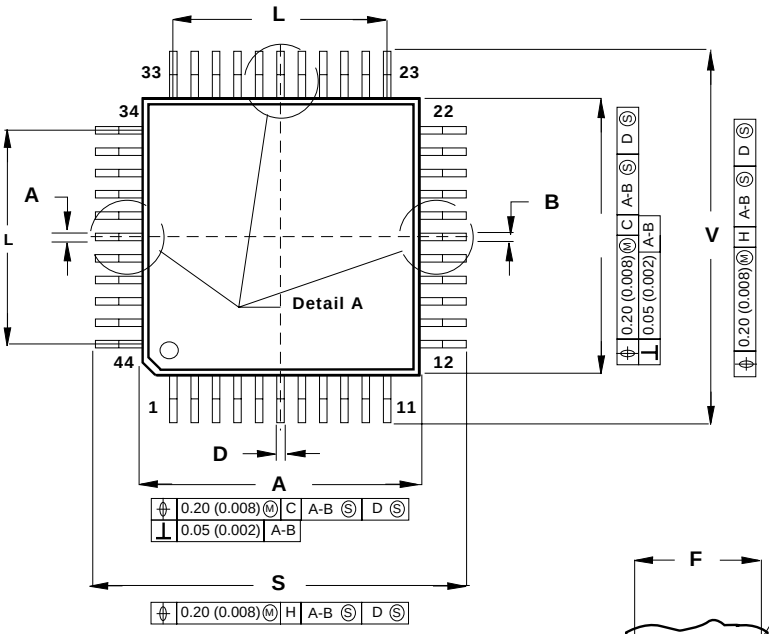


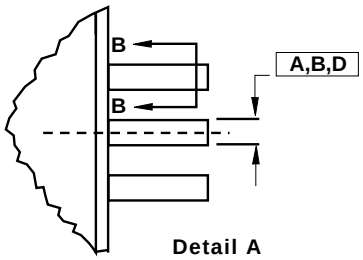
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	-	0.020	-
K	0.64	-	0.025	-
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	-	0.50	-	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	-	0.040	-
Z1	2°	10°	2	10°

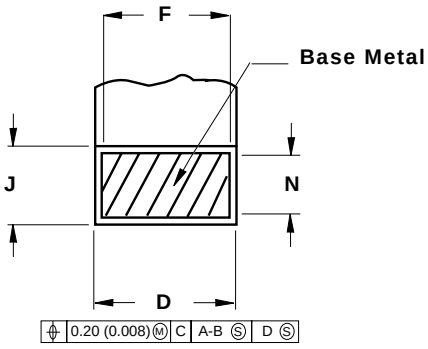
Notes:
1. Due to space limitation, the chip is represented by a general (smaller) case outline drawing rather than showing all 44 leads.
2. Datums L, M, N, and P determine where the top of the lead shoulder exits plastic body at mold parting line
3. DIM G1, true position to be measured at Datum T, Seating Plane
4. DIM R and U do not include mold protusion. Allowable mold protusion is 0.25 (0.010) per side.
5. Dimensioning and tolerancing per Ansi Y14.5M, 1982
6. Controlling dimension: Inch

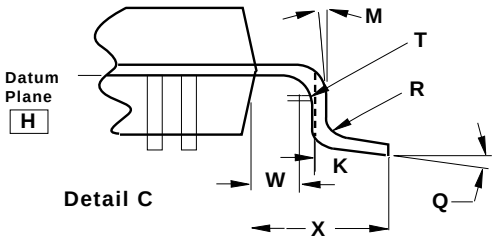
Copyright Semtech, 1997-2001

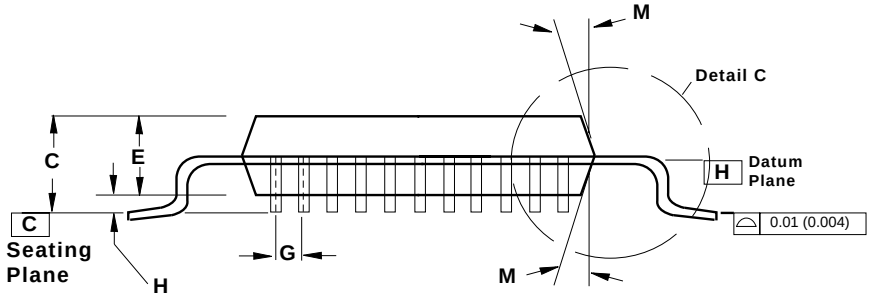
MECHANICALS FOR THE UR5HCFJ8-FB











Notes

1. Dimensioning and tolerancing per Ansi Y14.5-M, 1982
2. Controlling dimension: Millimeter
3. Datum Plane "H" is located at the bottom of the lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums -A-, -B-, and -D- to be determined at Datum Plane -H-.
5. Dimensions S and V to be determined at seating plane -C-.
6. Dimensions A and B do not include Mold protusion. Allowable protusion is 0.25 (0.010) per side. Dimensions A and B do include mold mismatch and are determined at Datum Plane -H-.
7. Dimension D does not include Danbar protrusion. Allowable Danbar protrusion is 0.08 (0.003) total in excess of the D dimension at Maximum Material Condition. Danbar cannot be located on the lower radius or the foot.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	-	0.25	-	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5 °	10 °	5 °	10 °
N	0.13	0.17	0.005	0.007
Q	0 °	7 °	0 °	7 °
R	0.13	.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	-	0.005	-
U	0 °	-	0 °	-
V	12.95	13.45	0.510	0.530
W	0.40	-	0.016	-
X	1.6 REF		0.063 REF	

Copyright Semtech, 1997-2001

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Ratings	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	Vss -0.3 to V_{DD} +0.3	V
Current Drain per Pin (not including Vss or Vdd)	I	25	mA
Operating Temperature UR5HCFJ8-XX	TA	T low to T high -40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance	T_{JA}		°C per W
■ Plastic DIP		60	
■ Plastic PLCC		70	

DC Electrical Characteristics (V_{DD}=5.0 V_{DC} +/-10%, V_{SS}=0 V_{DC}, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I load<10µA)	V_{OL}			0.1	V
	V_{OH}	V_{DD}–0.1			
Output High Voltage (I load=0.8mA)	V_{OH}	V_{DD}–0.8			V
Output Low Voltage (I load=1.6mA)	V_{OL}			0.4	V
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V
Input Low Voltage	V_{IL}	Vss		0.2xV_{DD}	V
User Mode Current	I_{PP}		5	10	mA
Data Retention Mode (0 to 70°C)	V_{RM}	2.0			V
Supply Current* (Run)	I_{DD}		4.7	7.0	mA
I/O Ports Hi-Z Leakage Current	I_{IL}			+/-10	µA
Input Current	I_{IN}			+/- 1	µA
I/O Port Capacitance	C_{IO}		8	12	pF

*In a typical application circuit, including external A/D.

Control Timing (V_{DD}=5.0 V_{DC} +/-10%, V_{SS}=0 V_{DC}, Temperature range=T low to T high unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation	f_{OSC}			MHz
■ Crystal Option			2.0	
■ External Clock Option		dc	2.0	
Crystal Oscillator Startup Time	f_{OP}			MHz
■Crystal (f_{OSC}/2)			2.0	
■External Clock Option		dc	2.0	
Cycle Time	t_{CYC}	1000		ns
Crystal Oscillator Startup Time	toxov		100	ms
Stop Recovery Startup Time	t_{ILCH}		100	ms
Reset Pulse Width	t_{RL}	8		tcyc
Interrupt Pulse Width Low	t_{LIH}	125		ns
Interrupt Pulse Period	t_{ILIL}	*		tcyc
OSC1Pulse Width	t_{OH}, t_{OL}	90		ns

*The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 tcyc.

Copyright Semtech, 1997-2001

SEMTECH

UR5HCFJ8 BILL OF MATERIALS FOR PAGE 10 SCHEMATIC

UR7HCFJ8-XX	BOM			
Description	Quantity	Manufacturer	Part#	Description
Bare PCB				
PCB	1		PCB5-FJ8-100	PCB for UR5EVB. Thru Hole
Capacitors:				
C1, C2	2	Generic	Any	.1uF Ceramic disk or Monolythic cap, THD
C3, C4	2	Generic	Any	22pF, Ceramic disk cap, THD
C5, C7	2	Generic	Any	.01uF Ceramic disk cap, THD
C6	1	Generic	Any	10uF, 16V Tantalum Cap, THD
C8, C9, C10, C11	4	Generic	Any	47pF Ceramic disk cap, THD
ICs:				
U1	1	Semtech	UR7HCFJ8	LapCoder™
Connectors:				
J1	1	Molex	39-51-3144	14 pos, ZIF Conn, Straight
J2	1	Molex	39-51-3084	8 pos ZIF Conn, Straight
J5	1	AMP	640456-5	5 positions .1”ST/Header
J6	1	AMP	640456-6	6 positions .1”ST/HeaderJP1, JP2
JP1-JP2	1	AMP	103322-3	Header, 2x3 positions, 1”
E1, E2	2	S.E.	PH1-025-2G	Male Str Header 1x2 pos
Diode:				
D1-D8	8	Generic	Any	Diode, small signal, THD, DO-35
LED:				
J4	3	King Bright	L113GDT	Rect LED, cross to SSL-LX2573GD, THD
Resistors:				
R1, R6, R7	3	Generic	Any	1M Resistor, Carbon Film, THD
R2, R3, R4	3	Generic	Any	330 Ohm Resistor, Carbon Film
R5	1	Generic	Any	1M Resistor, Carbon Film
R8, R9	2	Generic	Any	4.7K Resistor, Carbon Film, THD
R10, R11	2	Generic	Any	2K Resistor, Carbon Film, THD
R12	1	Generic	Any	100K Resistor, Carbon Film, THD
R13-R16	4	Generic	Any	47 Ohm Resistor, Carbon Film, THD
R20	1	Generic	Any	22K Resistor, Carbon Fil, THD
Resistor Net:				
RP1, RP2, RP3	3	CTS	761-3-332G	3.3K, 8 Resistor, 16 pins, THD, DIP
RP4	1	KOA	RKC82223G	22K, 8 Resistor, 9 pins, THD, SIP
Crystal:				
Y1	1	ECS	EC2-040-4.00	4.00MHz Low Profile Crystal, THD
Shunts:				
E1-S, JP1-S, JP2-S	3	Solid Electronics	MJ-254M	Standard Gold 2 Position Jumper
Socket:				
U1_S	1	McKenzie	PLCC44P-T	44PLCC THD Socket

Notes: J3 not installed. Install shunts as follow: JP1, JP2 between pins 2 & 3; also installs in E1

Updated 2000/08/01

Copyright Semtech, 1997-2001

SEMTECH

For sales information and product literature, contact:

HID & System Mgmt Division
Semtech Corporation
568 Broadway
New York, NY 10012
hidinfo@semtech.com
http://www.semtech.com
212 226 2042 Telephone
212 226 3215 Telefax

Semtech Western Regional Sales
805-498-2111 Telephone
805-498-3804 Telefax

Semtech Central Regional Sales
972-437-0380 Telephone
972-437-0381 Telefax

Semtech Eastern Regional Sales
203-964-1766 Telephone
203-964-1755 Telefax

Semtech Asia-Pacific Sales Office
+886-2-2748-3380 Telephone
+886-2-2748-3390 Telefax

Semtech Japan Sales Office
+81-45-948-5925 Telephone
+81-45-948-5930 Telefax

Semtech Korea Sales Sales
+82-2-527-4377 Telephone
+82-2-527-4376 Telefax

Northern European Sales Office
+44 (0)2380-769008 Telephone
+44 (0)2380-768612 Telefax

Southern European Sales Office
+33 (0)1 69-28-22-00 Telephone
+33 (0)1 69-28-12-98 Telefax

Central European Sales Office
+49 (0)8161 140 123 Telephone
+49 (0)8161 140 124 Telefax

Copyright 1997-2001 Semtech Corporation. All rights reserved. KeyCoder, LapCoder, Zero-Power and Self-Power Management are trademarks of Semtech Corporation. Semtech is a registered trademark of Semtech Company. All other trademarks belong to their respective companies.

INTELLECTUAL PROPERTY DISCLAIMER
This specification is provided "as is" with no warranties whatsoever including any warranty of merchantability, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification or sample. A license is hereby granted to reproduce and distribute this specification for internal use only. No other license, expressed or implied to any other intellectual property rights is granted or intended hereby. Authors of this specification disclaim any liability, including liability for infringement of proprietary rights, relating to the implementation of information in this specification. Authors of this specification also do not warrant or represent that such implementation(s) will not infringe such rights.