Applications

- DSL clock source
- Set-top boxes
- Telecom switching
- MPEG Video clock source
- HDTV

General Description

The Vaishali VT83201 is a single-chip, integrated VCXO and Phase Locked Loop (PLL) clock synthesizer. The device uses the VCXO and an analog Phase-Locked Loop (PLL) to accept a 10 MHz to 20 MHz, 30pF (pull range of 200 ppm) crystal input, in order to produce either one or two output clocks. A 0 to 3V control signal is used to fine tune the output clock frequency in the ±100ppm range. Select inputs S0 and S1 are used for frequency and output selection.

Features

- 3.3V supply operation
- Packaged in 16-pin SOIC package
- Replaces separate VCXO and multiplier
- Uses inexpensive pullable crystal
- On-chip VCXO with 200 ppm pull range (±100 ppm)
- 5V-tolerant control inputs
- Zero ppm synthesis error in both clocks

Figure 1. Functional Block Diagram

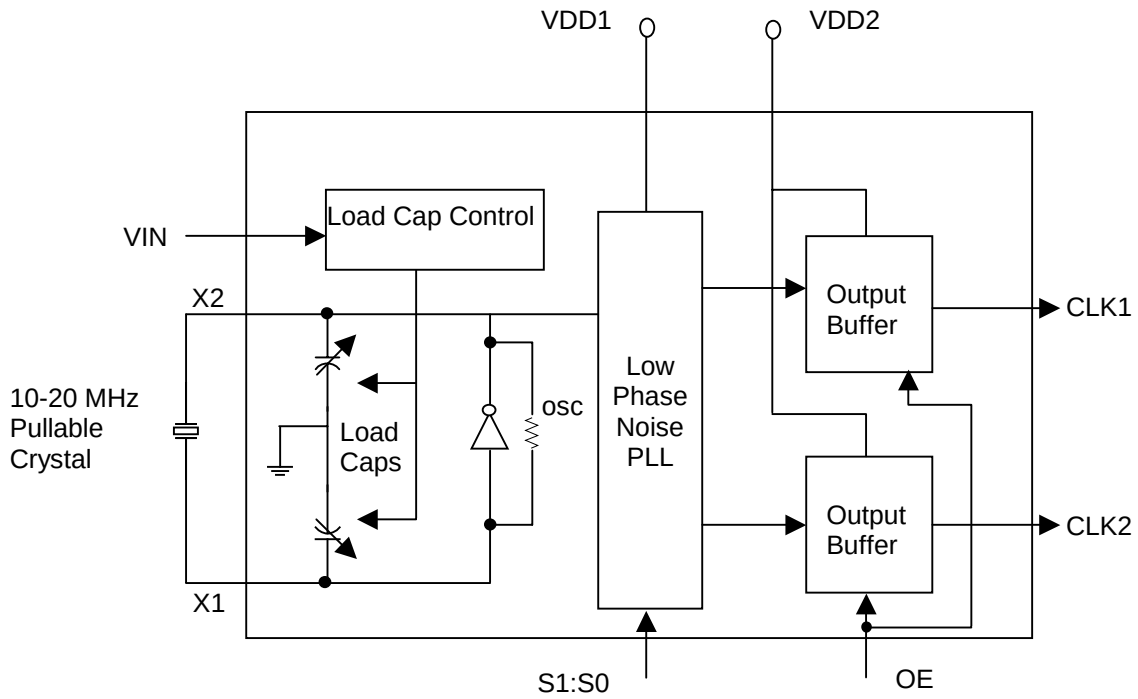

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Figure 2. Pin Configuration

VT83201
16 pin SOIC

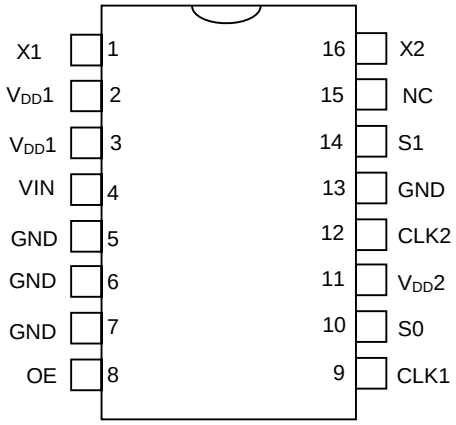


Table 1. Pin Description

Name	Pin #	Type	Description
X1	1	XI	Crystal connection. Connect to a pullable crystal of 10–20 MHz
$V_{DD}1$	2,3	P	Core V_{DD}. Connect to 3.3V
VIN	4	I	Voltage input to VCXO. Zero to 3V signal controls the frequency of the VCXO.
GND	5,6, 7,13	P	Connect to ground.
OE	8	I	Active HIGH Output enable . Outputs in Hi-Z state when LOW
CLK1	9	O	Clock output #1 per Table 2.
S0	10	I	Select input #0. Selects output per Table 2
$V_{DD}2$	11	P	Output V_{DD}. Connect to 3.3V
CLK2	12	O	Clock output #2 per Table 2
S1	14	I	Select input #1. Selects outputs per Table 2
NC	15	-	There is no internal connection to this pin.
X2	16	XO	Crystal connection. Connect to a pullable crystal of 10 MHz – 20 MHz.

Legend: I = Input
O = Output
P = Power supply connection
XI, XO = Crystal connections.

Table 2. Clock Selection Table (OE = High)

S1	S0	CLK1	CLK2
0	0	REF/4	REF/2
0	M[1]	OFF	X 0.666
0	1	OFF	X 2.6666
1	0	OFF	X 4
1	1	OFF	X 1.3333

Note:

1. SO has three valid states: 0 (LOW) = $V_{IN} \leq 0.5V$
1 (HIGH) = $V_{IN} \geq V_{DD} - 0.5$
M (MID) = $0.5V < V_{IN} < V_{DD} - 0.5V$

Table 3. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage, V_{DD}	Referenced to GND			4.6	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4. Operating Conditions

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage, V_{DD}		3.15	3.3	3.45	V
Input High Voltage, V_{IH}, X1 pin only		2.5			V
Input Low Voltage, V_{IL}, X1 pin only				0.4	V
Input High Voltage, V_{IH}, binary inputs	S1, OE	2			V
Input Low Voltage, V_{IL}, binary inputs	S1, OE			0.8	V
Input High Voltage, V_{IH}, trinary input	S0	V_{DD}-0.5			V
Input Low Voltage, V_{IL}, trinary input	S0			0.5	V
Operating Temperature		0		70	°C
VCXO control voltage, V_{IN}		0		3	V

Table 5. DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = 3.15 V to 3.45 V

Parameter	Condition	Min	Typ[1]	Max	Units
Output High Voltage, V_{OH}	I_{OH}=-25mA	2.4			V
Output Low Voltage, V_{OL}	I_{OL}=25mA			0.4	V
Operating Supply Current, I_{DD}	No Load		38		mA
Short Circuit Current	Each output		±85		mA
Input Capacitance	S0, S1, OE		7		pF

Note:

1. Typical values are at V_{DD} = 3.3V and 25°C

Table 6. AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = 3.15 V to 3.45 V

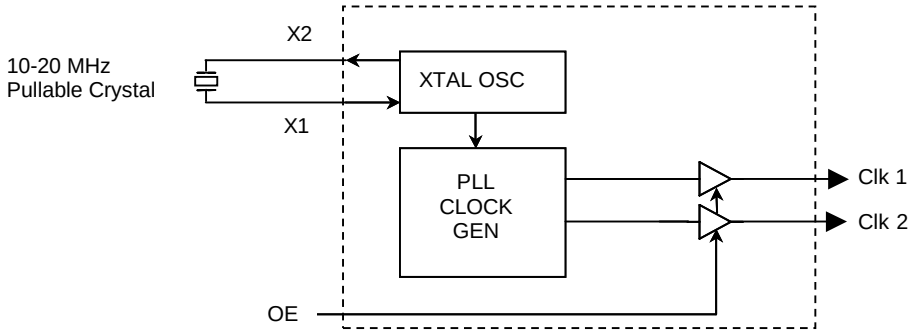
Symbol	Parameter	Condition	Min	Typ	Max	Units
Fosc	Input Crystal Frequency		10		20	MHz
tr	Output Clock Rise Time	0.8 to 2.0V			1.5	ns
tf	Output Clock Fall Time	2.0 to 0.8V			1.5	ns
t_{od}	Output Clock Duty Cycle	At V_{DD}/2	40		60	%
tpZL, tpZH	Enable Time. OE to CLK	C_L = 50pf		5	6.5	ns
tpLZ, tpHZ	Disable Time. OE to CLK	C_L = 50pf		4	5.5	ns
t_{jit} (pk – pk)	Maximum Absolute Jitter (Peak to Peak)			±100		ps
	Phase Noise, relative to carrier	10 KHz offset		-115		dBc/Hz
	Output pullability	0V ≤V_{IN} ≤3V	±100			ppm

Note:
1. Typical values are at V_{DD} = 3.3V and 25°C

Table 7 Pullable Crystal Specifications

Parameter	Value
Correlation (load) capacitance	30 pF
C0/C1	240 max
ESR	35 Ω max
Operating Temperature	0°C to +70°C
Initial Accuracy	±20 ppm
Temperature + Aging Stability	±50 ppm

Figure 3. External Crystal Connection Block Diagram



Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
VT83201S1	VT83201S1	Tubes	16	SOIC	0°C to +70°C
VT83201S1X	VT83201S1	Tape & Reel	16	SOIC	0°C to +70°C
VT83201/D		Dice in waffle packe			0°C to +70°C
VT83201/DW		Dice in wafer form			0°C to +70°C