TMB2193MS100

Demonstration Board for the TMC2193

Features

- 10-bit or 20-bit Parallel YCbCr input
- 24-bit RGB input
- D1, Genlock and Master mode operation
- Composite, S-video and component analog outputs
- Digital Composite output
- Fairchild demo board compatibility

Applications

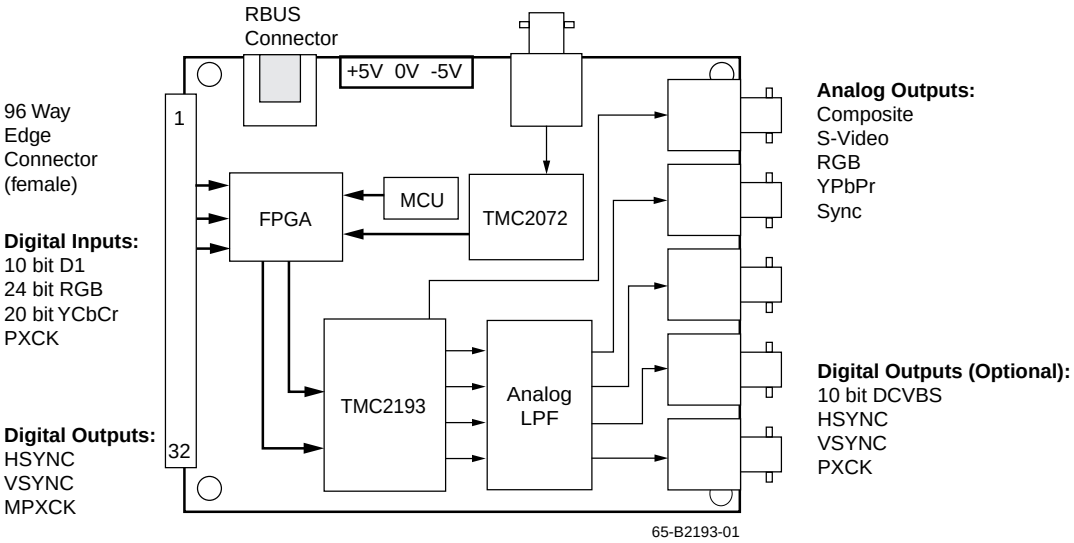
- Evaluation of TMC2193 DENC
- Evaluation of TMC2072 Genlock interface
- Output for TMC2068P7C Decoder demo board
- System Breadboarding

Description

The TMB2193MS100 demonstration board provides a flexible base for evaluating the performance of the TMC2193 Digital Video Encoder (DENC). The demonstration board can be driven by either a D1 or Genlock signal, or it can supply the synchronization signals needed to drive a framestore or any MPEG Decoder. Both YCbCr, in either 4:2:2, D1, or 4:4:4 formats, and RGB inputs are supported. The board provides high quality analog composite video, analog S-video, analog component video and digital composite video outputs.

Preliminary Information

Block Diagram



Rev. 0.9.0

Functional Description

The TMB2193MS100 is designed to demonstrate the performance of the TMC2193 Digital Video Encoder (DENC). For a complete description of the TMC2193, please refer to the TMC2193 data sheet. The TMB2193MS100 is compatible with other Fairchild Demo boards. Typical configurations are the TMC2067P7C, the TMC2068P7C, and the TMB2193MS100 or the TMB0001MS100 and the TMB2193MS100. The first configuration requires an analog composite or S-video input and supplies a re-encoded analog composite or S-video output. The later requires a parallel D1 input and supplies an encoded analog composite or S-video output.

The TMC2193 can be operated in D1, Genlock or Master mode. In the D1 mode the synchronization is derived from the TRS codes embedded in the D1 data stream. The TMB2193MS100 has the TMC2072 Genlock front end, which supplies the HSYNC, VSYNC and subcarrier information to the TMC2193 for the Genlock operation of the encoder. In Master mode the synchronization is driven by the TMC2193, supplying the line ($\overline{\text{HSYNC}}$) and field ($\overline{\text{VSYNC}}$ or BnT) synchronization signals. With the TMC2193 running in Master mode the TMB2193MS100 demo board interfaces directly to either a MPEG decoder or a video framestore with no additional glue logic.

The TMB2193MS100 has an onboard microcontroller (MCU) to program the TMC2193, the TMC2072, and to configure the FPGA. All the default register maps are held within the MCU. Table 1 provides a description of each of the default register maps. A control register map is written to the TMC2193, the TMC2072, and to Port 2 of the MCU each time the MRST\ button is pressed. The MCU determines which map to load from the PROG[3-0] (Px) dip switches. The TMC2193, 2072 and the MCU can also be driven by the Raydemo software. The interface is provided by the RBUS connector on the TMB2193MS100 and the TMC2070P7C R-Bus interface board. With this setup the user can configure the TMC2193, the TMC2072 and the MCU with any IBM compatible PC.

Table 1. Default Control Register Maps

P3	P2	P1	P0	Format	Mode	Source	Output Mode
0	0	0	0	NTSC	MASTER	Mod. Ramp	Composite, S-Video
0	0	0	1	NTSC	MASTER	75% CB	Composite, YPBPR
0	0	1	0	NTSC	MASTER	100% CB	Composite, RGB
0	0	1	1	NTSC	D1	D1	Composite, YPBPR
0	1	0	0	NTSC	D1	D1	Composite, RGB
0	1	0	1	NTSC	D1	D1	DCVBS
0	1	1	0	NTSC	Genlock	601	Composite, YPBPR
0	1	1	1	NTSC	Genlock	601	Composite, RGB
1	0	0	0	PAL	MASTER	Mod. Ramp	Composite, S-Video
1	0	0	1	PAL	MASTER	75% CB	Composite, YPBPR
1	0	1	0	PAL	MASTER	100% CB	Composite, RGB
1	0	1	1	PAL	D1	D1	Composite, YPBPR
1	1	0	0	PAL	D1	D1	Composite, RGB
1	1	0	1	PAL	D1	D1	DCVBS
1	1	1	0	PAL	Genlock	601	Composite, YPBPR
1	1	1	1	PAL	Genlock	601	Composite, RGB

CPLD Description

The Altera 10K20 CLPD functions as the central matrix for routing the buses to the TMC2193. Eight (8) control pins are connected from port 2 of the MCU to the CLPD. These pins are used to configure the CPLD and are broken up into 2 buses: FPGA control1 is on pins P2[7:4] and FPGA control2 is on pins P2[3:0]. The 10K20 default configuration routes the 3 buses from the input edge connector and the bus from the framestore header to the pixel data (PD[23:0]) port of the TMC2193. This enables the various input formats of the TMC2193 to be supported. In addition, the PD input can be delayed in respect to the HSIN and VSIN for proper data alignment. Table 2 describes the function of the pixel data formatting.

Table 2. FPGA Control 1

FGPA Control1 bit#	Function	Description
3-2	PDMODE	PD Input
	00	10-bit format, A bus
	01	20-bit format, C and B buses
	10	24-bit format, C, A, and B buses
	11	10-bit format, A bus delayed
1-0	PDDEL	PD delay
	00	0 pxck's of delay
	01	1 pxck's of delay
	10	2 pxck's of delay
	11	3 pxck's of delay

The FPGA Control 2 bus selects which subcarrier reference signal to be used; either the GRS from the TMC2072 or the xRS signal from bus B of the input edge connector. FGPA Control 2 also selects which set of synchronization signals are to used; either the IXHSYNC and IXVSYNC from the input edge connector or the TMC2072 GHSYNC and GVSYNC.

Table 3. FPGA Control 2

FGPA Control2 bit#	Function	Description
3-2		No Modes
1	REFSEL	CVBS Input
	0	B[5:2] bus
	1	GENLOCK
0	SYNCSEL	HSIN, VSIN Input
	0	IXH and IXV
	1	GH and GV

FPGA Controls 1 and 2 can be accessed by the Raydemo software. The dialog box exists in the MCU icon of the TMB2193MS100 window. The functions of these controls are purposely left generic to allow for the reconfiguration of the CPLD.

The 10K20 utilization is approximately 20% of the available logic cells. This allows for additional functions to be implemented in the 10K20 such as notch filters, interpolation filters for 4:2:2 to 4:4:4 conversion, simple comb filtering and ancillary data insertion. These are just some of the possibilities.

Table 4. Switch, Button, and Jumper Description

Button	Description
$\overline{\text{MRST}}$	Resets the AT89C55. When the GLOBAL RESET jumper is in place, the reset line on all boards connected to the TMB2193MS100 are driven by $\overline{\text{MRST}}$.
Jumpers	**Description**
GLOBAL RESET	When GLOBAL RESET is open, only the TMC2193, the TMC2072, the framestore header and the AT89C55 receive the reset pulse from $\overline{\text{MRST}}$. When GLOBAL RESET is closed, the reset line on all boards connected to the TMB2193MS100 are driven by $\overline{\text{MRST}}$.
CASC INT	**Cascade Programming Enable.** When CASC INT is open, the AT89C55 automatically initializes the devices after reset. When CASC INT is closed, the AT89C55 will wait for a LOW pulse on the PGM_IN pin before initializing the devices on the TMB2193MS100.
RBUSEN	When RBUSEN is open, the RBUS port is disabled. When RBUSEN is closed, the RBUS port is enabled.

Preliminary Information

Table 4. Switch, Button, and Jumper Description (continued)

Button	Description
JP20, JP21, JP22, JP23	When JPx is open, the output video is a single 75Ohm termination. When JPx is closed, the output video is a double 75Ohm termination.
Switches	**Description**
E1	**Onboard Clock Selection.** Selects either the PXCK from the TMC2072 or the onboard TTL clock oscillator.
E2	**Master Clock Selection.** When Pass is selected the clock source for the entire board is either the TMC2072 PXCK or the TTL clock oscillator. When IXPCK is selected the clock source for the entire board is the PXCK from the input header.
E3	**Output Header Clock Selection.** Selects either PXCK or $\overline{\text{PXCK}}$ for the output header.
Dip Switches	**Description**
SA1-0	Configures the bits 2 and 1 of the TMC2193 RBUS chip address. When SAx is ON (down), ESAx is in a LOW state. When SAx is OFF (up), ESAx is in a HIGH state.
CAS	Configures the bit 2 of the TMC2072 RBUS chip address. When CAS is ON (down), GSA1 is in a LOW state. When CAS is OFF (up), GSA1 is in a HIGH state.
ERS	Configures the bit 1 of the TMC2072 RBUS chip address. When ERS is ON (down), GSA0 is in a LOW state. When ERS is OFF (up), GSA0 is in a HIGH state.
P3-0	**Control Register Programming.** P3-0 selects which control register map to configure the devices with. Refer to Table 1 Default Control Register Maps for a description.

Setup Procedure

Set E1 to MPXCK and E2 to PASS, enable the onboard TTL clock oscillator as the clock source.

1. Set ESA1-0 to ON (down).
2. Set P3-0 to 0h, P3 is ON (down), P2 is ON (down), P1 is ON (down), and P0 is ON (down).
3. Plug in power supply connector and apply power. The LED's corresponding to +5 Volts and -5 Volts should be illuminated.
4. Reset board by pressing the MRST button.
5. Connect a scope probe to TP25 and adjust R39 until the sync to blank amplitude is 286 mV.
6. Connect a scope probe to TP19 and adjust R36 until the sync to blank amplitude is 286 mV.
7. Connect a scope probe to TP21 and adjust R37 until the sync to blank amplitude is 286 mV.
8. Connect a scope probe to TP23 and adjust R38 until the burst amplitude is 286 mV.

Power Supply Requirements

The TMB2193MS100 board requires 1.5 Amps from the +5 Volt power supply and 0.5 Amps from the -5 Volt power supply. Both the +5 Volt and -5 Volt supplies are connected to the input connector to supply the power requirements of any upstream board. The +5 Volt power supply not only drives TTL logic devices but it also provides the power and voltage references to the D/A's in the TMC2193. Therefore, it is recommended that a bench power supply be used with the cable lengths kept to a minimum.

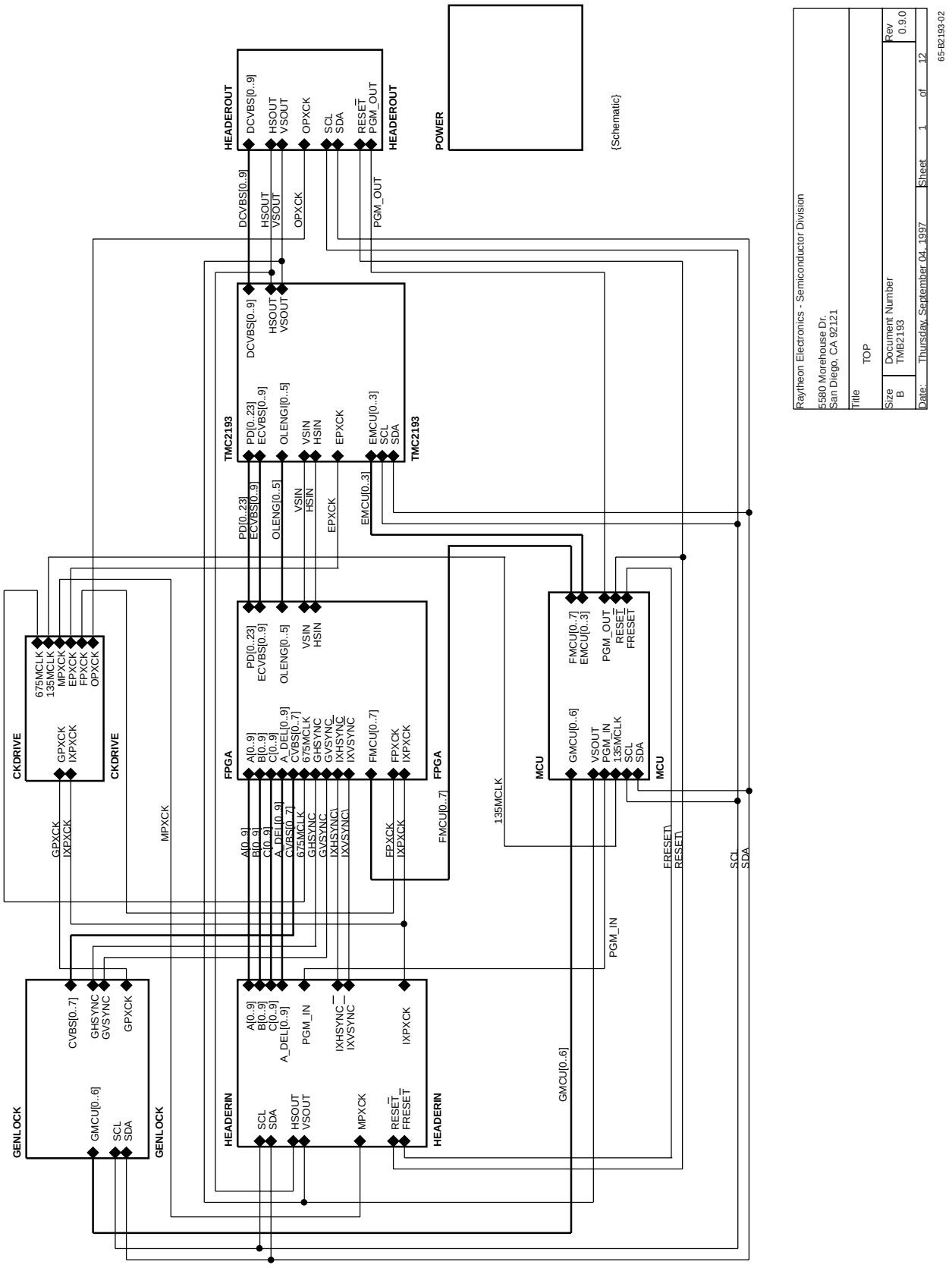


Figure 1.

Preliminary Information

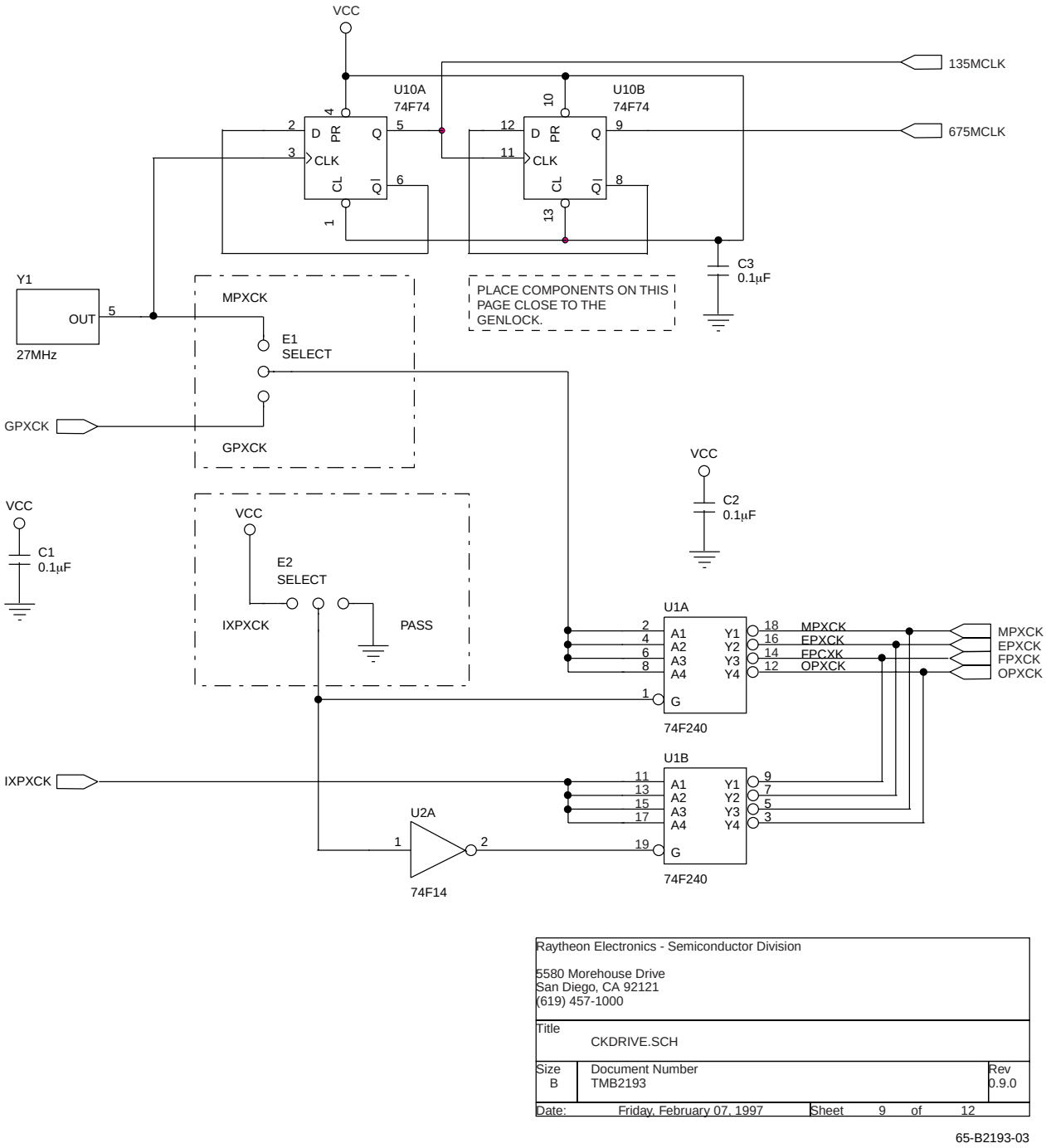


Figure 2.

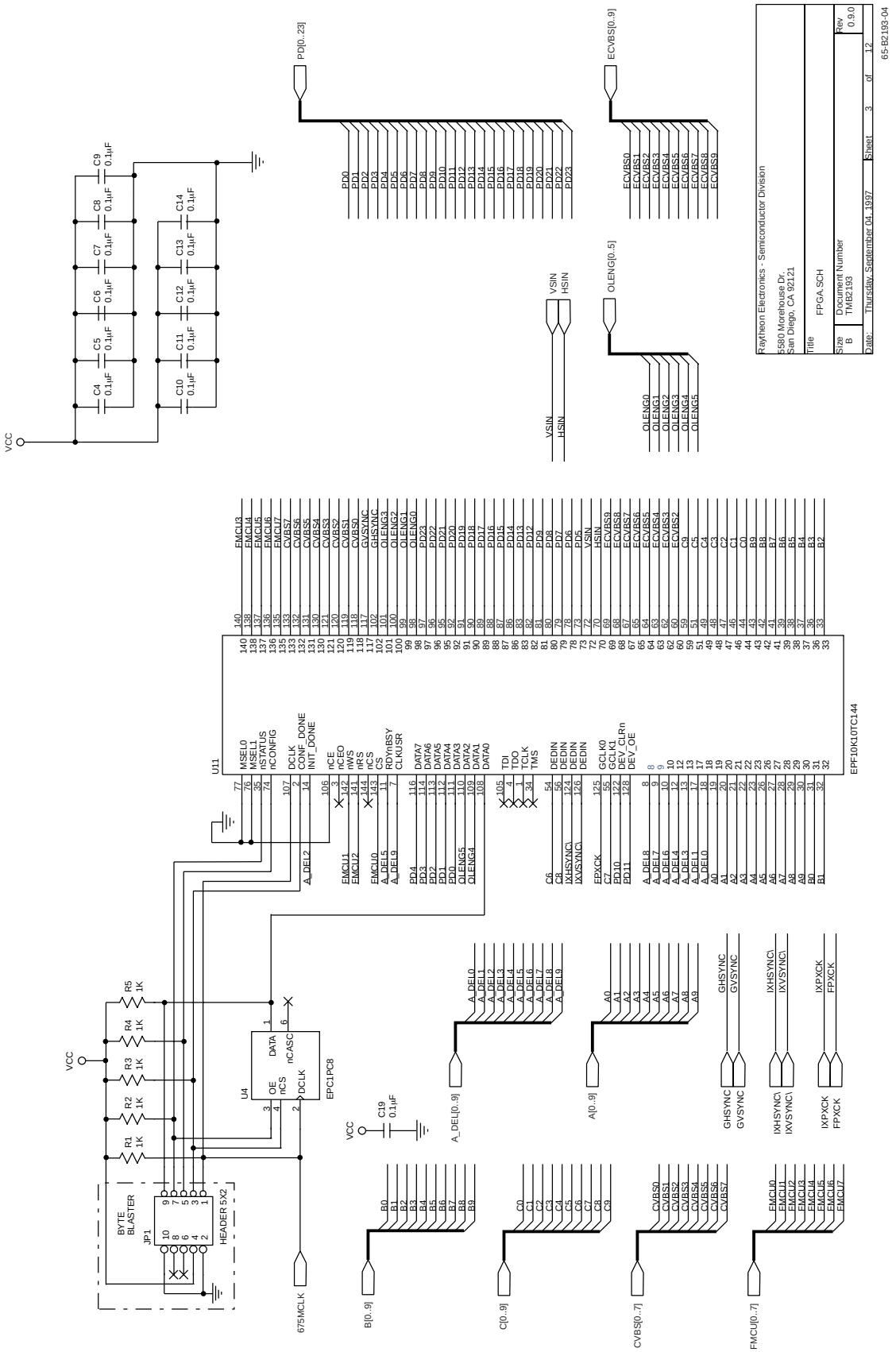


Figure 3.

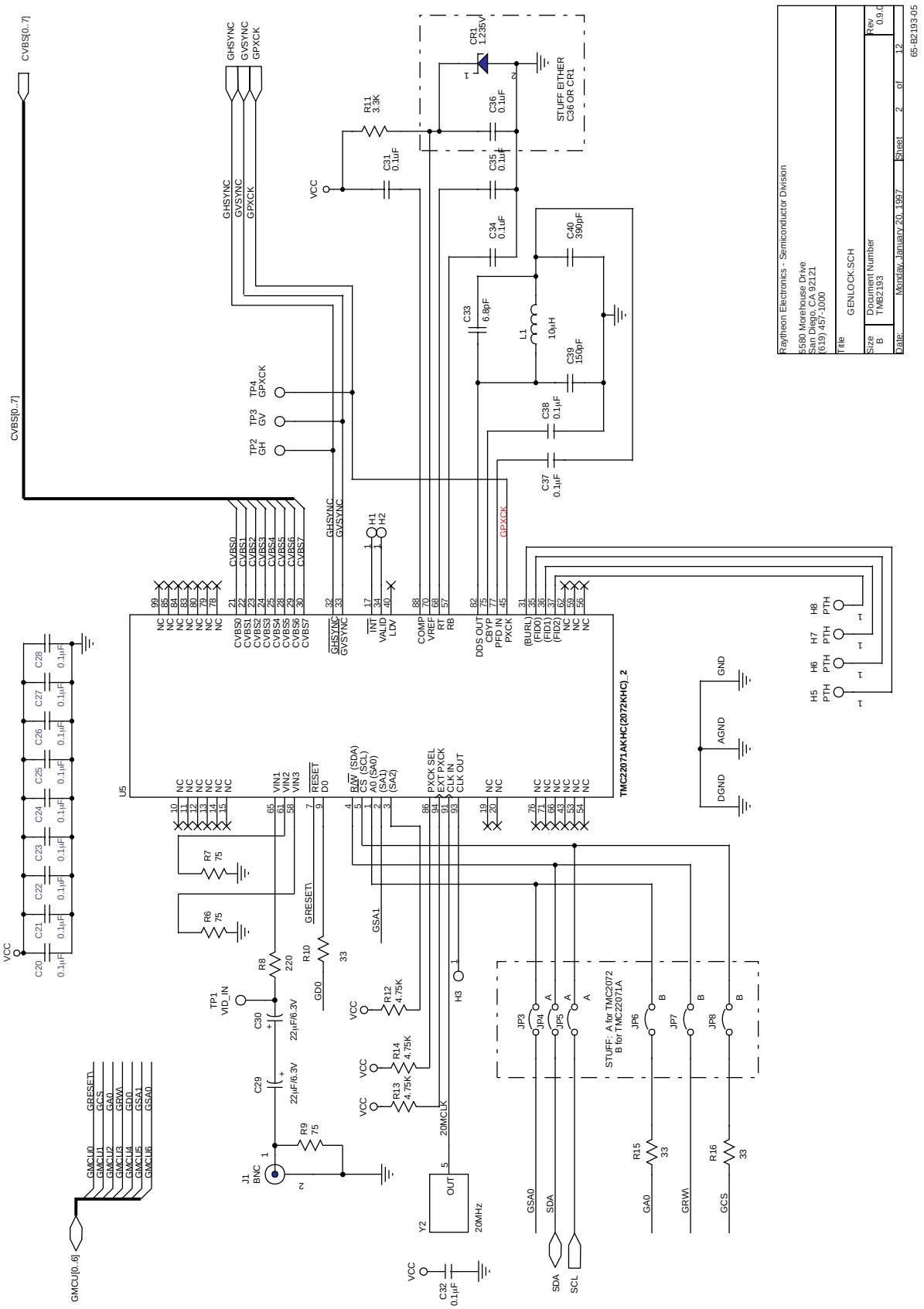


Figure 4.

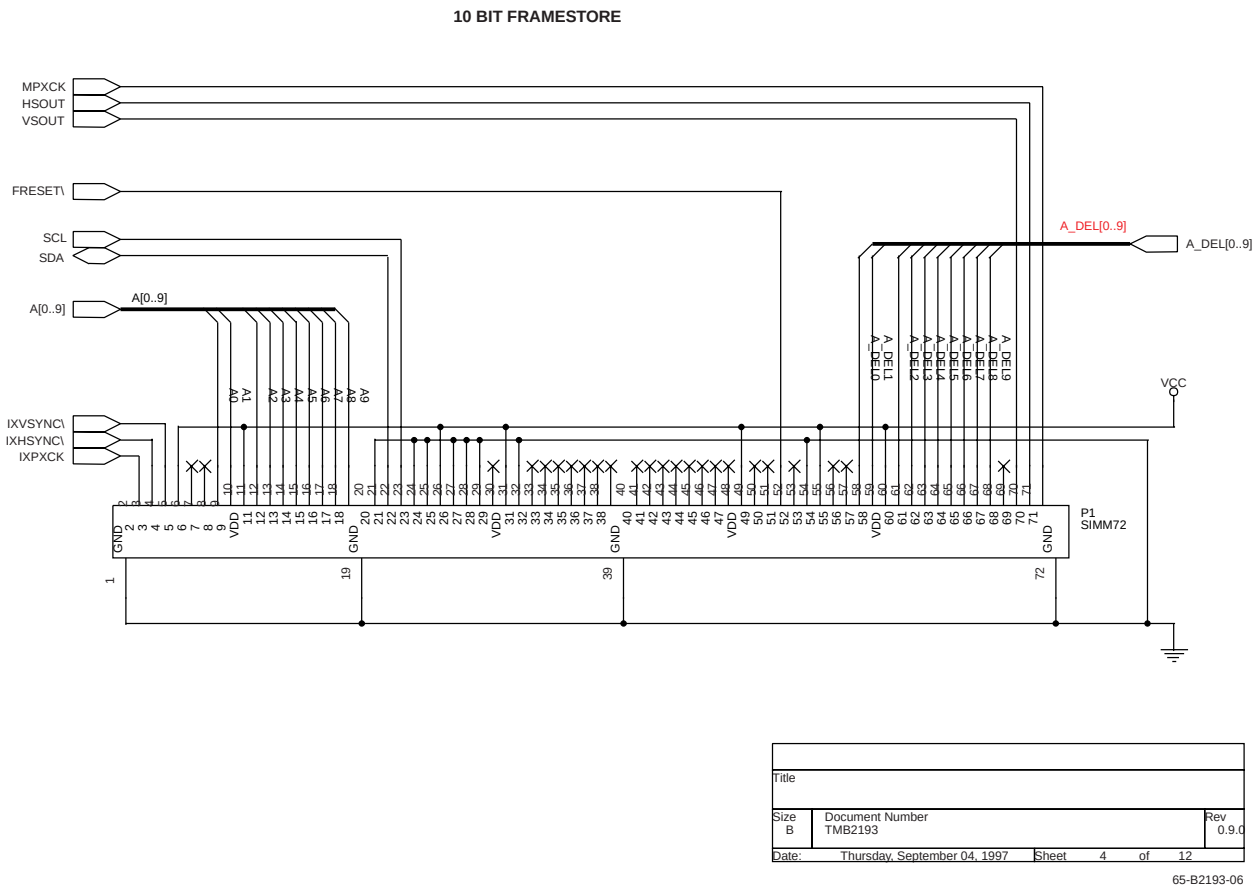
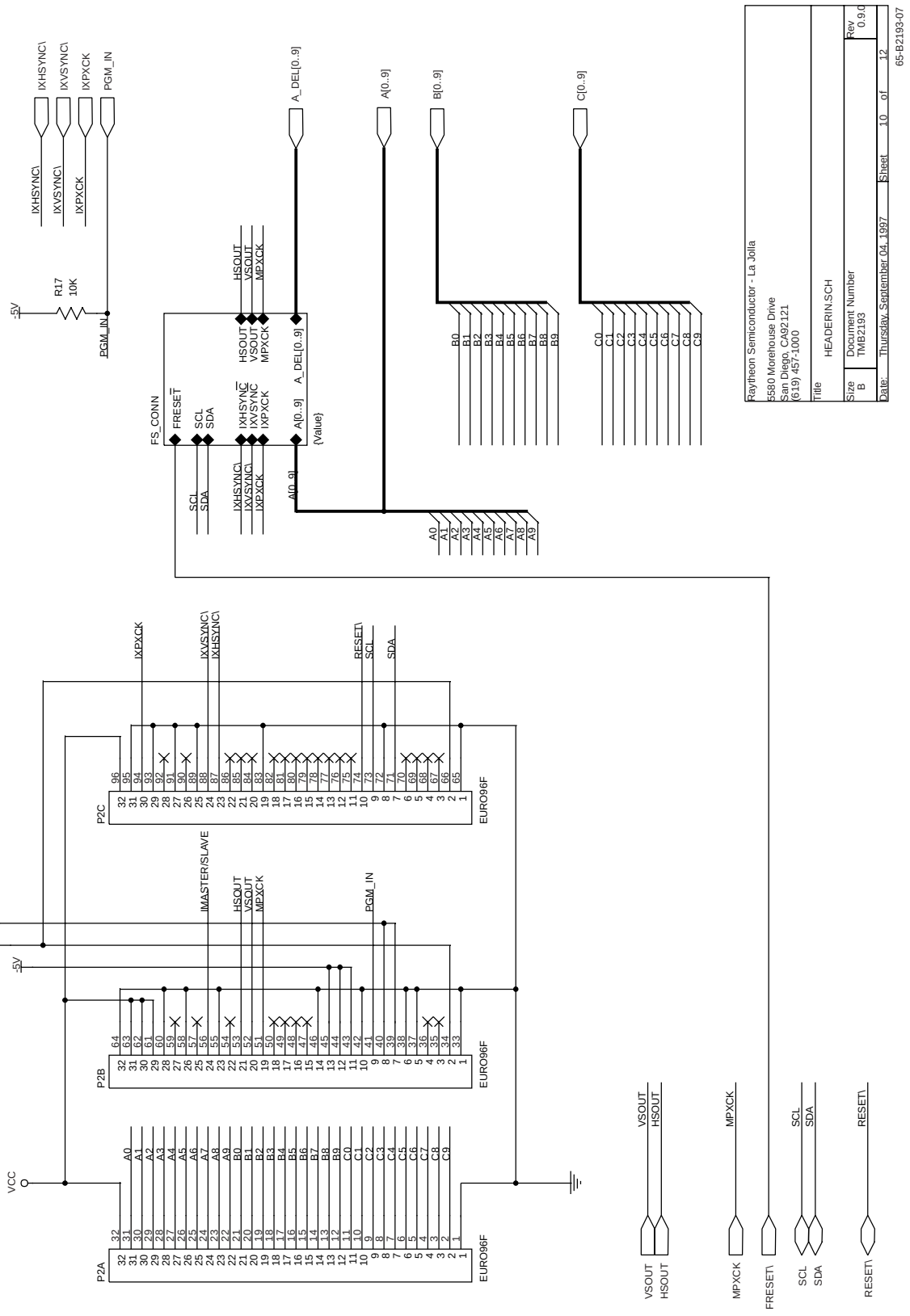


Figure 5.

Preliminary Information



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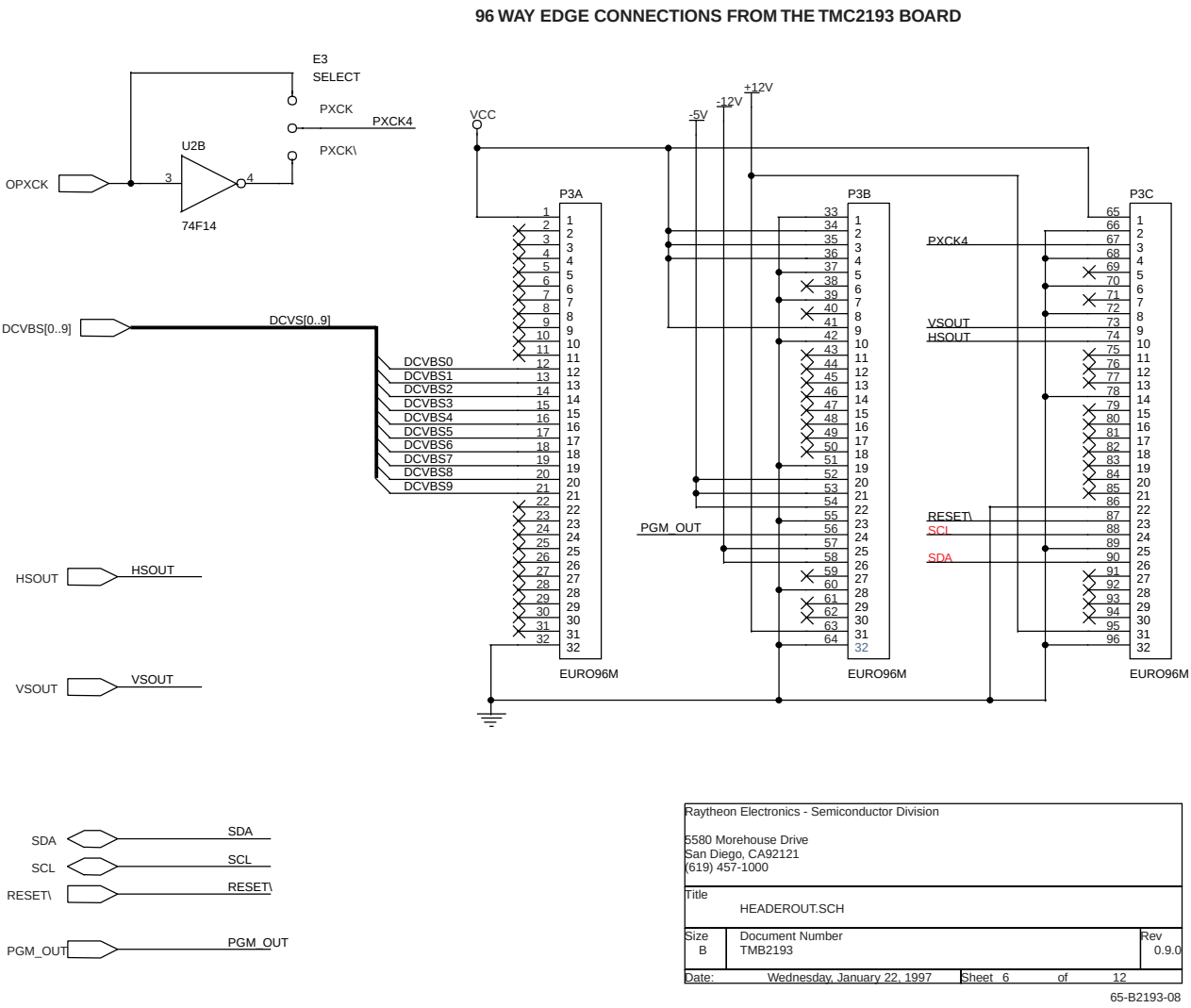

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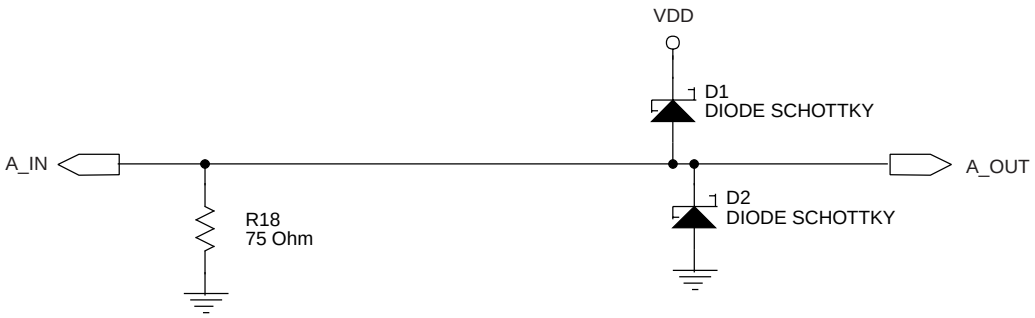

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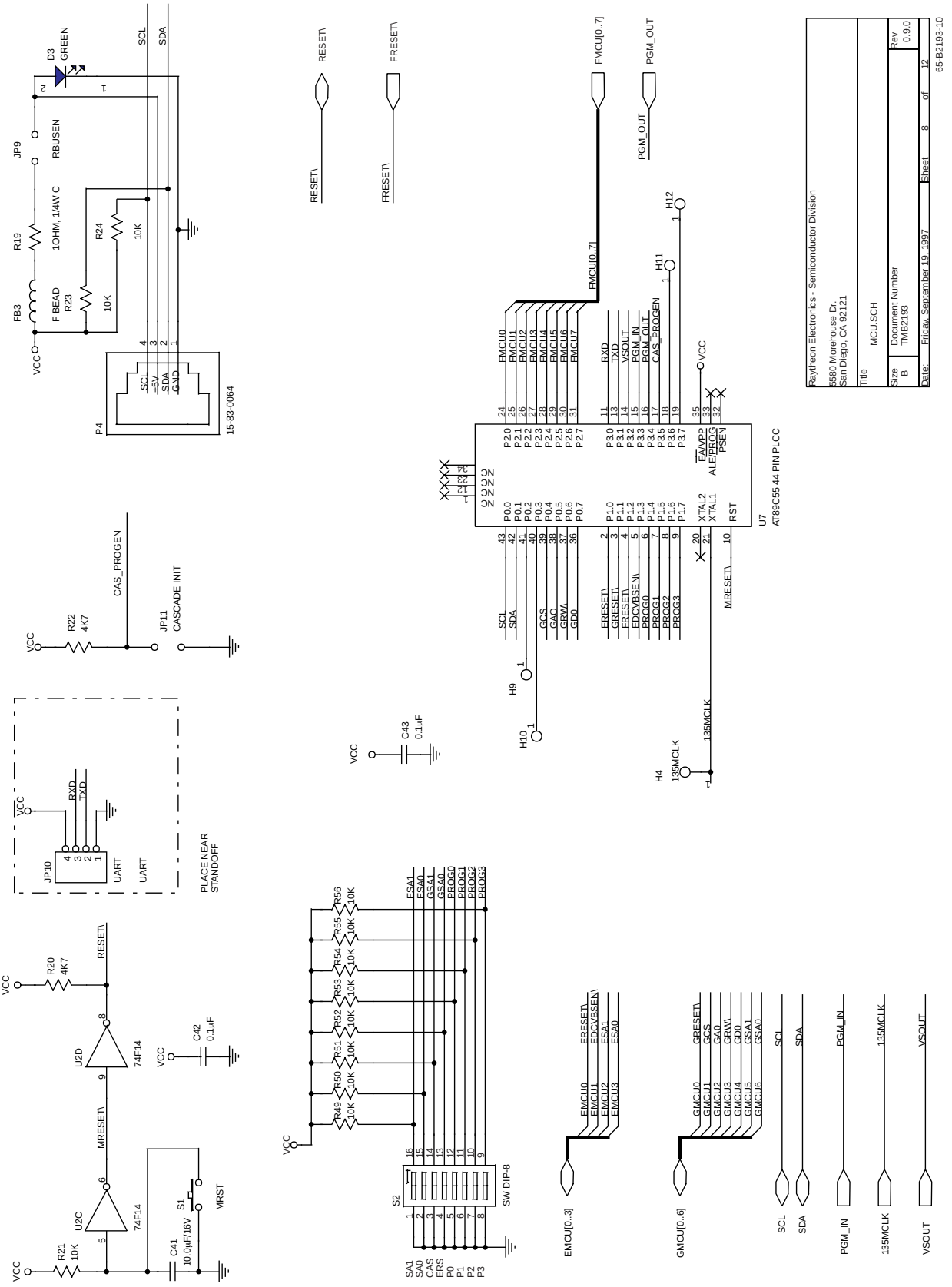
Figure 8.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San Diego, CA 92121
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Size B
Document Number TMB2193
Rev 0.9.0
Date: Friday, September 19, 1997
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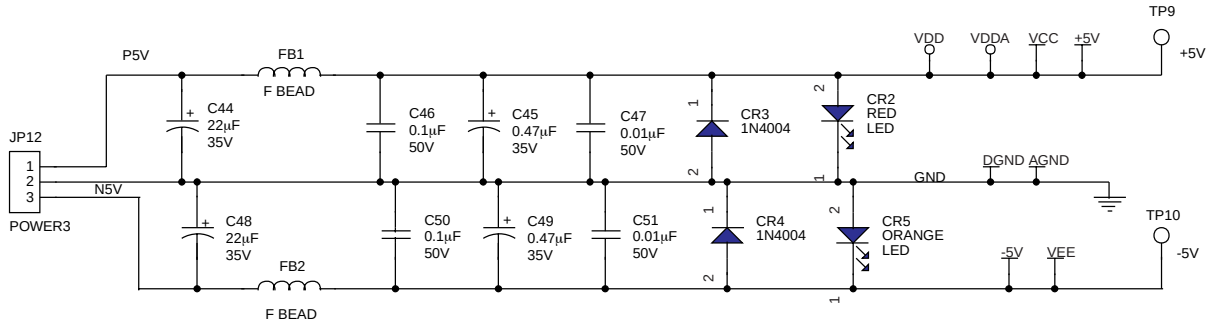
RESET\
FRESET\
FMCU[0..7]
PGM_OUT
U7
AT89C55 44 PIN PLCC
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
P2.0
P2.1
P2.2
P2.3
P2.4
P2.5
P2.6
P2.7
P3.0
P3.1
P3.2
P3.3
P3.4
P3.5
P3.6
P3.7
RST
XTAL1
XTAL2
EA/VPP
ALE/PROG
PSEN
RXD
TXD
VSOUT
PGM_IN
CAS_PROGEN
SCL
SDA
GCS
GA0
GRW\
GD0
ERESET\
GRESET\
FRESET\
EDCVBSEN\
PROG0
PROG1
PROG2
PROG3
MRESET\
135MCLK
H4
H9
H10
H11
H12
JP9
RBUSEN
D3
GREEN
R19
10HM, 1/4W C
F BEAD
FB3
R23
10K
R24
10K
P4
15-83-0064
SCL
+5V
SDA
GND
R22
4K7
JP11
CASCADE INIT
CAS_PROGEN
JP10
UART
PLACE NEAR STANDOFF
R20
4K7
U2D
74F14
C42
0.1µF
R21
10K
U2C
74F14
C41
10.0µF/16V
S1
MRST
C43
0.1µF
R49
10K
R50
10K
R51
10K
R52
10K
R53
10K
R54
10K
R55
10K
R56
10K
S2
SW DIP-8
SA1
SA0
CAS
ERS
P0
P1
P2
P3
EMCU[0..3]
GMCU[0..6]
VCC

Figure 9.



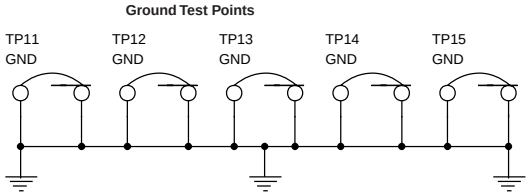


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Figure 10.

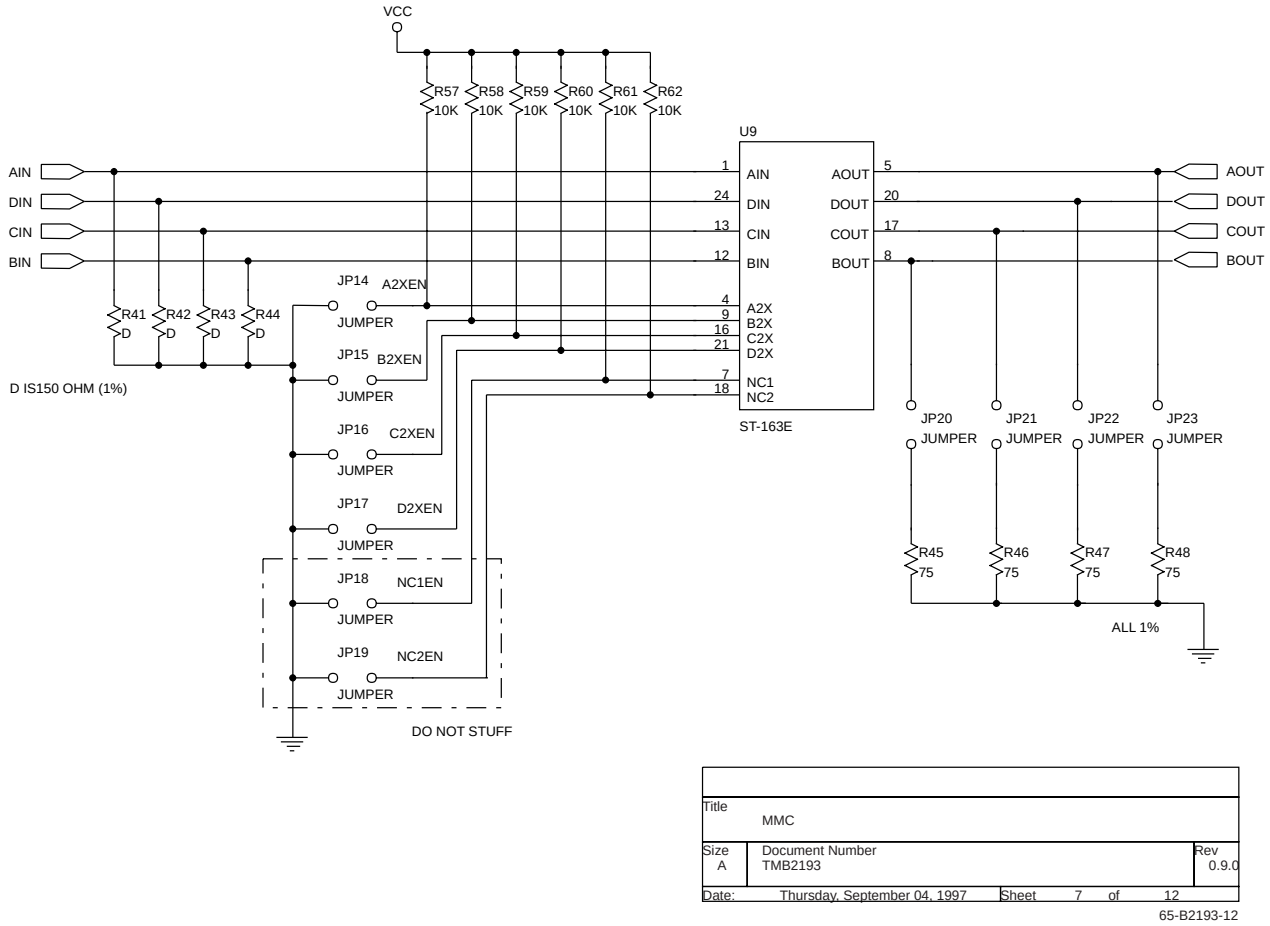


Figure 11.

Preliminary Information

Preliminary Information

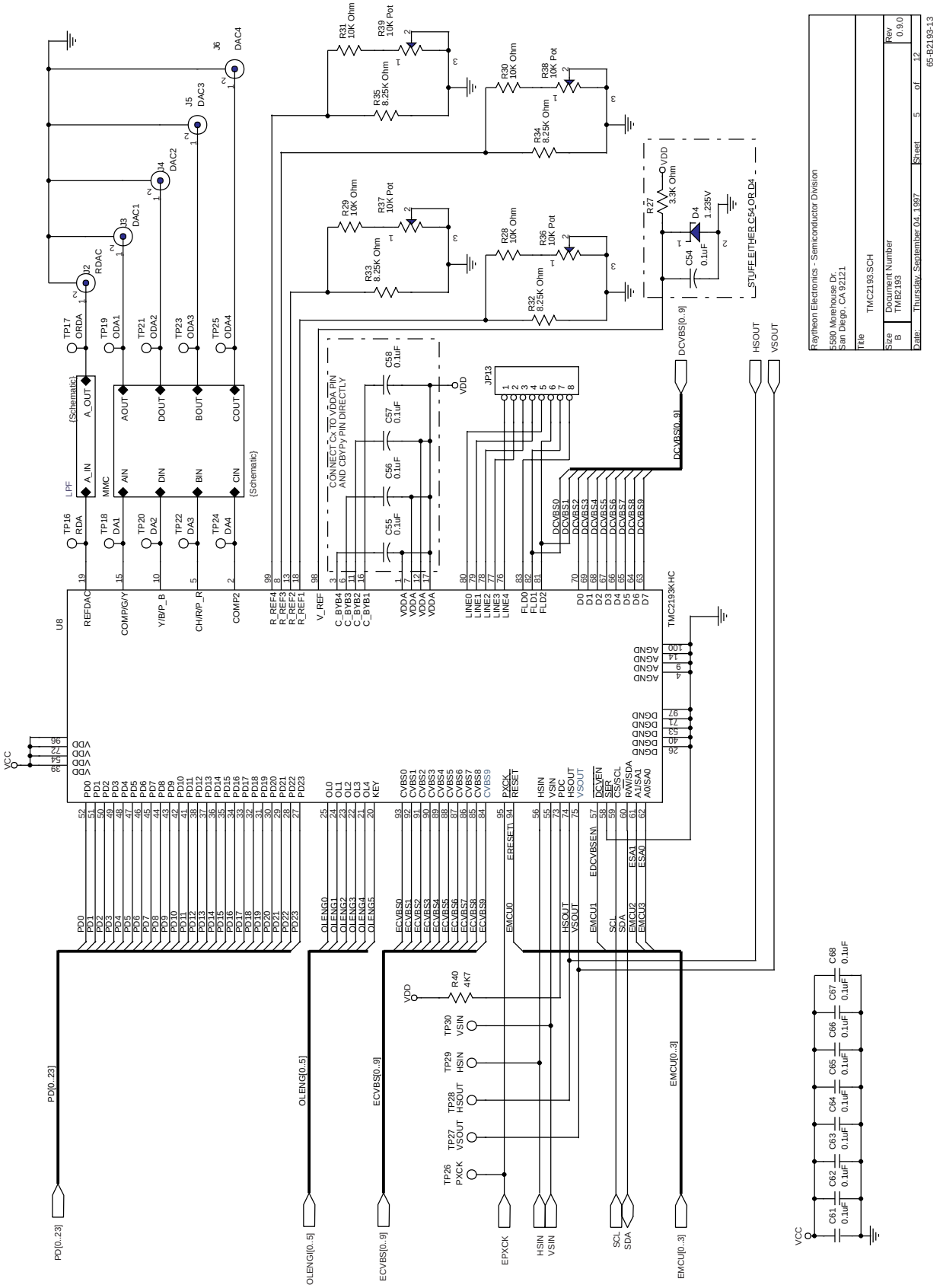


Figure 12.

Table 5. TMB2193MS100 Parts List

Item	Quantity	Reference	Part Number	Manufacturer	Description
1	48	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C19 C20 C21 C22 C23 C24C25 C26 C27 C28 C31 C32 C34 C35 C36 C37 C38 C42 C43 C46 C50 C54 C55 C56 C57 C58 C61 C62 C63 C64 C65 C66 C67 C68		MiniReel: 605-611	0.1μF (0805 FP)
2	2	C29 C30		Minireel	22μF/6.3v (D FP)
3	1	C33		MiniReel: 605-168	6.8pF (0805 FP)
4	1	C39		MiniReel: 605-315	150pF (0805 FP)
5	1	C40		MiniReel: 605-339	390pF (0805 FP)
6	1	C41		MiniReel: 642-810	10.0μF/16V (B FP)
7	2	C44 C48		MiniReel: 645-823	22μF/25v (D FP)
8	2	C45 C49		MiniReel: 641-647	0.47μF/25v (A FP)
9	2	C47 C51		MiniReel: 605-510	0.01μF (0805 FP)
10	5	R1 R2 R3 R4 R5		MiniReel: 615-410	1K (0805 FP)
11	7	R6 R7 R9 R45 R46 R47 R48		MiniReel: 615-275	75 (0805 FP)
12	1	R8		MiniReel: 615-822	220 (0805 FP)
13	3	R10 R15 R16		MiniReel: 615-844	33 (0805 FP)
14	1	R11		MiniReel: 615-844	3.3K (0805 FP)
15	3	R12 R13 R14		MiniReel: 615-447	4.75K (0805 FP)
16	18	R17 R21 R23 R24 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62		MiniReel: 615-510	10K (0805 FP)
17	1	R18		MiniReel: 615-275	75 (0805 FP)
18	1	R19		ROHM	1 OHM, 1/4W Carbon
19	3	R20 R22 R40		MiniReel: 615-848	4.7k (0805 FP)
20	1	R27		MiniReel: 615-844	3.3K Ohm (0805 FP)
21	4	R28 R29 R30 R31		MiniReel: 615-849	10K Ohm (0805 FP)
22	4	R32 R33 R34 R35		MiniReel: 615-415	8.25K Ohm (0805 FP)
23	4	R36 R37 R38 R39		Bourns	10K Pot (SMT)
24	4	R41 R42 R43 R44			150 (0805 FP)
25	1	L1		MiniReel	10uH (3225M FP)
26	3	FB1 FB2 FB3		Ferrite	Ferrite Bead
27	2	CR1 D4		Linear Technology	1.235V Reference
28	2	D1 D2		Motorola	Diode Schottky
29	2	CR3 CR4		MiniReel: 76-4004	Diode Rectifier
30	1	CR2		Hewlett Packard	Red LED
31	1	CR5		Hewlett Packard	Orange LED
32	1	D3		Hewlett Packard	Green LED
35	1	JP1		Amp	Header 5X2

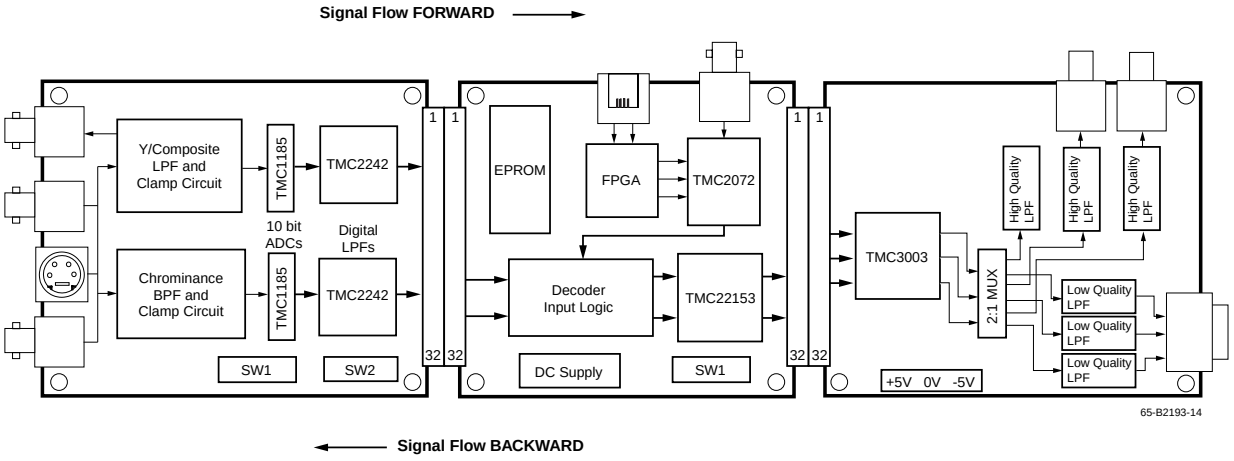
Table 5. TMB2193MS100 Parts List (continued)

Item	Quantity	Reference	Part Number	Manufacturer	Description
36	6	JP9 JP11 JP20 JP21 JP22 JP23		Amp	2 Pin Header
37	1	JP10		Amp	4 Pin Header
38	1	JP13		Amp	8 Pin Header
39	1	P1		Amp	72 Pin Header
40	1	JP12		Beau	Power, Plug Power, Socket
41	6	J1 J2 J3 J4 J5 J6		Amphenol	BNC
42	1	P2		Amp	96 Pin Euro Connector (Female)
43	1	P3		Amp	96 Pin Euro Connector (Male)
44	1	P4		Molex	Rbus Connector
45	3	E1 E2 E3		Secma	SPDT Switch
46	1	S1		ITT Canon	SMT Push Button Switch
47	1	S2		Alco	8 Position DIP Switch
48	21	TP1 TP2 TP3 TP4 TP9 TP10 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30		Mouser	Test Point
49	5	TP11 TP12 TP13 TP14 TP15		Bare Wire	Ground Point
50	1	U1		Motorola	74F240
51	1	U2		Motorola	74F14
52	1	U4		Atmel	Serial Eprom
53	1	U5		Fairchild	Genlock
54	1	U7		Atmel	Microprocessor
55	1	U8		Fairchild	Encoder
56	1	U9		MMC	Video Filter ST-163E
57	1	U10		Motorola	74F74
58	1	U11		Altera	FPGA
59	1	Y1		Ecliptec	27MHz
60	1	Y2		Ecliptec	20MHz

Table 6. INPUT 96 Way Connector (Female)

row A		row B		row C	
32	+**5V**	32	**GND**	32	**+5V**
31	D1 or R/V [bit 0]	31	**+5V**	31	**GND**
30	D1 or R/V [bit 1]	30	**+5V**	30	PXCK
29	D1 or R/V [bit 2]	29	**+5V**	29	**GND**
28	D1 or R/V [bit 3]	28	**GND**	28	PCK
27	D1 or R/V [bit 4]	27	***Analog Composite/luma***	27	**GND**
26	D1 or R/V [bit 5]	26	**GND**	26	CREF
25	D1 or R/V [bit 6]	25	***Analog chroma***	25	**GND**
24	D1 or R/V [bit 7]	24	XEN	24	$\overline{\text{VSYNC}}$
23	D1 or R/V [bit 8]	23	**GND**	23	$\overline{\text{HSYNC}}$
22	D1 or R/V [bit 9]	22	XDIR	22	HREF
21	Comp, G/Y, or Luma [bit 0]	21	$\overline{\text{XHSYNC}}$	21	VREF
20	Comp, G/Y, or Luma [bit 1]	20	$\overline{\text{XVSYNC}}$	20	ODD IN
19	Comp, G/Y, or Luma [bit 2]	19	XPXCK	19	**GND**
18	Comp, G/Y, or Luma [bit 3]	18	XRS [bit 3]	18	NTSC/PAL
17	Comp, G/Y, or Luma [bit 4]	17	XRS [bit 2]	17	CLAMP pulse
16	Comp, G/Y, or Luma [bit 5]	16	XRS [bit 1]	16	RGB
15	Comp, G/Y, or Luma [bit 6]	15	XRS [bit 0]	15	
14	Comp, G/Y, or Luma [bit 7]	14	**GND**	14	
13	Comp, G/Y, or Luma [bit 8]	13	**-5V**	13	
12	Comp, G/Y, or Luma [bit 9]	12	**-5V**	12	LOCK
11	Chroma or B/U [bit 0]	11	**-5V**	11	D1
10	Chroma or B/U [bit 1]	10	GND	10	$\overline{\text{RESET}}$
9	Chroma or B/U [bit 2]	9	PGM_IN	9	SCL
8	Chroma or B/U [bit 3]	8	**-12V**	8	GND
7	Chroma or B/U [bit 4]	7	**-12V**	7	SDA
6	Chroma or B/U [bit 5]	6	IE (input enable)	6	OE (output enable)
5	Chroma or B/U [bit 6]	5	**GND**	5	$\overline{\text{BLANK}}$ (DAC)
4	Chroma or B/U [bit 7]	4		4	
3	Chroma or B/U [bit 8]	3		3	
2	Chroma or B/U [bit 9]	2	**+12V**	2	**+12V**
1	**GND**	1	**GND**	1	**GND**

Input Edge Connector Design Notes

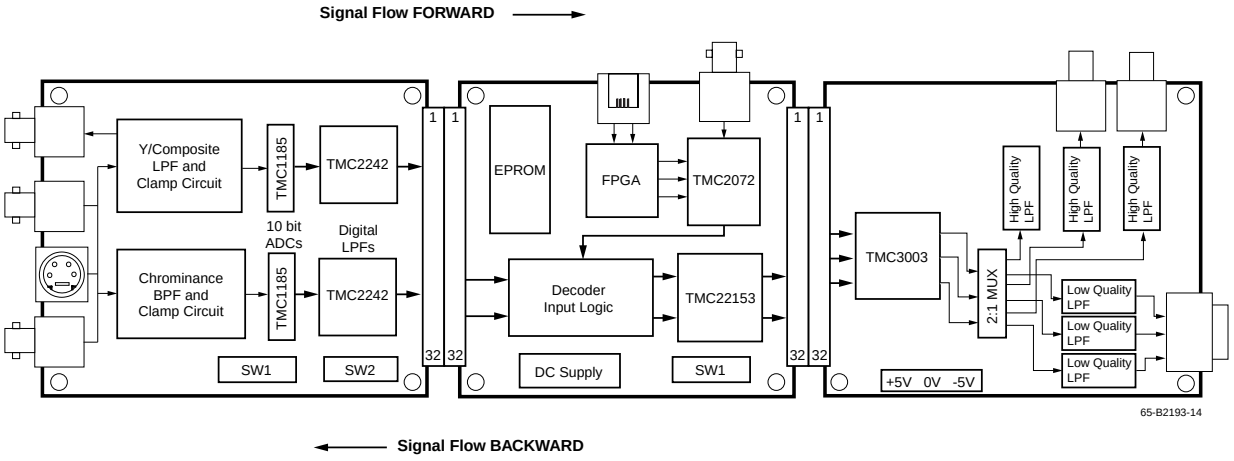


1. **Boards with different revision letters may not be compatible. Damage may occur if they are connected together!**
2. XPXCK is a two times pixel clock fed BACKWARD.
3. XHSYNC and XVSYNC are timing reference signals fed BACKWARD.
4. The MASTER/SLAVE signal states if a board is a MASTER or a SLAVE board. This signal is fed FORWARD. A MASTER board produces the PXCK, HSYNC, and VSYNC signals, and a SLAVE board expects to receive XPXCK, XHSYNC, XVSYNC, etc.
5. XDIR is fed FORWARD and controls in which direction the XRS[3:0] data flows.
6. PGM_IN is a negative going pulse, logically ANDed with the onboard program start pulse, for initiating the programming sequence for components on that board. Care must be taken to ensure that multiple devices do not try to drive the RBUS at any given time. Minimum width of PGM_IN is 1uS.
7. The RESET pin on the input edge connector should be connected directly to the RESET pin on the output connector. A link should be used to connect any pulse to the RESET line.
8. The MASTER/SLAVE, XDIR, PGM_IN and RESET pins on the input edge connector should be connected to +5V through a 10k pull up resistor.
9. The CLAMP signal is fed BACKWARD from a MASTER to a SLAVE board. The CLAMP signal should not be fed FORWARD.

Table 7. OUTPUT 96 Way Connector (Male)

row A		row B		row C	
1	**+5V**	1	**GND**	1	**+5v**
2	D1 or R/V [bit 0]	2	**+5V**	2	**GND**
3	D1 or R/V [bit 1]	3	**+5V**	3	PXCK
4	D1 or R/V [bit 2]	4	**+5V**	4	**GND**
5	D1 or R/V [bit 3]	5	**GND**	5	PCK
6	D1 or R/V [bit 4]	6	***Analog Composite/luma***	6	**GND**
7	D1 or R/V [bit 5]	7	**GND**	7	CREF
8	D1 or R/V [bit 6]	8	***Analog chroma***	8	**GND**
9	D1 or R/V [bit 7]	9	XEN	9	$\overline{\text{VSYNC}}$
10	D1 or R/V [bit 8]	10	**GND**	10	$\overline{\text{HSYNC}}$
11	D1 or R/V [bit 9]	11	XDIR	11	HREF
12	Comp, G/Y, or Luma [bit 0]	12	$\overline{\text{XHSYNC}}$	12	VREF
13	Comp, G/Y, or Luma [bit 1]	13	$\overline{\text{XVSYNC}}$	13	ODD IN
14	Comp, G/Y, or Luma [bit 2]	14	XPXCK	14	**GND**
15	Comp, G/Y, or Luma [bit 3]	15	XRS [bit 3]	15	NTSC/PAL
16	Comp, G/Y, or Luma [bit 4]	16	XRS [bit 2]	16	CLAMP pulse
17	Comp, G/Y, or Luma [bit 5]	17	XRS [bit 1]	17	RGB
18	Comp, G/Y, or Luma [bit 6]	18	XRS [bit 0]	18	
19	Comp, G/Y, or Luma [bit 7]	19	**GND**	19	
20	Comp, G/Y, or Luma [bit 8]	20	**-5V**	20	
21	Comp, G/Y, or Luma [bit 9]	21	**-5V**	21	LOCK
22	Chroma or B/U [bit 0]	22	**-5V**	22	D1
23	Chroma or B/U [bit 1]	23	**GND**	23	$\overline{\text{RESET}}$
24	Chroma or B/U [bit 2]	24	PGM_OUT	24	SCL
25	Chroma or B/U [bit 3]	25	**-12V**	25	GND
26	Chroma or B/U [bit 4]	26	**-12V**	26	SDA
27	Chroma or B/U [bit 5]	27	IE (input enable)	27	OE (output enable)
28	Chroma or B/U [bit 6]	28	**GND**	28	$\overline{\text{BLANK}}$ (DAC)
29	Chroma or B/U [bit 7]	29		29	
30	Chroma or B/U [bit 8]	30		30	
31	Chroma or B/U [bit 9]	31	**+12V**	31	**+12V**
32	**GND**	32	**GND**	32	**GND**

Output Edge Connector Design Notes



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5. XDIR is fed FORWARD and controls in which direction the XRS[3:0] data flows.
6. PGM_OUT negative going signal pulse for initiating programming of down stream boards, generated once the devices on the board have been programmed. Care must be taken to ensure that multiple devices do not try to drive the RBUS at any given time. The Minimum width of PGM_OUT is 1uS.
7. The RESET pin on the output edge connector should be connected directly to the RESET pin on the input connector. A link should be used to connect any pulse to the RESET line.
8. The MASTER/SLAVE, XDIR, PGM_OUT and RESET pins on the output edge connector should be connected to +5V through a 10k pull up resistor.
9. The CLAMP signal is fed BACKWARD from a MASTER to a SLAVE board. The CLAMP signal should not be fed FORWARD.

Related Products

- TMB22153MS101 Decoder demonstration board
- TMB1185MS102 ADC demonstration board
- TMB0000UG100 RBUS Interface
- TMB0001MS100 Parallel D1 interface board
- Raydemo software

Preliminary Information

Notes:

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMB2193MS100	25°C	27 MHz	Commercial	4" by 5" Printed Circuit Board	TMB2193MS100

A schematic database is available in OrCAD™ format. Contact the factory.

The TMB2193MS100 Demonstration Board, design documentation, and software are provided as a design example for the customers of Fairchild. Fairchild makes no warranties, express, statutory, or implied regarding merchantability or fitness for a particular purpose.

FCC Compliance

This device has not been approved by the Federal Communications Commission (FCC). This board is intended for the evaluation of Fairchild products only. This device is not and may not be offered for sale or lease or sold or leased until the approval of the FCC has been obtained.

Preliminary Information