

**ANSALDO****Ansaldo Trasporti s.p.a.  
Unita' Semiconduttori**Via N. Lorenzi 8 - I 16152 GENOVA - ITALY  
Tel. int. +39/(0)10 6556549 - (0)10 6556488  
Fax Int. +39/(0)10 6442510  
Tx 270318 ANSUSE I -**PHASE CONTROL THYRISTOR****AT875LT**

Repetitive voltage up to	<b>4400 V</b>
Mean on-state current	<b>2200 A</b>
Surge current	<b>25.2 kA</b>

**FINAL SPECIFICATION**

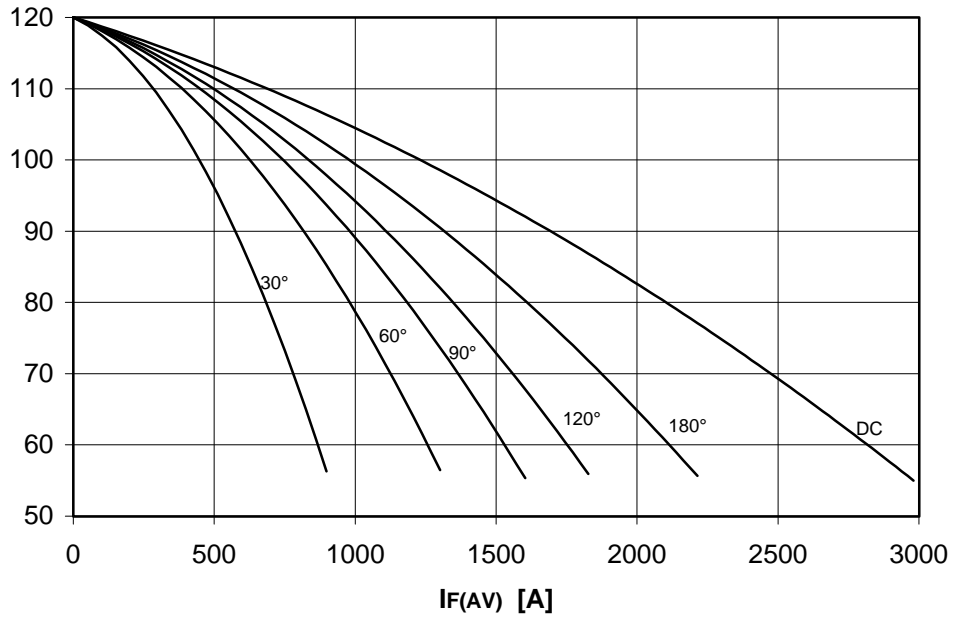
apr 97 - ISSUE : 01

Symbol	Characteristic	Conditions	T <sub>j</sub> [°C]	Value	Unit
<b>BLOCKING</b>					
V <sub>RRM</sub>	Repetitive peak reverse voltage		120	4400	V
V <sub>RSM</sub>	Non-repetitive peak reverse voltage		120	4500	V
V <sub>DRM</sub>	Repetitive peak off-state voltage		120	4400	V
I <sub>RRM</sub>	Repetitive peak reverse current	V=V <sub>RRM</sub>	120	200	mA
I <sub>DRM</sub>	Repetitive peak off-state current	V=V <sub>DRM</sub>	120	200	mA
<b>CONDUCTING</b>					
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Th=55°C, double side cooled		2200	A
I <sub>T(AV)</sub>	Mean on-state current	180° sin, 50 Hz, Tc=85°C, double side cooled		1720	A
I <sub>TSM</sub>	Surge on-state current	sine wave, 10 ms	120	25.2	kA
I <sup>2</sup> t	I <sup>2</sup> t	without reverse voltage		3175 x1E3	A <sup>2</sup> s
V <sub>T</sub>	On-state voltage	On-state current = 2000 A	25	2	V
V <sub>T(TO)</sub>	Threshold voltage		120	1.3	V
r <sub>T</sub>	On-state slope resistance		120	0.334	mohm
<b>SWITCHING</b>					
di/dt	Critical rate of rise of on-state current, min.	From 75% V <sub>DRM</sub> up to 1600 A, gate 10V 5ohm	120	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V <sub>DRM</sub>	120	1000	V/μs
t <sub>d</sub>	Gate controlled delay time, typical	V <sub>D</sub> =100V, gate source 40V, 10 ohm, tr=.5 μs	25	3	μs
t <sub>q</sub>	Circuit commutated turn-off time, typical	dV/dt = 20 V/μs linear up to 75% V <sub>DRM</sub>		400	μs
Q <sub>rr</sub>	Reverse recovery charge	di/dt=-20 A/μs, I <sub>s</sub> = 1050 A	120		μC
I <sub>rr</sub>	Peak reverse recovery current	V <sub>R</sub> = 50 V			A
I <sub>H</sub>	Holding current, typical	V <sub>D</sub> =5V, gate open circuit	25	300	mA
I <sub>L</sub>	Latching current, typical	V <sub>D</sub> =12V, tp=30μs	25	1000	mA
<b>GATE</b>					
V <sub>GT</sub>	Gate trigger voltage	V <sub>D</sub> =12V	25	3.5	V
I <sub>GT</sub>	Gate trigger current	V <sub>D</sub> =12V	25	400	mA
V <sub>GD</sub>	Non-trigger gate voltage, min.	V <sub>D</sub> =2000 V	120	0.8	V
V <sub>FGM</sub>	Peak gate voltage (forward)			30	V
I <sub>FGM</sub>	Peak gate current			10	A
V <sub>RGM</sub>	Peak gate voltage (reverse)			10	V
P <sub>GM</sub>	Peak gate power dissipation	Pulse width 100 μs		150	W
P <sub>G</sub>	Average gate power dissipation			2	W
<b>MOUNTING</b>					
R <sub>th(j-h)</sub>	Thermal impedance, DC	Junction to heatsink, double side cooled		9.5	°C/kW
R <sub>th(c-h)</sub>	Thermal impedance	Case to heatsink, double side cooled		2	°C/kW
T <sub>j</sub>	Operating junction temperature			-30 / 120	°C
F	Mounting force			40.0 / 50.0	kN
	Mass			1150	g
<b>ORDERING INFORMATION : AT875LT S 44</b>					
standard specification <input type="checkbox"/> VDRM&VRRM/100 <input type="checkbox"/>					

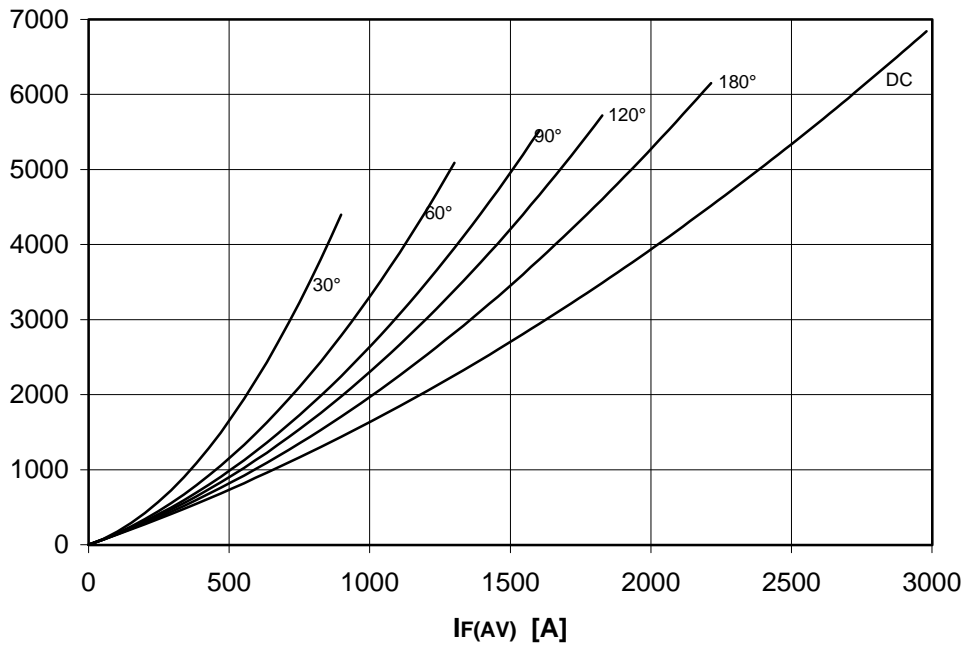
DISSIPATION CHARACTERISTICS

SQUARE WAVE

Th [°C]



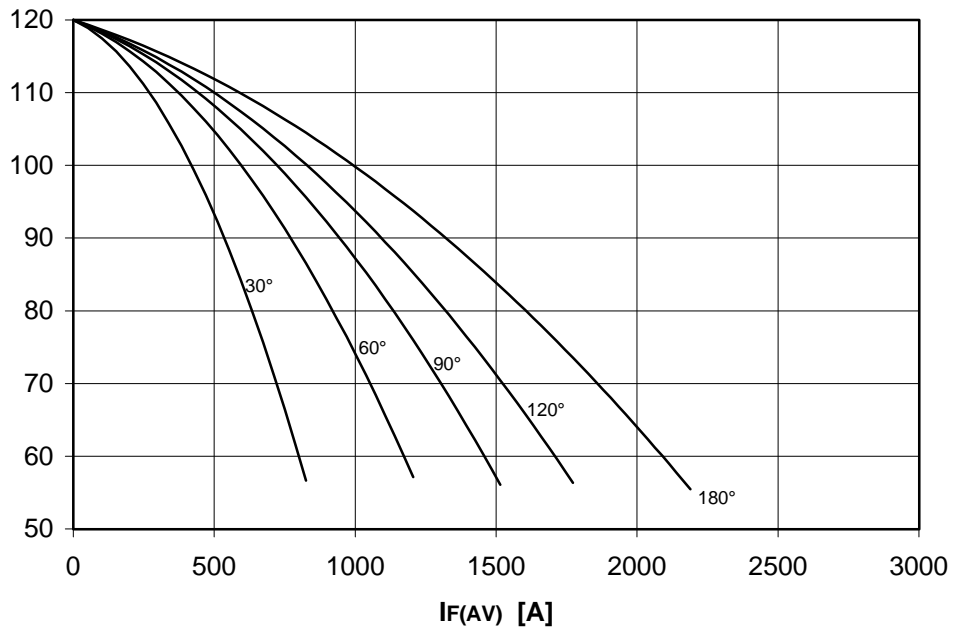
PF(AV) [W]



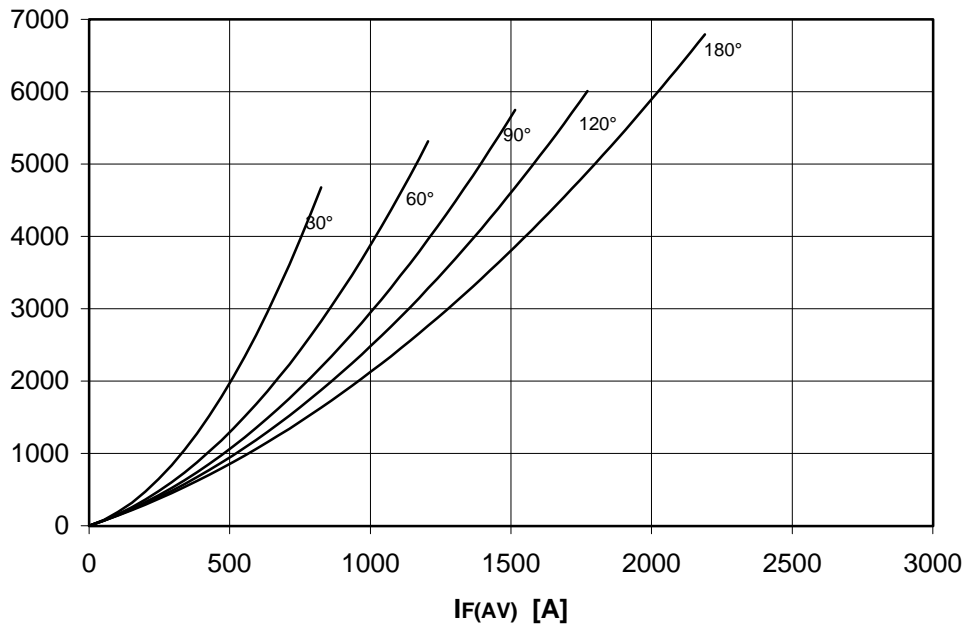
DISSIPATION CHARACTERISTICS

SINE WAVE

Th [°C]



PF(AV) [W]

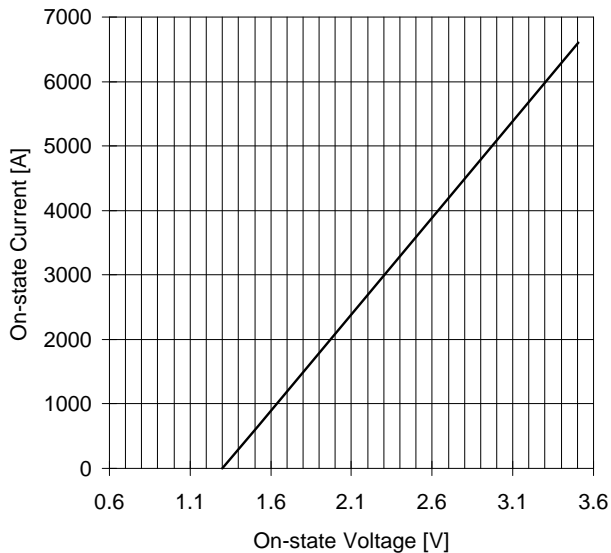


# AT875LT PHASE CONTROL THYRISTOR

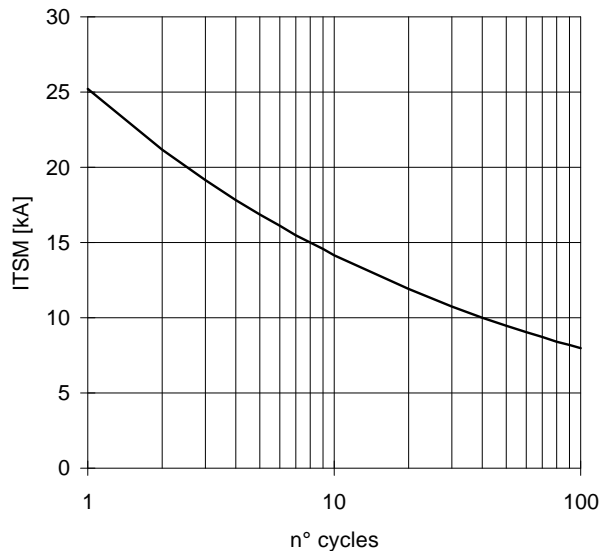
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FINAL SPECIFICATION apr 97 - ISSUE : 01

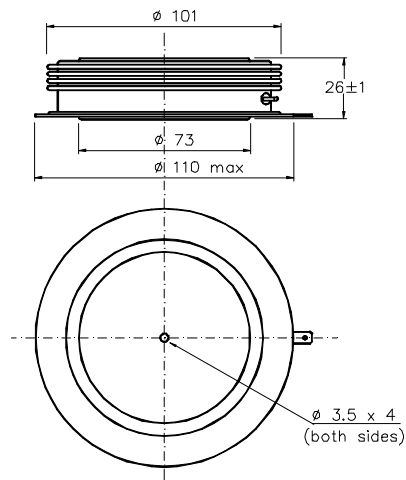
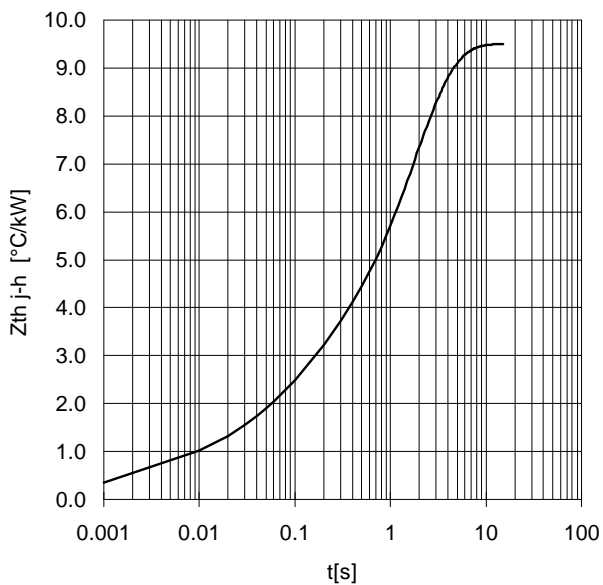
ON-STATE CHARACTERISTIC  
T<sub>j</sub> = 120 °C



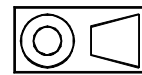
SURGE CHARACTERISTIC  
T<sub>j</sub> = 120 °C



TRANSIENT THERMAL IMPEDANCE  
DOUBLE SIDE COOLED



Dimensions  
in mm



Cathode terminal type DIN 46244 - A 4.8 - 0.8

Gate terminal type AMP 60598 - 1

All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 μm.

In the interest of product improvement ANSALDO reserves the right to change any data given in this data sheet at any time without previous notice.

If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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