

# System Reset Monolithic IC PST591 ~595 Series

## Outline

These ICs function in a variety of CPU systems and other logic systems, to detect power supply voltage and reset the system accurately when power is turned on or interrupted, and has a built-in fixed delay time generating circuit. This series has been represented in the past by PST574/PST575, but these new low reset type system reset ICs expand the delay time series with a counter timer using an analog/digital hybrid circuit.

## Features

- |   |  |   |
|---|--|---|
| 1. Fixed delay time setting by counter timer        | Excellent delay time temperature characteristics | ±800ppm/°C  |
| 2. Low operating limit voltage                      |  | 0.65V typ.  |
| 3. Hysteresis voltage provided in detection voltage |  | 50mV typ.   |
| 4. Current consumption for no-load                  |  | I <sub>CC</sub> L=300μA typ. I <sub>CC</sub> H=200μA typ.   |
| 5. 5 delay time products available                  |  | PST591 50mS      PST594 400mS<br>PST592 100mS    PST595 800mS<br>PST593 200mS   |
| 6. Each product has 9 detection voltage ranks.      |  | C : 4.5V typ.      H : 3.1V typ.<br>D : 4.2V typ.      I : 2.9V typ.<br>E : 3.9V typ.      J : 2.7V typ.<br>F : 3.6V typ.      K : 2.5V typ.<br>G : 3.3V typ. |

## Package

MMP-4A (PST59 × □ M)

TO-92A (PST59 × □)

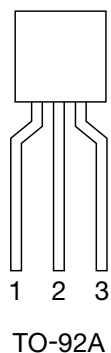
\*□ contains detection voltage rank.

(MMP-4A has a manual reset pin, which should be set at GND or NC during normal operation.)

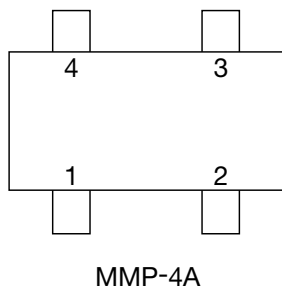
## Applications

1. Reset circuits in microcomputers, CPUs and MPUs
2. Logic circuit reset circuits.
3. Battery voltage check circuits.
4. Back-up power supply switching circuits.
5. Level detection circuits.
6. Mechanical reset circuits

### Pin Assignment

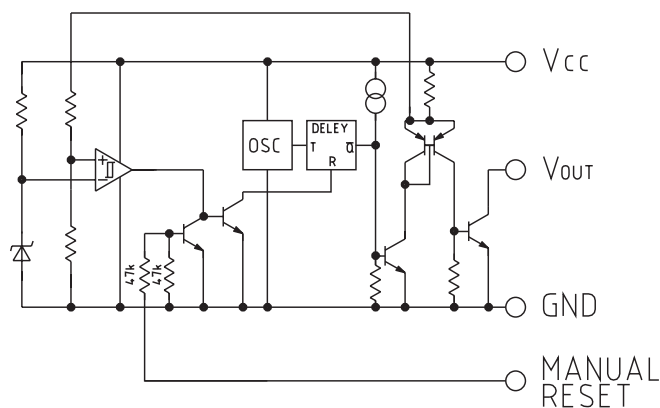


1	V <sub>CC</sub>
2	GND
3	V <sub>OUT</sub>



1	V <sub>OUT</sub>
2	Manual Reset
3	V <sub>CC</sub>
4	GND

### Equivalent Circuit Diagram



### Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Units
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Power supply voltage	V <sub>CC</sub> max.	-0.3~10	V
Manual reset input voltage	V <sub>RES</sub> max.	-0.3~10	V
Allowable loss	P <sub>d</sub>	200 (MMP-4P) 300 (TO-92)	mW

**Electrical Characteristics** (Ta=25°C) (Except where noted otherwise, resistance unit isΩ)

Item	Symbol	Measuring circuit	Measurement conditions	Min.	Typ.	Max.	Unit	
Detection voltage	Vs	1	R <sub>L</sub> =470 V <sub>OL</sub> ≤ 0.4V V <sub>CC</sub> =H→L	C	4.3	4.5	4.7	V
				D	4.0	4.2	4.4	
				E	3.7	3.9	4.1	
				F	3.4	3.6	3.8	
				G	3.1	3.3	3.5	
				H	2.9	3.1	3.3	
				I	2.75	2.90	3.05	
				J	2.55	2.70	2.85	
K	2.35	2.50	2.65					
Hysteresis voltage	ΔVs	1	R <sub>L</sub> =470, V <sub>CC</sub> =L→H→L	30	50	100	mV	
Detection voltage temperature coefficient	Vs/ΔT	1	R <sub>L</sub> =470, Ta=-20°C~+75°C		±0.01		%/°C	
Low-level output voltage	V <sub>OL</sub>	1	V <sub>CC</sub> =Vs min.-0.05V, R <sub>L</sub> =470		0.1	0.4	V	
Output leakage current	I <sub>OH</sub>	1	V <sub>CC</sub> =10V			±0.1	μA	
Circuit current while on	I <sub>CCL</sub>	1	V <sub>CC</sub> =Vs min.-0.05V, R <sub>L</sub> =∞		300	600	μA	
Circuit current while off	I <sub>CCH</sub>	1	V <sub>CC</sub> =Vs typ./0.85V, R <sub>L</sub> =∞		200	350	μA	
"H" transport delay time	t <sub>PLH</sub>	2	R <sub>L</sub> =4.7k C <sub>L</sub> =100PF *1	PST591	30	50	75	mS
				PST592	60	100	150	
				PST593	120	200	300	
				PST594	240	400	600	
				PST595	480	800	1200	
"L" transport delay time	t <sub>PHL</sub>	2	R <sub>L</sub> =4.7k, C <sub>L</sub> =100PF *1		10		μS	
Operating power supply voltage	V <sub>OPL</sub>	1	R <sub>L</sub> =4.7k, V <sub>OL</sub> ≤ 0.4V		0.65	0.85	V	
Output current while on 1	I <sub>OL1</sub>	1	V <sub>CC</sub> =Vs min.-0.05V, R <sub>L</sub> =0	8			mA	
Output current while on 2	I <sub>OL2</sub>	1	Ta=-20°C~+75°C, R <sub>L</sub> =0 *2	6			mA	
Manual reset pin	Input high voltage	V <sub>RESH</sub>		2.0			V	
	Input high current	V <sub>RESH</sub>	V <sub>RES</sub> =2V			80	μA	
	Input low voltage	V <sub>RESL</sub>				0.8	V	

\*1 t<sub>PLH</sub> : V<sub>CC</sub>= (Vs typ.-0.4V) → (Vs typ.+0.4V), t<sub>PHL</sub> : V<sub>CC</sub>= (Vs typ.+0.4V) → (Vs typ.-0.4V)

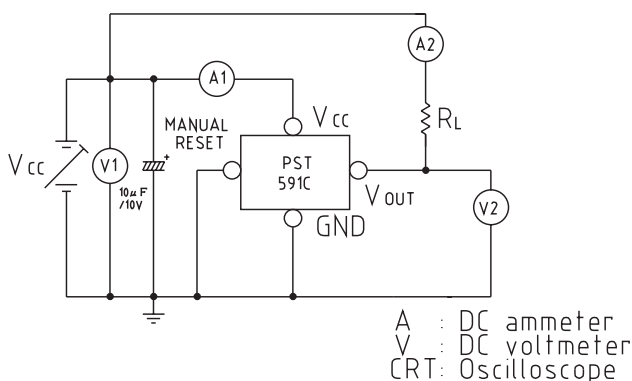
\*2 V<sub>CC</sub>=Vs min.-0.15V

Note 3: V<sub>OUT</sub> pin is low when manual reset pin is high.

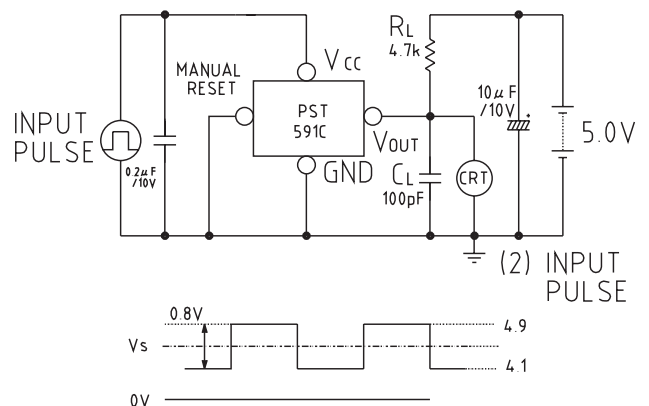
V<sub>OUT</sub> pin is high when manual reset pin is low.

**Measuring Circuit**

[1]



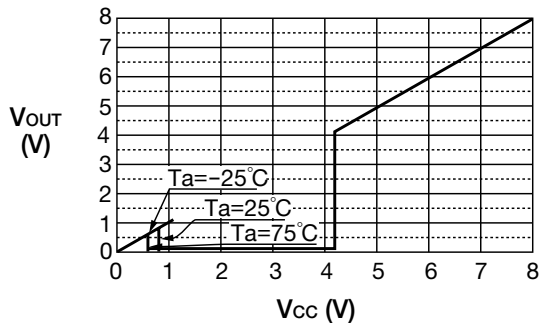
[2]



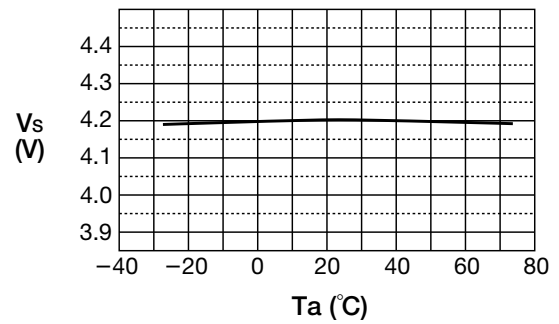
Note: Input model is an example for PST591C.

**Characteristics** (Example: PST591D)

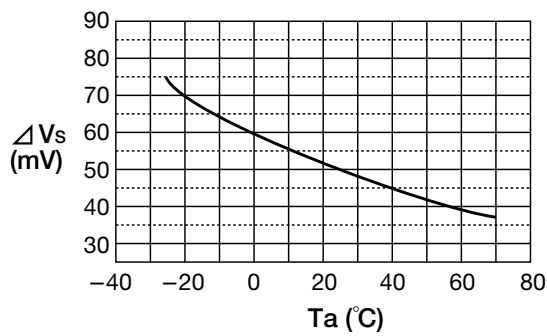
■ **V<sub>CC</sub> vs. V<sub>OUT</sub>**



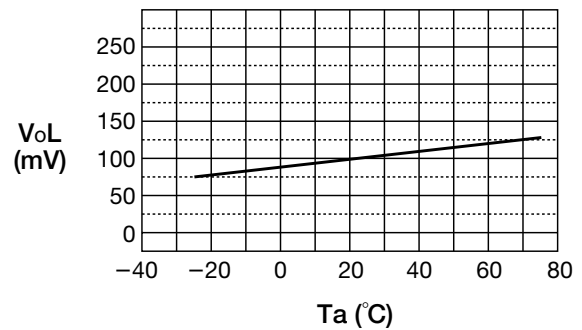
■ **V<sub>s</sub> vs. Ta**



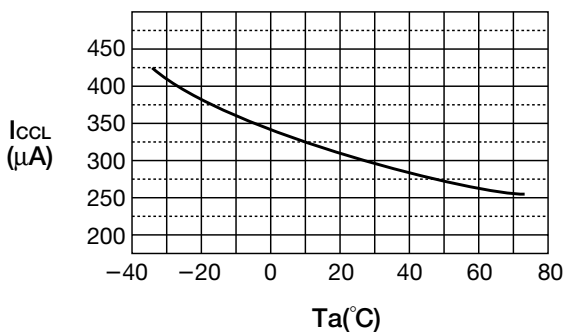
■ **ΔV<sub>s</sub> vs. Ta**



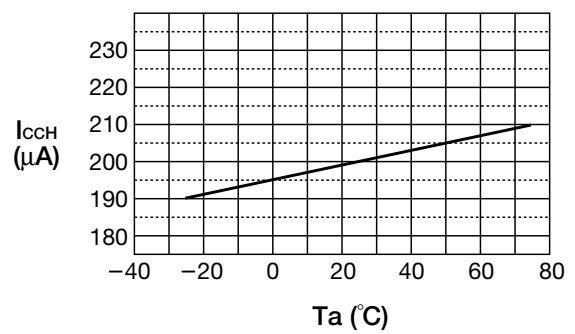
■ **V<sub>oL</sub> vs. Ta**



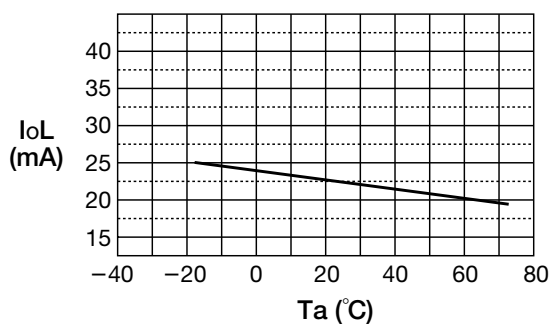
■ **I<sub>CC</sub>L vs. Ta**



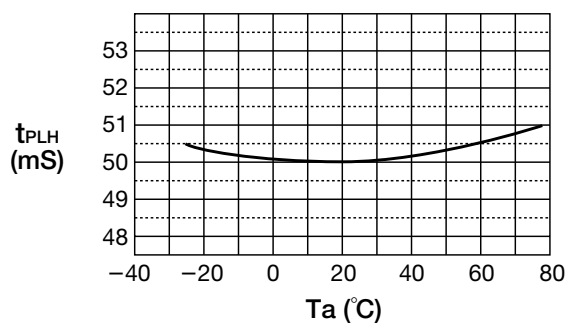
■ **I<sub>CC</sub>H vs. Ta**



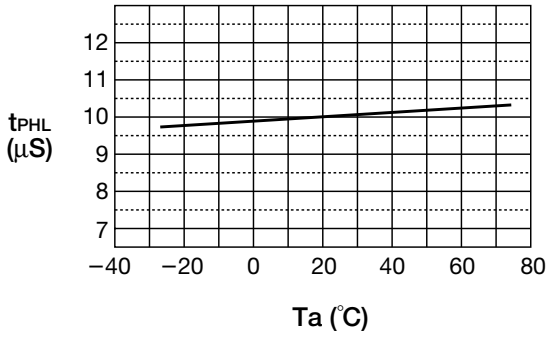
■ **I<sub>oL</sub> vs. Ta**



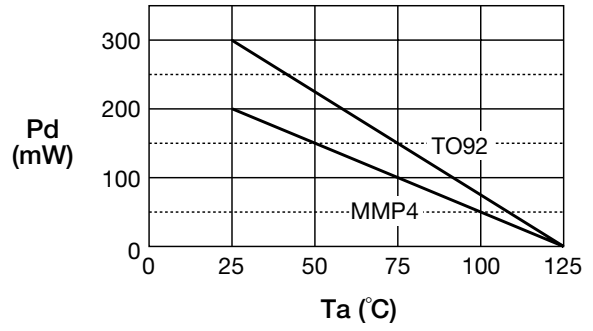
■ **t<sub>PLH</sub> vs. Ta**



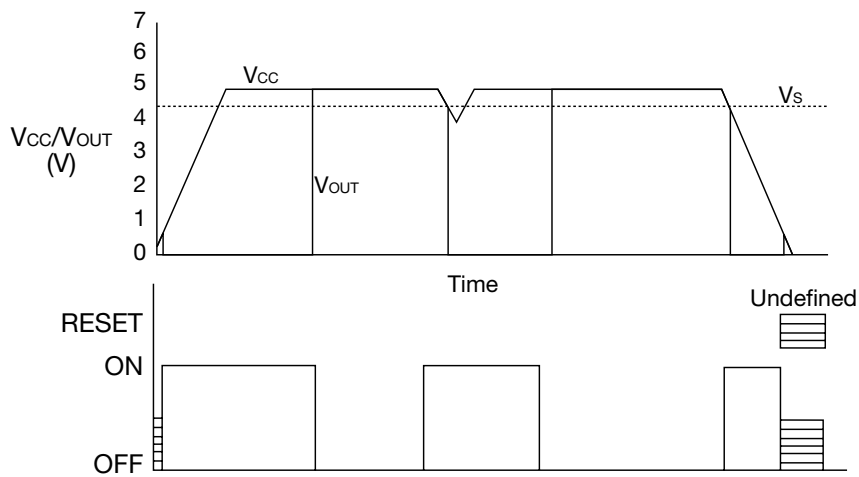
■ t<sub>PHL</sub> vs. Ta



■ Pd vs. Ta

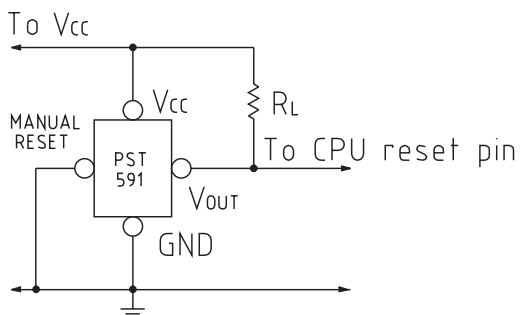


## Timing Chart



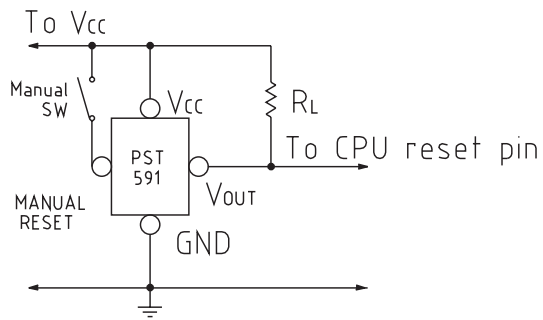
## Application circuits

### 1. Normal hard reset



Note: Connect a capacitor between IC  $V_{CC}$  and GND pins if  $V_{CC}$  line impedance is high.

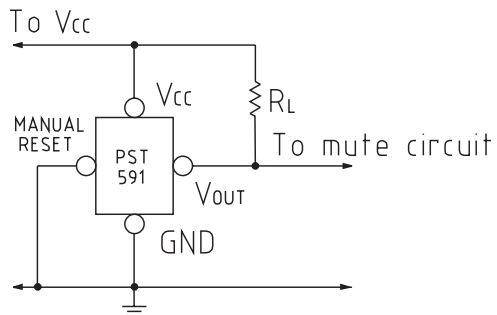
2. Manual reset



V<sub>OUT</sub> pin low for manual switch ON.  
 V<sub>OUT</sub> pin high for manual switch OFF.

Note: Connect a capacitor between IC V<sub>CC</sub> and GND pins if V<sub>CC</sub> line impedance is high.

3. Mute circuit



Note: Connect a capacitor between IC V<sub>CC</sub> and GND pins if V<sub>CC</sub> line impedance is high.