

DATA SHEET

74ABT16273
74ABTH16273
16-bit D-type flip-flop

Product specification
Supersedes data of 1995 Sep 28
IC23 Data Handbook

1998 Feb 27

16-bit D-type flip-flop

74ABT16273 74ABTH16273

FEATURES

- 16-bit D-type edge triggered flip-flops
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Live insertion/extraction permitted
- Power-up reset
- 74ABTH16273 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16273 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

This part is a 16-bit edge triggered D-type flip-flop with non-inverting high drive outputs. This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. When the clock (CP) goes High, the data on the D inputs is stored and the Q outputs display the stored data.

This device also features a master reset (\overline{MR}) that resets all flip-flops to the Low state when \overline{MR} is set to the Low state.

Two options are available, 74ABT16273 which does not have the bus-hold feature and 74ABTH16273 which incorporates the bus-hold feature.

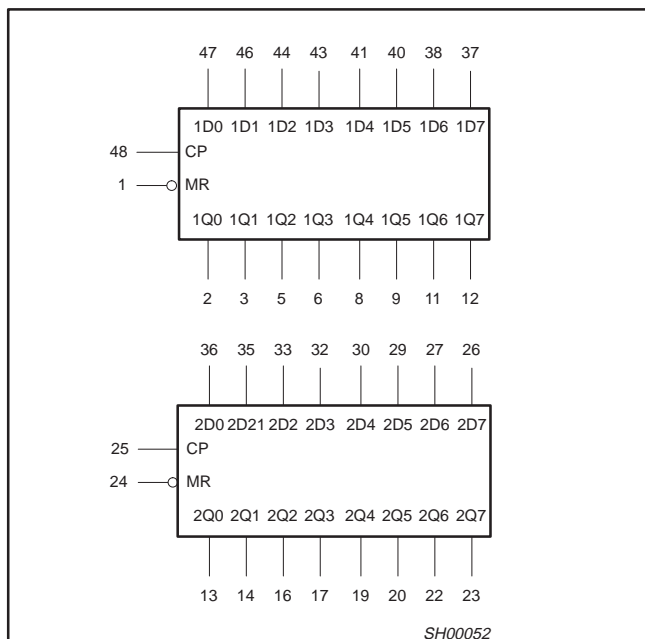
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF};$ $V_{CC} = 5.0\text{V}$	2.5 2.0	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
I_{CCH}	Quiescent supply current	Outputs High; $V_{CC} = 5.5\text{V}$	200	μA
I_{CCL}		Outputs low; $V_{CC} = 5.5\text{V}$	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABT16273 DL	BT16273 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABT16273 DGG	BT16273 DGG	SOT362-1
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABTH16273 DL	BH16273 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABTH16273 DGG	BH16273 DGG	SOT362-1

LOGIC SYMBOL



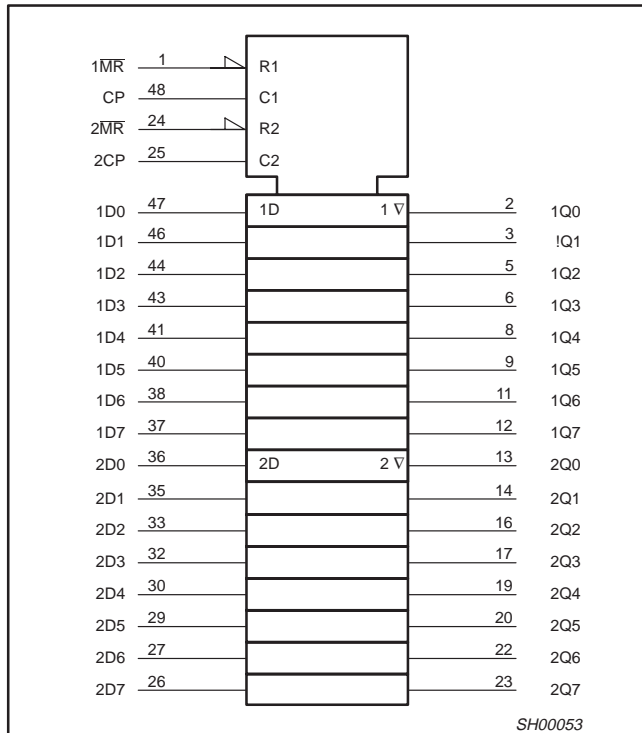
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	$1\overline{MR}, 2\overline{MR}$	Master reset input (active-Low)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0-1Q7 2Q0-2Q7	Data outputs
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0-1D7 2D0-2D7	Data inputs
25, 48	1CP, 2CP	Clock pulse input (active rising edge)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

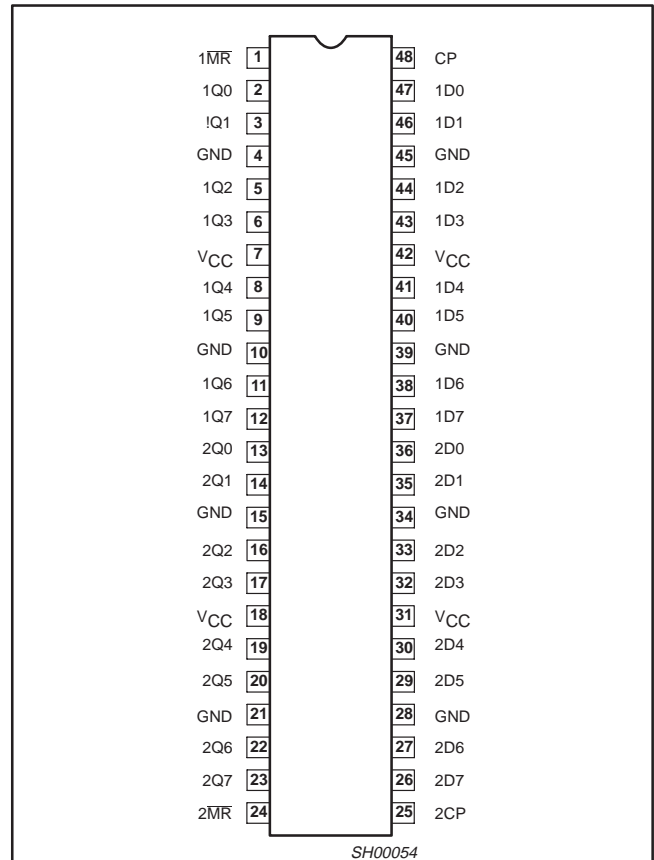
16-bit D-type flip-flop

74ABT16273
74ABTH16273

LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



FUNCTION TABLE

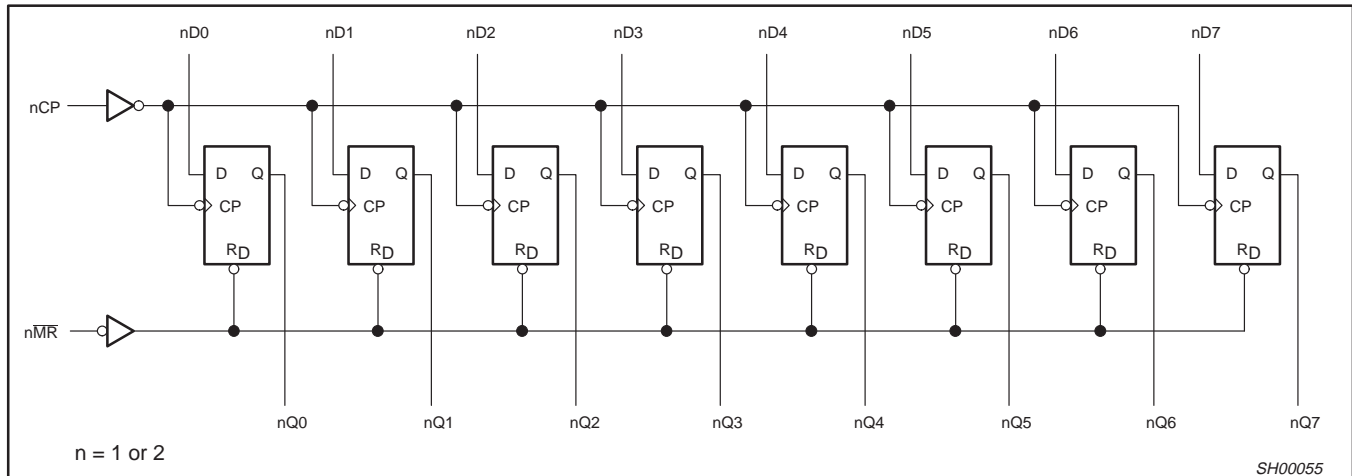
Inputs			Output	operating mode
nMR	nCP	nDX	nQ0-nQ7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"
H	L	X	Q ₀	Retain state

H = High voltage level
h = high voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Q₀ = Output as it was

16-bit D-type flip-flop

74ABT16273
74ABTH16273

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to -7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage ³		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

16-bit D-type flip-flop

74ABT16273
74ABTH16273

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			Temp = +25°C			Temp = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA		0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		
		V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	
V _{RST}	Power-up output voltage ³	V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current 74ABT16273	V _{CC} = 5.5V; V _I = V _{CC} or GND		±0.1	±1		±1	µA
I _I	Input leakage current 74ABTH16273	V _{CC} = 5.5V; V _I = V _{CC} or GND	Control pins	±0.01	±1		±1	µA
		V _{CC} = 5.5V; V _I = V _{CC}		0.01	1		1	µA
		V _{CC} = 5.5V; V _I = 0	Data pins	-2	-3		-5	µA
I _{HOLD}	Bus Hold current inputs ⁴ 74ABTH16273	V _{CC} = 4.5V; V _I = 0.8V	35			35		µA
		V _{CC} = 4.5V; V _I = 2.0V	-75			-75		
		V _{CC} = 5.5V; V _I = 0 to 5.5V	±800					
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _O or V _I < 4.5V		±5.0	±100		±100	µA
I _O	output current ¹	V _{CC} = 5.5V; V _O = 2.5V	-50	-70	-180	-50	-180	mA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	µA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.2	1		1	mA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		8	19		19	
ΔI _{CC}	Additional supply current per input pin ² 74ABT16273	V _{CC} = 5.5V; One input at 3.4V. Other inputs at V _{CC} or GND		5	100		100	µA
ΔI _{CC}	Additional supply current per input pin ² 74ABTH16273	V _{CC} = 5.5V; One input at 3.4V. Other inputs at V _{CC} or GND		0.2	1		1	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω;

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85 °C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	1.5 1.2	2.5 2.0	3.4 2.7	1.5 1.2	4.0 3.0	ns
t _{PHL}	Propagation delay nMR to nQx	2	1.9	3.7	4.3	1.9	5.3	ns
f _{MAX}	Maximum clock frequency	1	150	240		150		MHz

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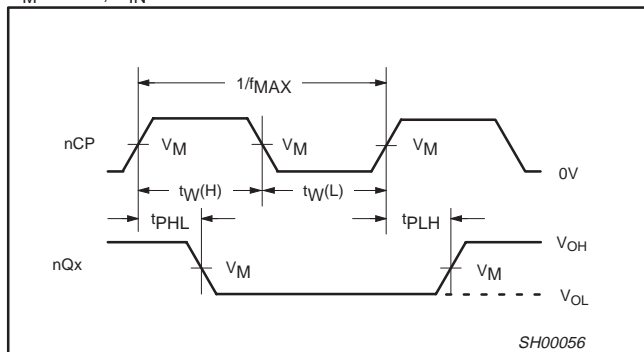
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$

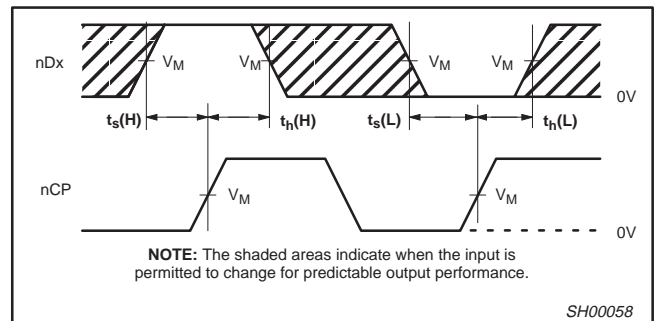
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time, High or Low nDx to nCP	3	2.0 2.0	1.0 1.0	2.0 2.0	ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold time, High or Low nDx to nCP	3	0 0	-0.6 -0.6	0 0	ns
$t_{\text{W}}(\text{H})$ $t_{\text{W}}(\text{L})$	Clock pulse width High or Low	1	3.3 3.3	1.2 1.0	3.3 3.3	ns
$t_{\text{W}}(\text{L})$	Master Reset pulse width, Low	2	3.3	1.1	3.3	ns
t_{REC}	Recovery time nMR + nCP	2	2.0	0.0	2.0	ns

AC WAVEFORMS

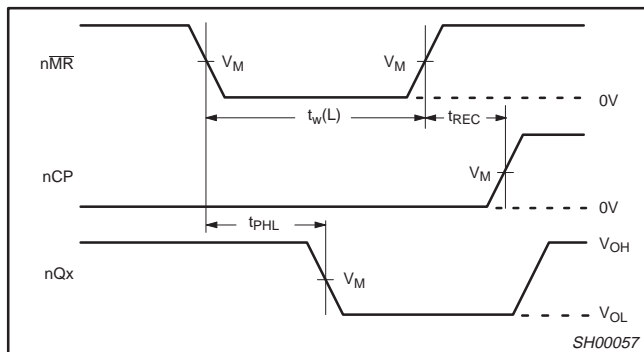
$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 2.7\text{V}$



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. Data Setup and Hold Times

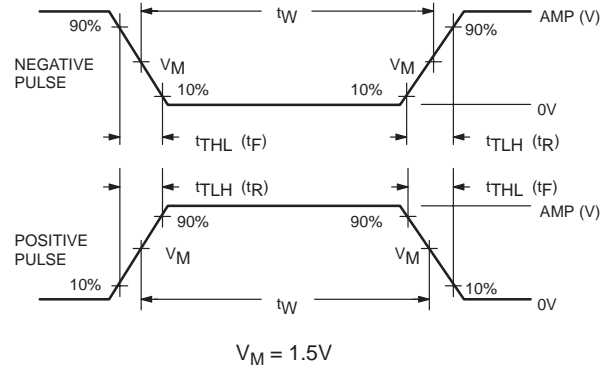
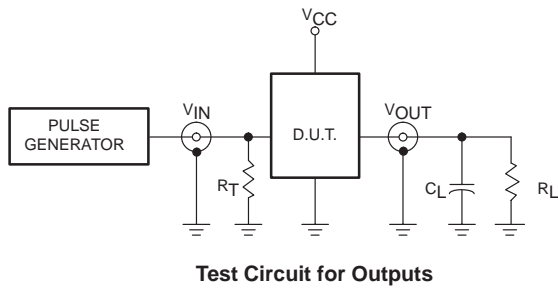


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

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74ABT16273
74ABTH16273

TEST CIRCUIT AND WAVEFORM



Input Pulse Definition

DEFINITIONS

- RL = Load resistor; see AC CHARACTERISTICS for value.
- CL = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- RT = Termination resistance should be equal to ZOUT of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t _W	t _R	t _F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

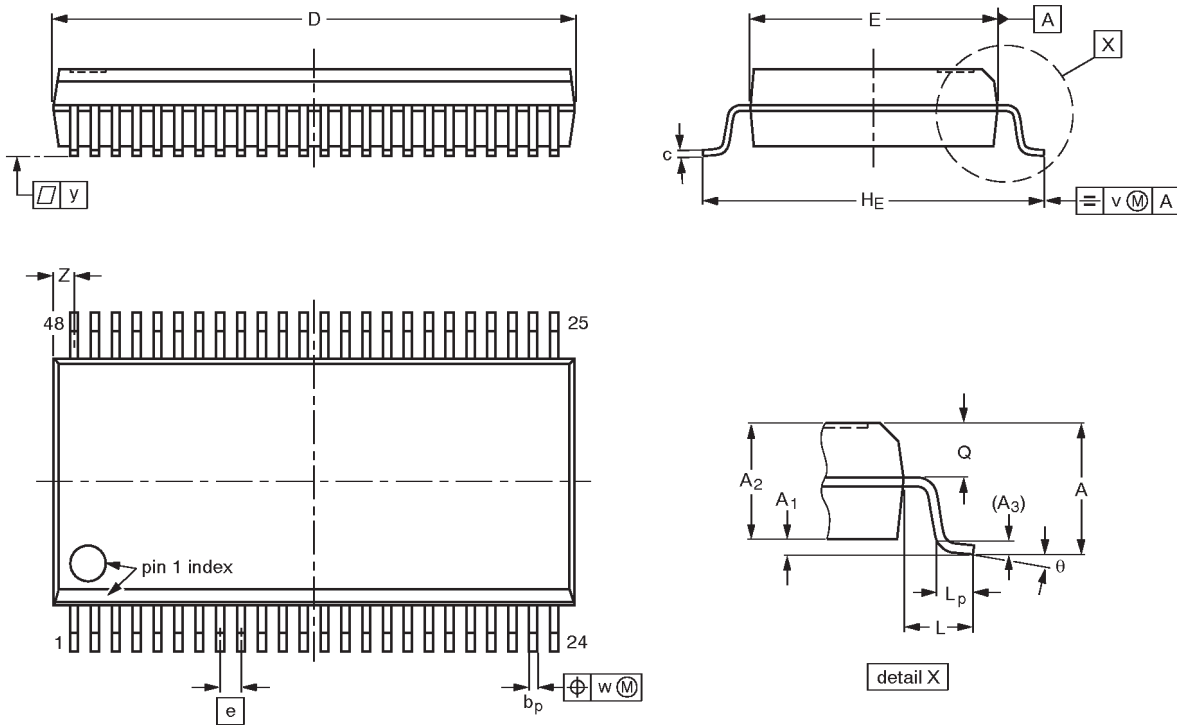
SH00059

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74ABT16273
74ABTH16273

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

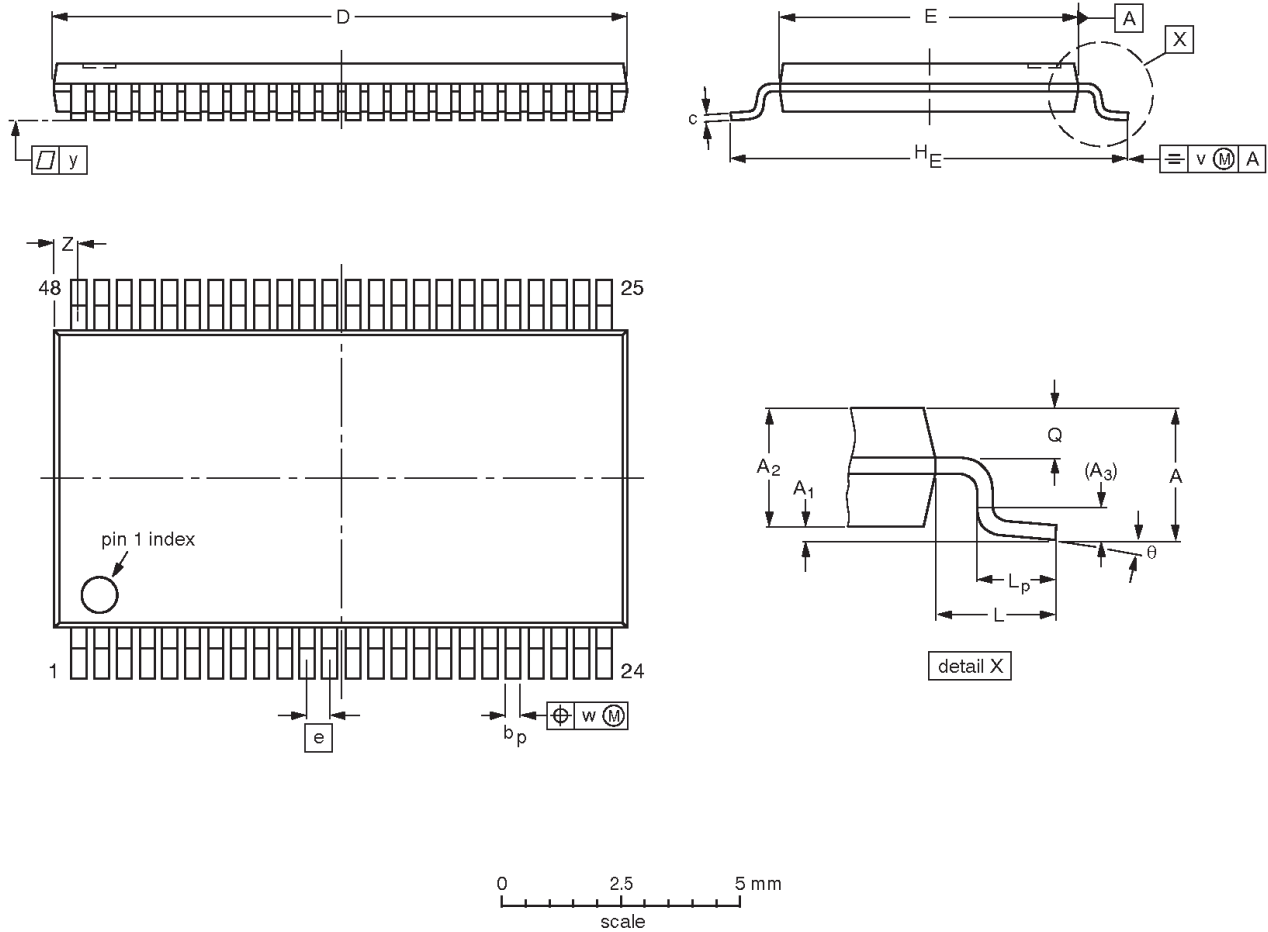
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				93-11-02- 95-02-04

16-bit D-type flip-flop

74ABT16273
74ABTH16273

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153ED				93-02-03 95-02-10

74ABT16273
74ABTH16273

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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