Ordering number : EN*5826

CMOS LSI

LC78632RE

Compact Disk Player DSP

Preliminary

Overview

The LC78632RE is a compact disc D/A signal-processing LSI for Video-CD players that provides a variable clock error correction (VCEC) mode. The LC78632RE demodulates the EFM signal from the optical pickup and performs de-interleaving, error detection, error correction, digital filtering, and other processing. The LC78632RE includes an on-chip 1-bit D/A converter, and executes commands sent from a control microprocessor.

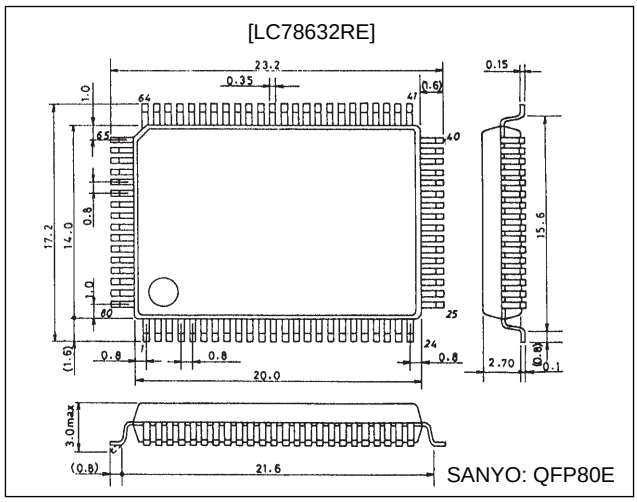
Features

- VCEC support
- Built-in PLL circuit for EFM detection (supports 4× playback)
- 18KB RAM on chip
- Error detection and correction (corrects two errors in C1 and four errors in C2)
- Frame jitter margin: ±8 frames
- Frame synchronization signal detection, protection, and insertion
- Dual interpolation adopted in the interpolation circuit.
- EFM data demodulation
- Subcode demodulation
- Zero-cross muting adopted
- Servo command interface
- 2fs digital filter
- Digital de-emphasis
- Built-in independent left- and right-channel digital attenuators (239 attenuation steps)
- Supports the bilingual function
- Left/right swap function
- Built-in 1-bit D/A converter (third-order ΔΣ noise shaper, PWM output)
- Built-in digital output circuit
- CLV servo
- Arbitrary track jumping (of up to 255 tracks)
- Variable sled voltage (four levels)
- Six extended I/O ports and 2 extended output ports
- Built-in oscillator circuit using an external 16.9344 MHz or 33.8688 MHz (for 4× playback) element
- Supply voltage: 4.5 to 5.5 V

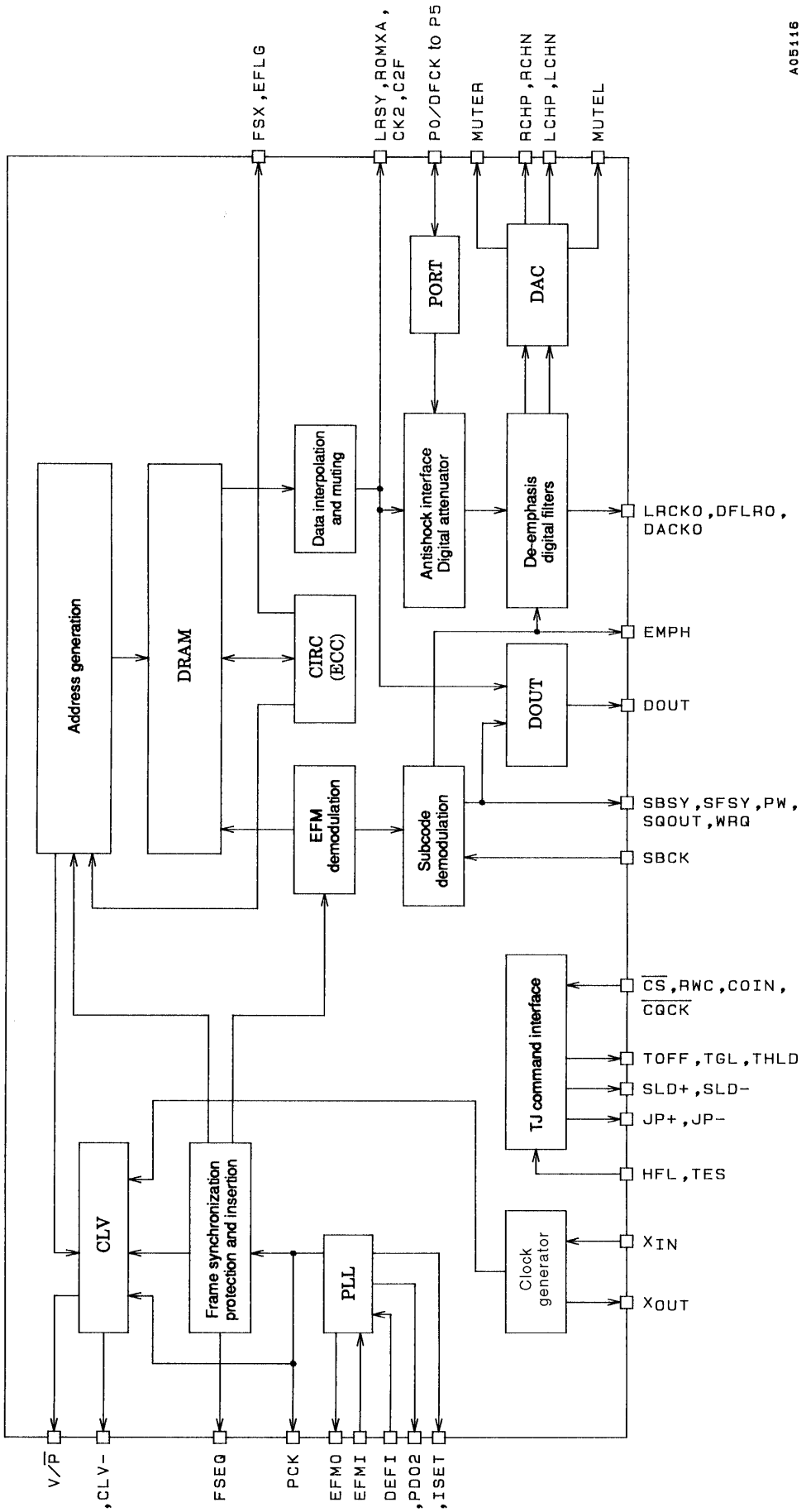
Package Dimensions

unit: mm

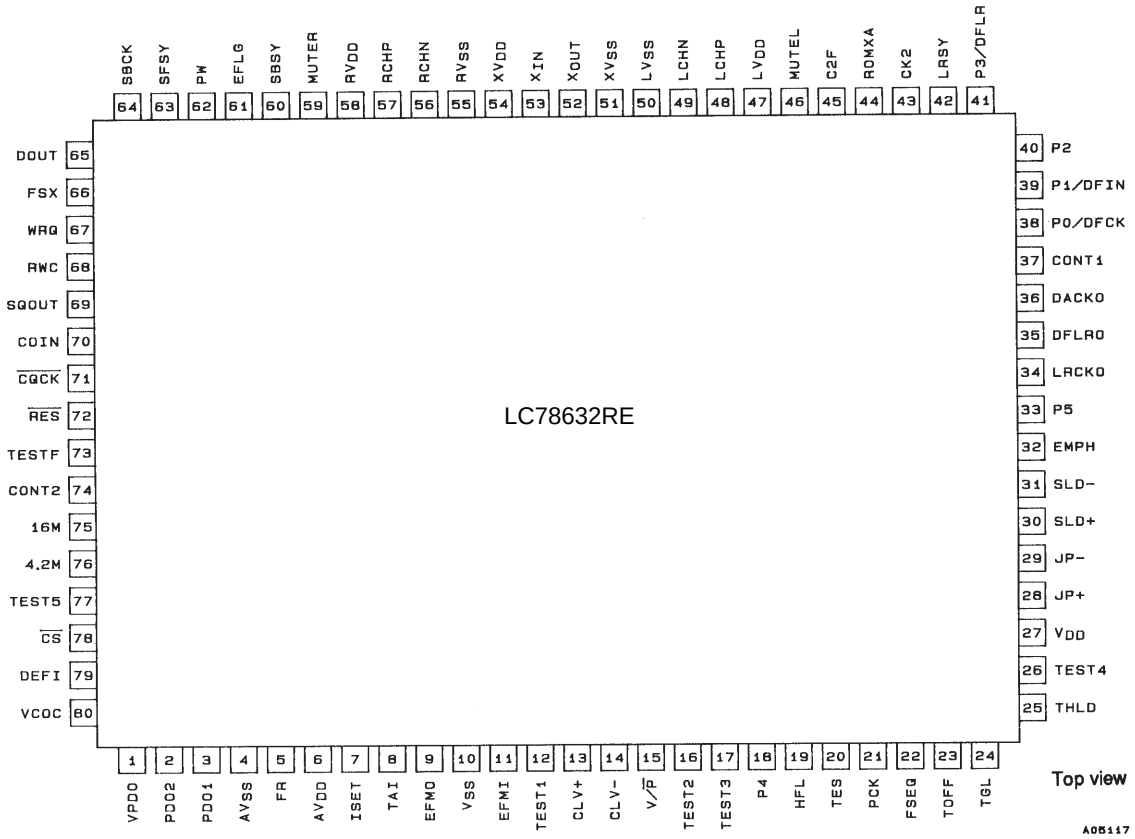
3174-QFP80E



Equivalent Circuit Block Diagram



Pin Assignment



Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		470	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	V_{DD}, AV_{DD}, XV_{DD}, LV_{DD}, RV_{DD}	4.5	5.0	5.5	V
Input high-level voltage	$V_{IH}1$	TEST1 to TEST5, TAI, HFL, TES, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5, SBCK, RWC, COIN, CQCK, RES, CS, X_{IN}, DEFI	0.7 V_{DD}		V_{DD}	V
	$V_{IH}2$	EFMI	0.6 V_{DD}		V_{DD}	V
Input low-level voltage	$V_{IL}1$	TEST1 to TEST5, TAI, HFL, TES, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5, SBCK, RWC, COIN, CQCK, RES, CS, X_{IN}, DEFI	0		0.3 V_{DD}	V
	$V_{IL}2$	EFMI	0		0.4 V_{DD}	V
Data setup time	t_{SU}	COIN, RWC: Figures 1 and 4	400			ns
	t_{PRS}	RWC: Figure 4	100			ns
Data hold time	t_{HD}	COIN, RWC: Figures 1 and 4	400			ns

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Parameter	Symbol	Conditions	min	typ	max	Unit
High-level clock pulse width	t_{WH}	SBCK, $\overline{CQCK}$: Figures 1, 2, 3, and 4	400			ns
Low-level clock pulse width	t_{WL}	SBCK, $\overline{CQCK}$: Figures 1, 2, 3, and 4	400			ns
Data read access time	t_{RAC}	SQOUT, PW: Figures 2, 3, and 4	0		400	ns
Command transfer time	t_{RWC}	RWC: Figures 1 and 4	1000			ns
Subcode Q read enable time	t_{SQE}	WRQ: Figure 2, with no RWC signal		11.2		ms
Subcode read cycle	t_{SC}	SFSY: Figure 3		136		µs
Subcode read enable	t_{SE}	SFSY: Figure 3	400			ns
Port output delay time	t_{PD}	CONT1, CONT2, P0 to P5: Figure 5			1200	ns
Input level	V_{EI}	EFMI	1.0			Vp-p
	V_{XI}	X_{IN}: Capacitance coupled input	1.0			Vp-p

Note: Due to the structure of this IC, the identical voltage must be applied to all power-supply pins.

Electrical Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I_{DD}	Normal-speed playback		30		mA
Input high-level current	$I_{IH}1$	EFMI, HFL, TES, SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{RES}$, DEFI: V_{IN} = 5 V			5	µA
	$I_{IH}2$	TAI, TEST1 to TEST5, $\overline{CS}$: V_{IN} = 5 V	25		75	µA
Input low-level current	I_{IL}	TAI, EFMI, HFL, TES, SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{RES}$, TEST1 to TEST5, $\overline{CS}$, DEFI: V_{IN} = 0 V	–5			µA
Output high-level voltage	$V_{OH}1$	EFMO, CLV^+, CLV^-, V/$\overline{P}$, PCK, FSEQ, TOFF, TGL, THLD, JP^+, JP^-, EMPH, EFLG, FSX I_{OH} = –1 mA	4			V
	$V_{OH}2$	MUTEL, MUTER, LRCKO, DFLRO, DACKO, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5, LRSY, CK2, ROMXA, C2F, SBSY, PW, SFSY, WRQ, SQOUT, 16M, 4.2M, CONT1, CONT2: I_{OH} = –0.5 mA	4			V
	$V_{OH}3$	VPDO: I_{OH} = –1 mA	4.5			V
	$V_{OH}4$	DOUT: I_{OH} = –12 mA	4.5			V
	$V_{OH}5$	LCHP, RCHP, LCHN, RCHN: I_{OH} = –1 mA	3.0		4.5	V
Output low-level voltage	$V_{OL}1$	EFMO, CLV^+, CLV^-, V/$\overline{P}$, PCK, FSEQ, TOFF, TGL, THLD, JP^+, JP^-, EMPH, EFLG, FSX I_{OL} = 1 mA			1	V
	$V_{OL}2$	MUTEL, MUTER, LRCKO, DFLRO, DACKO, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5, LRSY, CK2, ROMXA, C2F, SBSY, PW, SFSY, WRQ, SQOUT, 16M, 4.2M, CONT1, CONT2: I_{OL} = 2 mA			0.4	V
	$V_{OL}3$	VPDO: I_{OL} = 1 mA			0.5	V
	$V_{OL}4$	DOUT: I_{OL} = 12 mA			0.5	V
	$V_{OL}5$	LCHP, RCHP, LCHN, RCHN: I_{OL} = 1 mA	0.5		2.0	V
Output off leakage current	$I_{OFF}1$	PDO1, PDO2, VPDO, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5: V_{OUT} = 5 V			5	µA
	$I_{OFF}2$	PDO1, PDO2, VPDO, P0/DFCK, P1/DFIN, P2, P3/DFLR, P4, P5: V_{OUT} = 0 V	–5			µA
Charge pump output current	I_{PDOH}	PDO1, PDO2: R_{ISET} = 68 kΩ	–96	–80	–64	µA
	I_{PDOL}	PDO1, PDO2: R_{ISET} = 68 kΩ	64	80	96	µA
Sled output voltage	$V_{SLD}1$		1.0	1.25	1.5	V
	$V_{SLD}2$		2.25	2.5	2.75	V
	$V_{SLD}3$		3.5	3.75	4.0	V
	$V_{SLD}4$		4.75			V

D/A Converter Analog Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Total harmonic distortion	THD + N	LCHP, LCHN, RCHP, RCHN; 1 kHz: 0 dB input, using a 20-kHz low-pass filter (AD725D built in)		0.006		%
Dynamic range	DR	LCHP, LCHN, RCHP, RCHN; 1 kHz: –60 dB input, using the 20-kHz low-pass filter (A filter (AD725D built in))		90		dB
Signal-to-noise ratio	S/N	LCHP, LCHN, RCHP, RCHN; 1 kHz: 0 dB input, using the 20-kHz low-pass filter (A filter (AD725D built in))	98	100		dB
Crosstalk	CT	LCHP, LCHN, RCHP, RCHN; 1 kHz: 0 dB input, using a 20-kHz low-pass filter (AD725D built in)	96	98		dB

Note: Measured in normal-speed playback mode in a Sanyo 1-bit D/A converter block reference circuit, with the digital attenuator set to EE (hexadecimal).

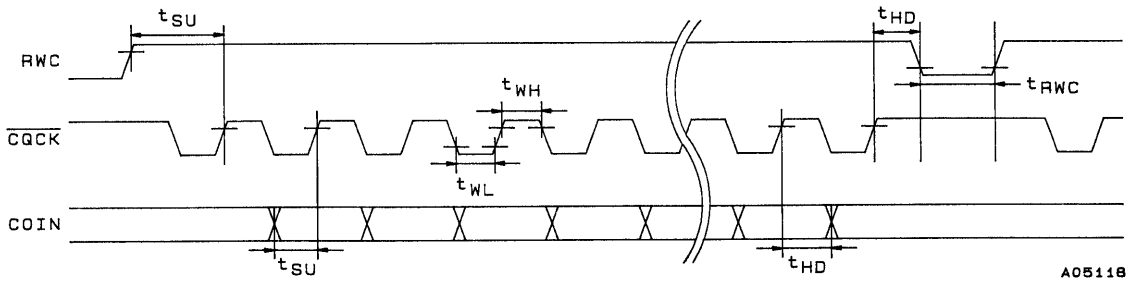


Figure 1 Command Input

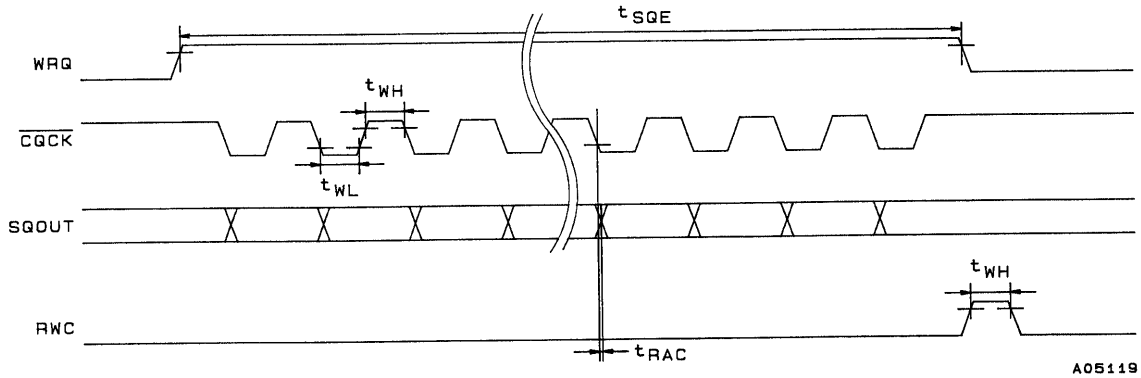


Figure 2 Subcode Q Output

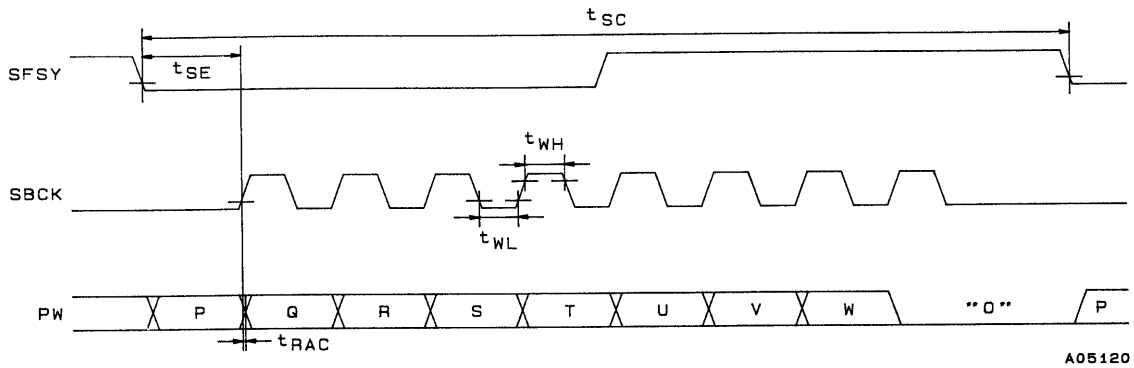


Figure 3 Subcode Output

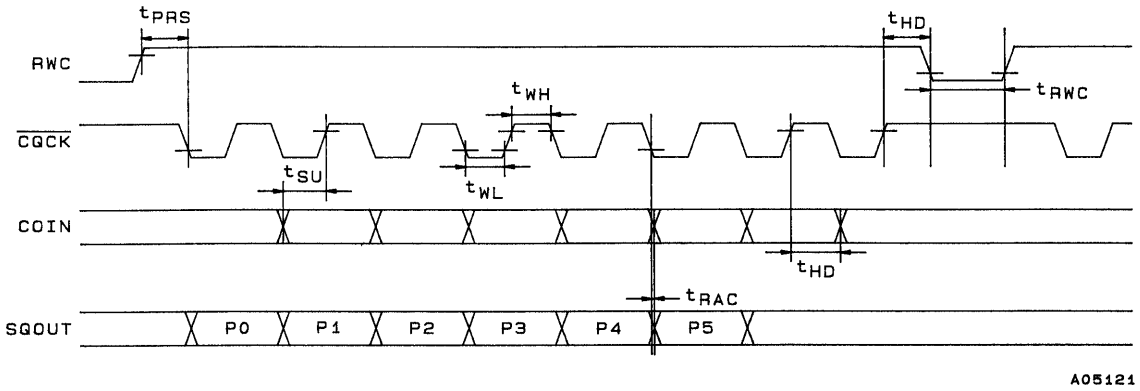


Figure 4 General-Purpose Port Read

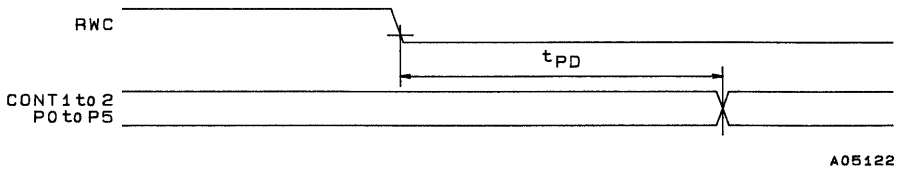
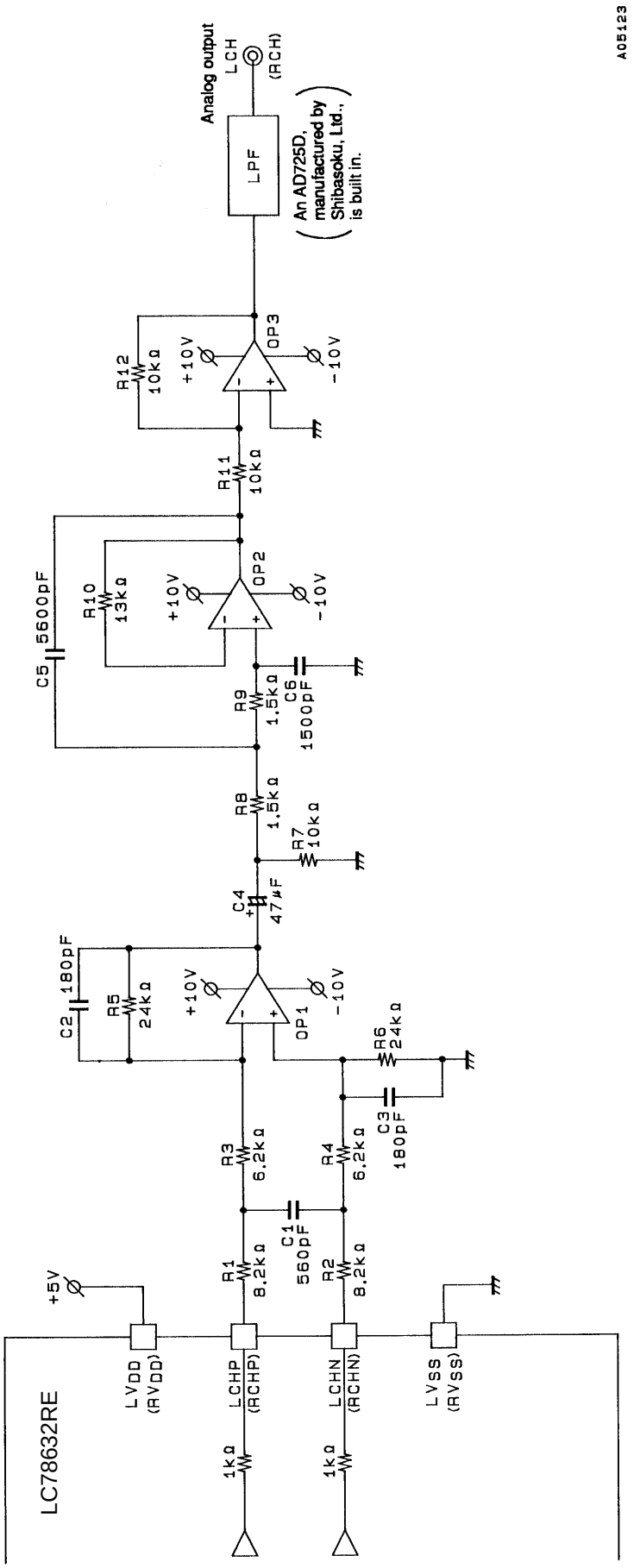


Figure 5 General-Purpose Port Output

One-Bit D/A Converter Output Block Reference Circuit



Pin Functions

Pin No.	Symbol	I/O	Function	
1	VPDO	O	Test output	
2	PDO2	O	Double-speed and quad-speed mode playback PLL charge pump output. Must be left open if unused.	
3	PDO1	O	Normal-speed mode playback PLL charge pump output	
4	AV_{SS}		Analog system ground. Must be connected to 0 V.	
5	FR		Built-in VCO frequency range setting resistor connection	
6	AV_{DD}		Analog system power supply	
7	ISET		PDO1 and PDO2 output current setting resistor connection	
8	TAI	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
9	EFMO	O	EFM signal output	
10	V_{SS}		Digital system ground. Must be connected to 0 V.	
11	EFMI	I	EFM signal input	
12	TEST1	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
13	CLV^+	O	Spindle servo control output. CLV^+ outputs a high level for acceleration, and CLV^- outputs a high level for deceleration.	
14	CLV^-	O		
15	$V/\overline{P}$	O	Rough servo/phase control automatic switching monitor output. A high-level output indicates rough servo, and a low-level output indicates phase control.	
16	TEST2	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
17	TEST3	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
18	P4	I/O	I/O port	
19	HFL	I	Track detection signal input. This is a Schmitt input.	
20	TES	I	Tracking error signal input. This is a Schmitt input.	
21	PCK	O	EFM data playback bit clock monitor. Outputs 4.3218 MHz when the phase is locked in normal-speed mode playback.	
22	FSEQ	O	Synchronization signal detection output. Outputs a high level when the synchronization signal detected from the EFM signal matches the internally generated synchronization signal.	
23	TOFF	O	Tracking off output	
24	TGL	O	Tracking gain switching output. Increase the gain when this pin outputs a low level.	
25	THLD	O	Tracking hold output	
26	TEST4	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
27	V_{DD}		Digital system power supply	
28	JP^+	O	Track jump output. JP^+ outputs a high level both for acceleration during outward direction jumps and for deceleration during inward direction jumps. JP^- outputs a high level both for acceleration during inward direction jumps and for deceleration during outward direction jumps.	
29	JP^-	O		
30	SLD^+	O	Sled output. This pin can be set to 1 of 4 levels by commands sent from the system control microprocessor.	
31	SLD^-	O		
32	EMPH	O	De-emphasis monitor. A high level indicates that a disk requiring de-emphasis is being played.	
33	P5	I/O	I/O port	
34	LRCKO	O	Digital filter outputs	LR clock output
35	DFLRO	O		LR data output. The digital filter can be turned off with the DFOFF command.
36	DACKO	O		Bit clock output
37	CONT1	O	Output port	
38	P0/DFCK	I/O	I/O port. DF bit clock input in antishock mode.	
39	P1/DFIN	I/O	I/O port. DF data input in antishock mode.	
40	P2	I/O	I/O port. Used as the de-emphasis filter on/off switching pin in antishock mode. The de-emphasis filter is turned on when this pin is high.	
41	P3/DFLR	I/O	I/O port output or digital filter LR clock input (when anti-shock mode)	
42	LRSY	O	ROMXA pins	LR clock output
43	CK2	O		Bit clock output. The polarity can be inverted with the CK2CON command.
44	ROMXA	O		Interpolated data output. Data that has not been interpolated can be output by issuing the ROMXA command.
45	C2F	O		C2 flag output
46	MUTEL	O	One-bit D/A converter pins	Left channel mute output
47	LV_{DD}			Left channel power supply
48	LCHP	O		Left channel P output
49	LCHN	O		Left channel N output
50	LV_{SS}			Left channel ground. Must be connected to 0V.

Note: Of the general-purpose I/O ports, any unused input ports must be connected to 0 V, or set to be output ports.

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Pin No.	Symbol	I/O	Function	
51	XV_{SS}		Crystal oscillator ground. Must be connected to 0 V.	
52	X_{OUT}	O	16.9344 MHz crystal oscillator connections. Use a 33.8688 MHz crystal oscillator for quad-speed playback.	
53	X_{IN}	I		
54	XV_{DD}		Crystal oscillator power supply	
55	RV_{SS}		One-bit D/A converter pins	Right channel ground. Must be connected to 0 V.
56	RCHN	O		Right channel N output
57	RCHP	O		Right channel P output
58	RV_{DD}			Right channel power supply
59	MUTER	O		Right channel mute output
60	SBSY	O	Subcode block synchronization signal output	
61	EFLG	O	C1 and C2 error correction state monitor	
62	PW	O	Subcode P, Q, R, S, T, U, V, and W output	
63	SFSY	O	Subcode frame synchronization signal output. Falls when the subcode output goes to the standby state.	
64	SBCK	I	Subcode readout clock input. This is a Schmitt input. This pin must be connected to 0 V if unused.	
65	DOUT	O	Digital output	
66	FSX	O	Outputs a 7.35 kHz synchronization signal generated by dividing the crystal oscillator frequency.	
67	WRQ	O	Subcode Q output standby output	
68	RWC	I	Read/write control input	
69	SQOUT	O	Subcode Q output	
70	COIN	I	Input for commands from the control microprocessor	
71	$\overline{CQCK}$	I	Command input acquisition clock. Also used as the SQOUT subcode readout clock input. This is a Schmitt input.	
72	$\overline{RES}$	I	Chip reset input. This pin must be set low temporarily when power is first applied.	
73	TESTF	O	Test output	
74	CONT2	O	Output port	
75	16M	O	16.9344 MHz output	
76	4.2M	O	4.2336 MHz output	
77	TEST5	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
78	$\overline{CS}$	I	Chip select input. A pull-down resistor is built in. When control is not used, this pin must be connected to 0 V.	
79	DEFI	I	Defect detection signal input. Must be connected to 0 V if unused.	
80	VCOC	I	Test input. Must be connected to 0 V.	

Note: Of the general-purpose I/O ports, any unused input ports must be connected to 0 V, or set to be output ports.