High Speed 8-Bit A/D Converter with Built-In Sample-and-Hold

FEATURES

- Built-In Sample-and-Hold
- No Missing Codes
- No User Trims Required
- All Timing Inputs Edge Sensitive for Easy Processor Interface
- Fast Conversion Time: 2.5μs
- Latched Three-State Outputs
- Single 5V Operation
- No External Clock
- Overflow Output Allows Cascading
- T_C Input Allows User Adjustable Conversion Time
- 0.3″ Wide 20-Pin DIP

KEY SPECIFICATIONS

■ Resolution	8 Bits
■ Conversion Time	2.5μs (RD Mode)
	2.5μs (WR-RD Mode)
■ Slew Rate Limit (Internal S/H)	2.5V/μs
■ Low Power	75mW Max
■ Total Unadjusted Error	
LTC1099	±1 LSB
LTC1099A	±1/2 LSB

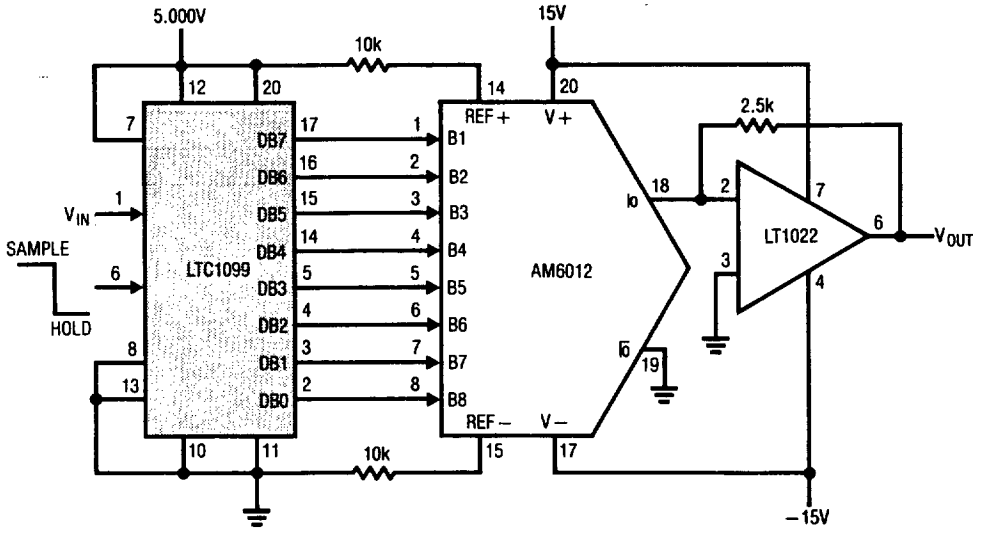
DESCRIPTION

The LTC1099 is a high speed microprocessor compatible 8-bit analog-to-digital converter (A/D). An internal sample-and-hold (S/H) allows the A/D to convert inputs up to the full Nyquist limit. With a conversion rate of 2.5μs this allows 156kHz 5Vp-p input signals, or slew rates as high as 2.5V/μs, to be digitized without the need for an external S/H.

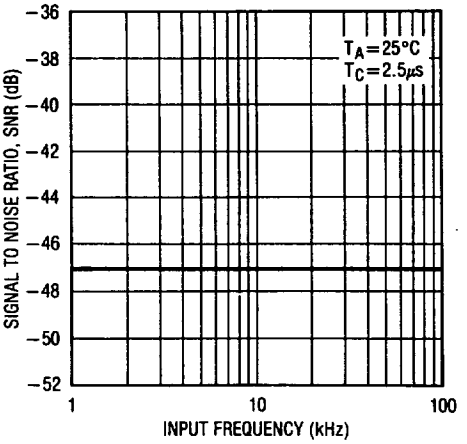
Two modes of operation, READ (RD) mode and WRITE-READ (WR-RD) mode, allow easy interface with processors. All timing is internal and edge sensitive which eliminates the need for external pulse shaping circuits. The Stand-Alone (SA) mode is convenient for those applications not involving a processor.

Data outputs are latched with three-state control to allow easy interface to a processor data bus or I/O port. An overflow output (OFL) is provided to allow cascading for higher resolution.

Infinite Hold Time Sample-and-Hold (T_{ACQ} = 240ns)



Signal to Noise Ratio (SNR) vs Input Frequency



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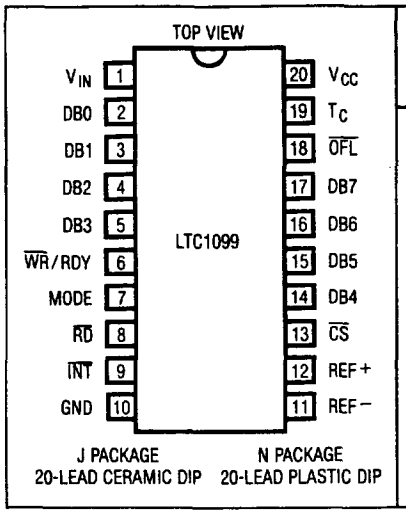
ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog and Reference Inputs ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs ..... −0.3V to 12V
  Digital Outputs ..... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1099C/1099AC ..... 0°C to 70°C
  LTC1099I/1099AI ..... −40°C to 85°C
  LTC1099M/1099AM ..... −55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
20-LEAD CERAMIC DIP

N PACKAGE
20-LEAD PLASTIC DIP

ORDER PART NUMBER
LTC1099CN
LTC1099ACN
LTC1099IN
LTC1099AIN
LTC1099IJ
LTC1099AIJ
LTC1099CJ
LTC1099ACJ
LTC1099MJ
LTC1099AMJ

CONVERTER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1099AI/1099I LTC1099AM/1099M MIN	TYP	MAX	LTC1099AC/1099C MIN	TYP	MAX	UNITS
Accuracy									
Total Unadjusted Error	Note 4								
LTC1099A		●			±1/2			±1/2	LSB
LTC1099		●			±1			±1	LSB
Minimum Resolution (No Missing Codes)		●	8			8			Bits
Reference Input									
Input Resistance		●	1	3.2	6	2	3.2	4.5	kΩ
REF+ Input Voltage Range	Note 5	●	REF−		V_{CC}	REF−		V_{CC}	V
REF− Input Voltage Range	Note 5	●	GND		REF+	GND		REF+	V
Analog Input									
Input Voltage Range		●	GND		V_{CC}	GND		V_{CC}	V
Input Leakage Current	$\overline{CS} = V_{CC}$, $V_{IN} = V_{CC}$, GND	●			±3			±3	μA
Input Capacitance				60			60		pF
Sample-and-Hold									
Acquisition Time				240			240		ns
Aperature Time				110			110		ns
Tracking Rate				2.5			2.5		V/μs

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1099AI/1099I LTC1099AM/1099M MIN	TYP	MAX	LTC1099AC/1099C MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	All Digital Inputs, V_{CC} = 5.25V	●	2.0			2.0			V
V_{IL}	Low Level Input Voltage	All Digital Inputs, V_{CC} = 4.75V	●			0.8		0.0001	0.8	V
I_{IH}	High Level Input Current	V_{IH} = 5V; $\overline{CS}$, $\overline{RD}$, Mode V_{IH} = 5V; $\overline{WR}$	● ●		0.0001 0.0005	1 3		0.0005	1 3	μA μA
I_{IL}	Low Level Input Current	V_{IL} = 0V; All Digital Inputs	●		−0.0001	−1		−0.0001	−1	μA
V_{OH}	High Level Output Voltage	DB0-DB7, $\overline{OFL}$, $\overline{INT}$; V_{CC} = 4.75V I_{OUT} = 360μA I_{OUT} = 10μA	●	2.4	4.0 4.7		2.4	4.0 4.7		V V
V_{OL}	Low Level Output Voltage	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY; V_{CC} = 4.75V I_{OUT} = 1.6mA	●			0.4			0.4	V
I_{OZ}	High-Z Output Leakage	DB0-DB7, RDY; V_{OUT} = 5V DB0-DB7, RDY; V_{OUT} = 0V	● ●		0.1 −0.1	3 −3		0.1 −0.1	3 −3	μA μA
I_{SOURCE}	Output Source Current	DB0-DB7, $\overline{OFL}$, $\overline{INT}$; V_{OUT} = 0V	●		−11	−6		−11	−7	mA
I_{SINK}	Output Sink Current	DB0-DB7, $\overline{OFL}$, $\overline{INT}$, RDY; V_{OUT} = 5V	●		14	7		14	9	mA
I_{CC}	Supply Current	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = V_{CC}	●		11	20		11	15	mA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1099AI/1099I LTC1099AM/1099M MIN	TYP	MAX	LTC1099AC/1099C MIN	TYP	MAX	UNITS
RD Mode (Figure 2) Pin 7 = GND										
t_{CRD}	Conversion Time	T_A = 25°C	 ●	2.3	2.5	2.8 5.0	2.3	2.5	2.8 3.75	μs μs
t_{RDY}	Delay From $\overline{CS}$↓ to RDY↓	C_L = 100pF			70			70		ns
t_{ACC0}	Delay From $\overline{RD}$↓ to Output Data Valid	C_L = 100pF			t_{CRD} + 35			t_{CRD} + 35		ns
t_{INTH}	Delay From $\overline{RD}$↑ to $\overline{INT}$↑	C_L = 100pF			70			70		ns
t_{1H}, t_{0H}	Delay From $\overline{RD}$↑ to High-Z State on Outputs	Test Circuit Figure 1			70			70		ns
t_P	Delay Time Between Conversions				700			700		ns
t_{ACC2}	Delay Time From $\overline{RD}$↓ to Output Data Valid				70			70		ns
WR-RD Mode (Figures 3 and 4) Pin 7 = V_{CC}										
t_{CWR}	Conversion Time	T_A = 25°C	 ●	2.3	2.5	2.8 5.0	2.3	2.5	2.8 3.75	μs μs
t_{ACC0}	Delay Time From $\overline{WR}$↓ to Output Data Valid	C_L = 100pF			t_{CWR} + 40			t_{CWR} + 40		ns
t_{ACC2}	Delay From $\overline{RD}$↓ to Output Data Valid	C_L = 100pF			70			70		ns
t_{INTH}	Delay From $\overline{RD}$↑ to $\overline{INT}$↑	C_L = 100pF			70			70		ns
t_{IHWR}	Delay From $\overline{WR}$↓ to $\overline{INT}$↑	C_L = 100pF			240			240		ns
t_{1H}, t_{0H}	Delay From $\overline{RD}$↑ to High-Z State on Outputs	Test Circuit Figure 1			70			70		ns
t_P	Delay Time Between Conversions				700			700		ns
t_{WR}	Minimum $\overline{WR}$ Pulse Width				55			55		ns

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are with respect to GND (Pin 10) unless otherwise noted.

Note 3: V_{CC} = 5V, REF + = 5V, REF − = 0V and T_A = T_{MIN} to T_{MAX} unless otherwise noted. All typical values at T_A = 25°C. The ● indicates specifications which apply over the full operating temperature range.

Note 4: Total unadjusted error includes offset, gain, linearity and hold step errors.

Note 5: Reference input voltage range is guaranteed but is not tested.

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TEST CIRCUITS

t_{1H}
$t_r = 20ns, C_L = 10pF$

t_{0H}
$t_r = 20ns, C_L = 10pF$

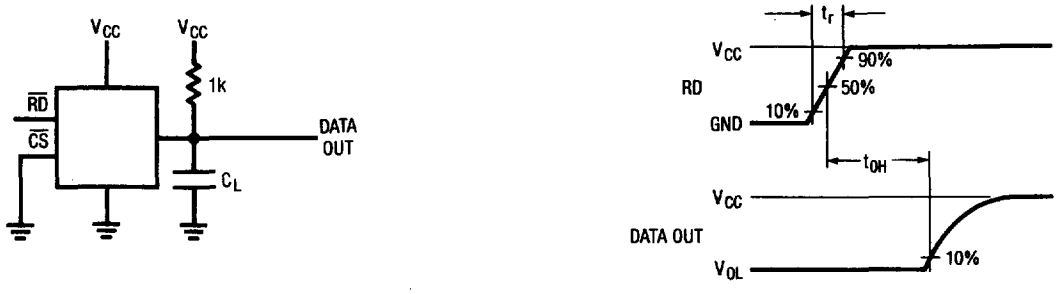

Figure 1. Three-State Test Circuit

TIMING DIAGRAMS

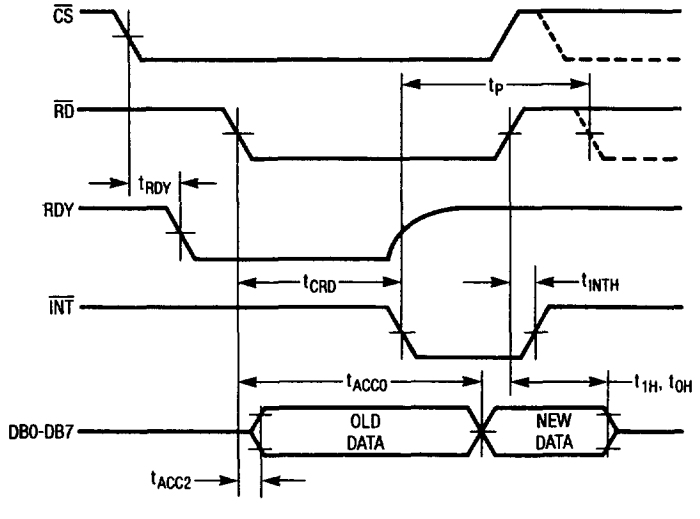

Figure 2. RD Mode (Pin 7 is GND)

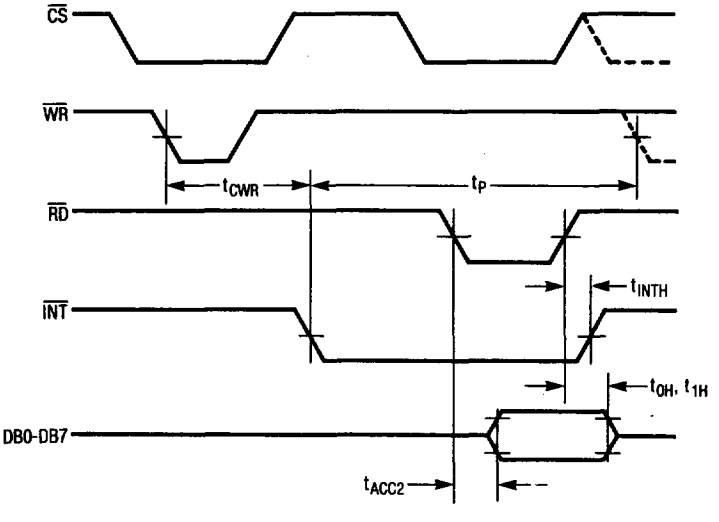

Figure 3A. WR-RD Mode (Pin 7 is HIGH and $t_{RD} > t_{CWR}$)

TIMING DIAGRAMS

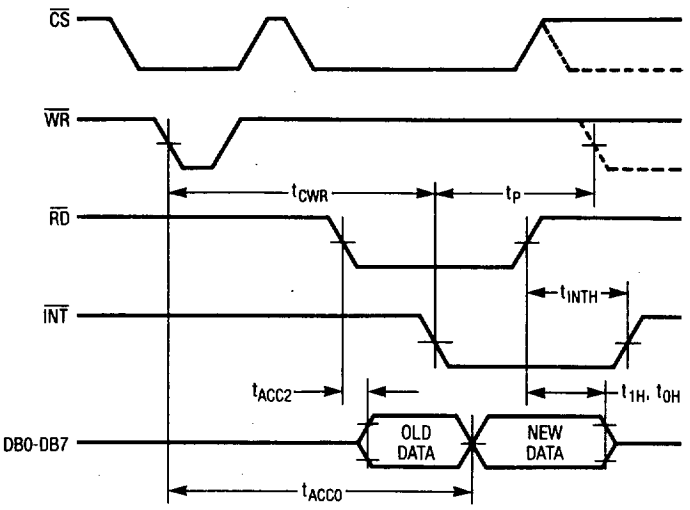

Figure 3B. WR-RD Mode (Pin 7 is HIGH and $t_{RD} < t_{CWR}$)

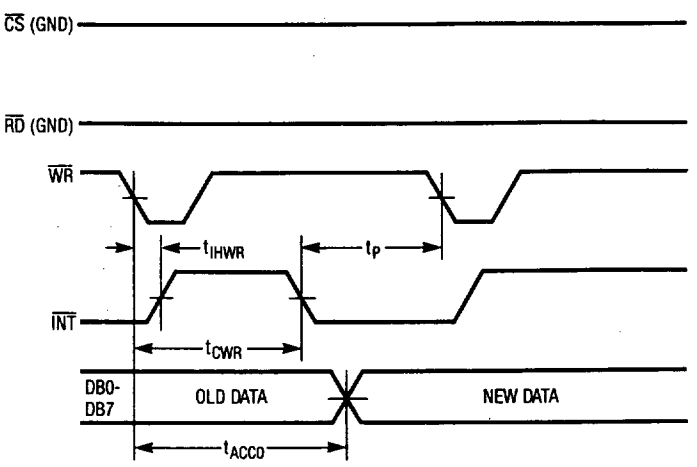

Figure 4. WR-RD Mode (Pin 7 is HIGH) Stand-Alone Operation

PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1	V_{IN}	Analog input.
2-5	DB0-DB3	Data outputs; DB0 = LSB.
6	$\overline{WR}$/RDY	$\overline{WR}$/RDY is an input when Mode = V_{CC}. Falling edge of $\overline{WR}$ switches internal S/H to hold then starts conversion. $\overline{WR}$/RDY is an open drain output (active pull down) when Mode = GND. RDY goes low at start of conversion and pull down is turned off when conversion is complete. Resistive pull up is usually used in this mode.
7	MODE	WR-RD when Mode = V_{CC}. RD when Mode = GND. No internal pull down.
8	$\overline{RD}$	A low on $\overline{RD}$ with $\overline{CS}$ low activates three-state outputs. With Mode = GND and $\overline{CS}$ low, the falling edge of $\overline{RD}$ switches internal S/H to hold and starts conversion.
9	$\overline{INT}$	Output that goes low when the conversion in process is complete and goes high after data is read.
10	GND	Ground connection.
11	REF–	Low reference potential (analog ground).
12	REF+	High reference potential; V_{REF} = Full Scale = (REF+) – (REF–).
13	$\overline{CS}$	Chip select — When high, data outputs are high impedance and all inputs are ignored.
14-17	DB4-DB7	Data outputs; DB7 = MSB.
18	$\overline{OFL}$	Overflow output — Goes low when $V_{IN} > V_{REF}$.
19	T_C	User adjustable conversion time.
20	V_{CC}	Positive supply; $4.75V \leq V_{CC} \leq 5.25V$.

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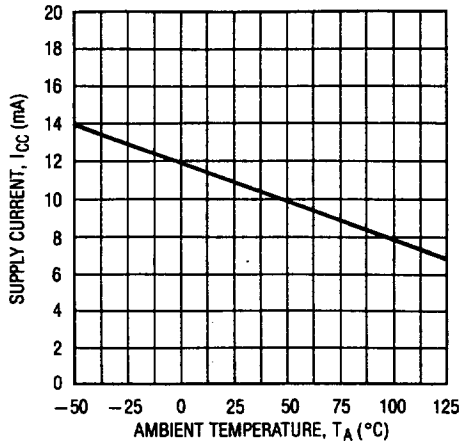
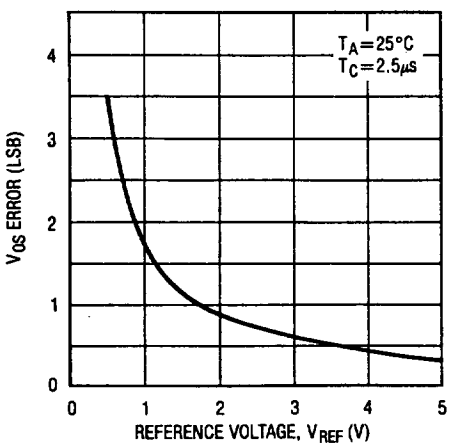
TYPICAL PERFORMANCE CHARACTERISTICS

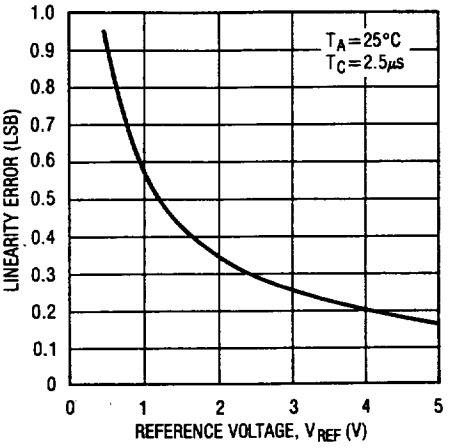
Supply Current vs Temperature



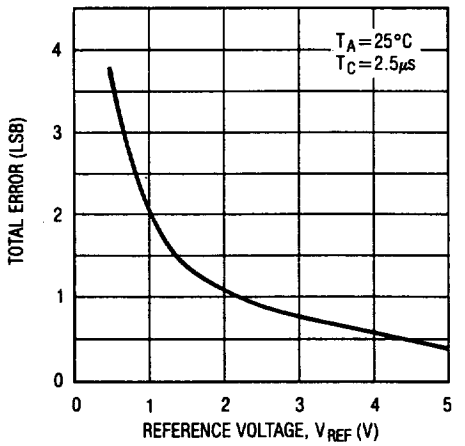
V_{OS} Error vs Reference Voltage



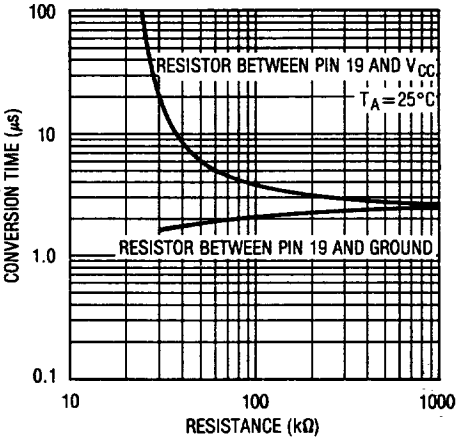
Linearity Error vs Reference Voltage



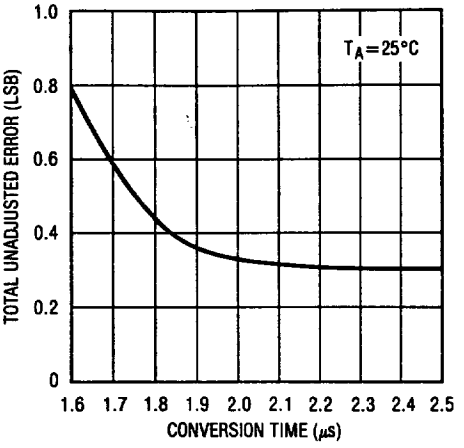
Total Error vs Reference Voltage



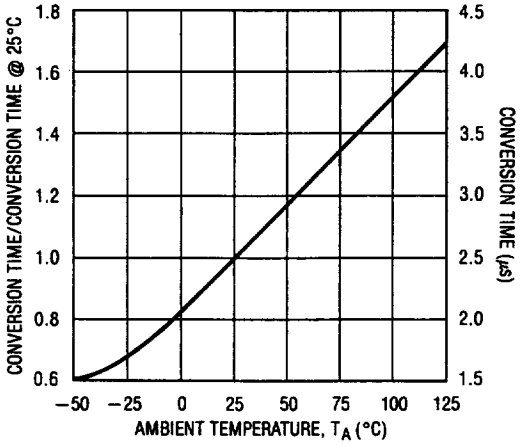
Conversion Time vs R_{EXT}



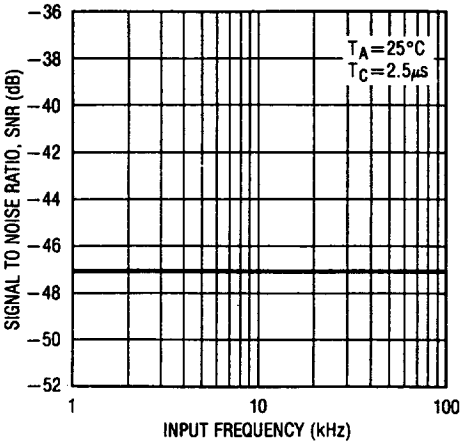
Accuracy vs Conversion Time



Conversion Time vs Temperature



Signal to Noise Ratio (SNR) vs Input Frequency



FUNCTIONAL DESCRIPTION

Figure 5 shows the functional block diagram for the LTC1099 two step flash ADC. It consists of two 4-bit flash converters, a 4-bit DAC and a differencing circuit. The conversion process proceeds as follows:

1) At the start of the conversion the on-board sample-and-hold switches from the sample to the hold mode. This is a true sample-and-hold with an acquisition time of 240ns, an aperture time of 110ns and a tracking rate of 2.5V/μs.

2) The held input voltage is converted by the 4-bit MS-Flash ADC. This generates the upper or most significant 4-bits of the 8-bit output.

3) A 4-bit approximation, from the DAC output, is subtracted from the held input voltage.

4) The LS-Flash ADC converts the difference between the held input voltage and the DAC approximation. This generates the lower or least significant 4-bits of the 8-bit output. The LS-Flash reference is one sixteenth of the MS-Flash reference. This effectively multiplies the difference by 16.

5) Upon the completion of the LS 4-bit flash the eight output latches are updated simultaneously. At the same time the sample-and-hold is switched from the the hold mode to the acquire mode in preparation for the next conversion.

The advantage of this approach is the reduction in the amount of hardware required. A full flash converter requires 255 comparators while this approach requires only 31. The price paid for this reduction in hardware is an increase in conversion time. A full flash converter requires only one comparison cycle while this approach requires two comparison cycles, hence two step flash.

This architecture is further simplified in the LTC1099 by reusing the MS-Flash hardware to do the LS-Flash. This reduces the number of comparators from 31 to 16. This is possible because the MS and LS conversions are done at different times.

To take the simple block diagram of Figure 5 and reconfigure it to reuse the MS-Flash to do the LS-Flash is conceptually simple, but from a hardware point of view is not practical. A new six input switched capacitor comparator is used to accomplish this function in a simple, although not straightforward, manner.

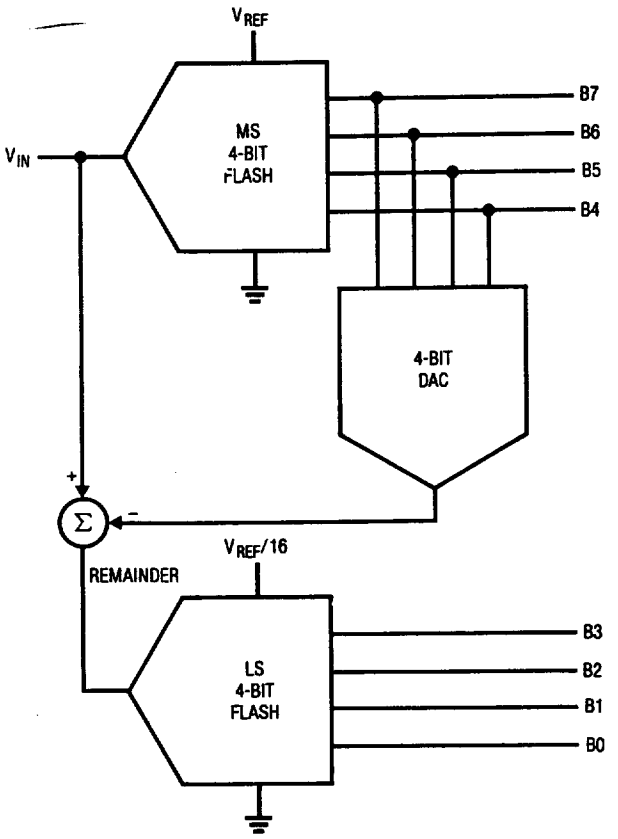


Figure 5. 8-Bit Two-Step Semiflash A/D

Figure 6 shows the six input switched capacitor comparator. Intuitively the comparator is easy to understand by noting that the common connection between the two input capacitors, C1 and C2, acts like a virtual ground. In operational amplifier circuits, current is summed at the virtual ground node. Input voltage is converted to current by the input resistors. In the switched capacitor comparator, input voltage is converted to charge by the input capacitors and these charges are summed at the virtual ground node.

FUNCTIONAL DESCRIPTION

A major advantage of this technique is that the switch-on impedance has no affect on accuracy as long as sufficient time exists to fully charge and discharge the capacitors.

During the first time period the T+ and T_Z switches are closed. This forces the common node between C1 and C2 to an arbitrary bias voltage. Since the capacitors subtract out this voltage it may be considered, for the sake of this discussion, to be exactly zero (i.e. virtual ground). Note also that variations in the bias voltage with time and temperature will also be rejected. In this state C1 charges to V_{IN}. When T_Z opens V_{IN} is held on C1.

The next step is the first comparison — the MS-Flash. T_Z and T+ are opened and T_{-1} is closed. The equation for each comparator is:

$$V_{IN} + 1/2LSB - MS_{TAP} = 0V$$

There are 16 identical comparators each tied to the tap on a 16 resistor ladder. The MS tap voltages vary from V_{REF} to 0V in 16 equal steps of $V_{REF}/16$.

Notice that capacitor C2 adds 1/2LSB to V_{IN}. This offsets the converter transfer function by 1/2LSB, equally distributing the 1LSB quantization error to ± 1/2LSB.

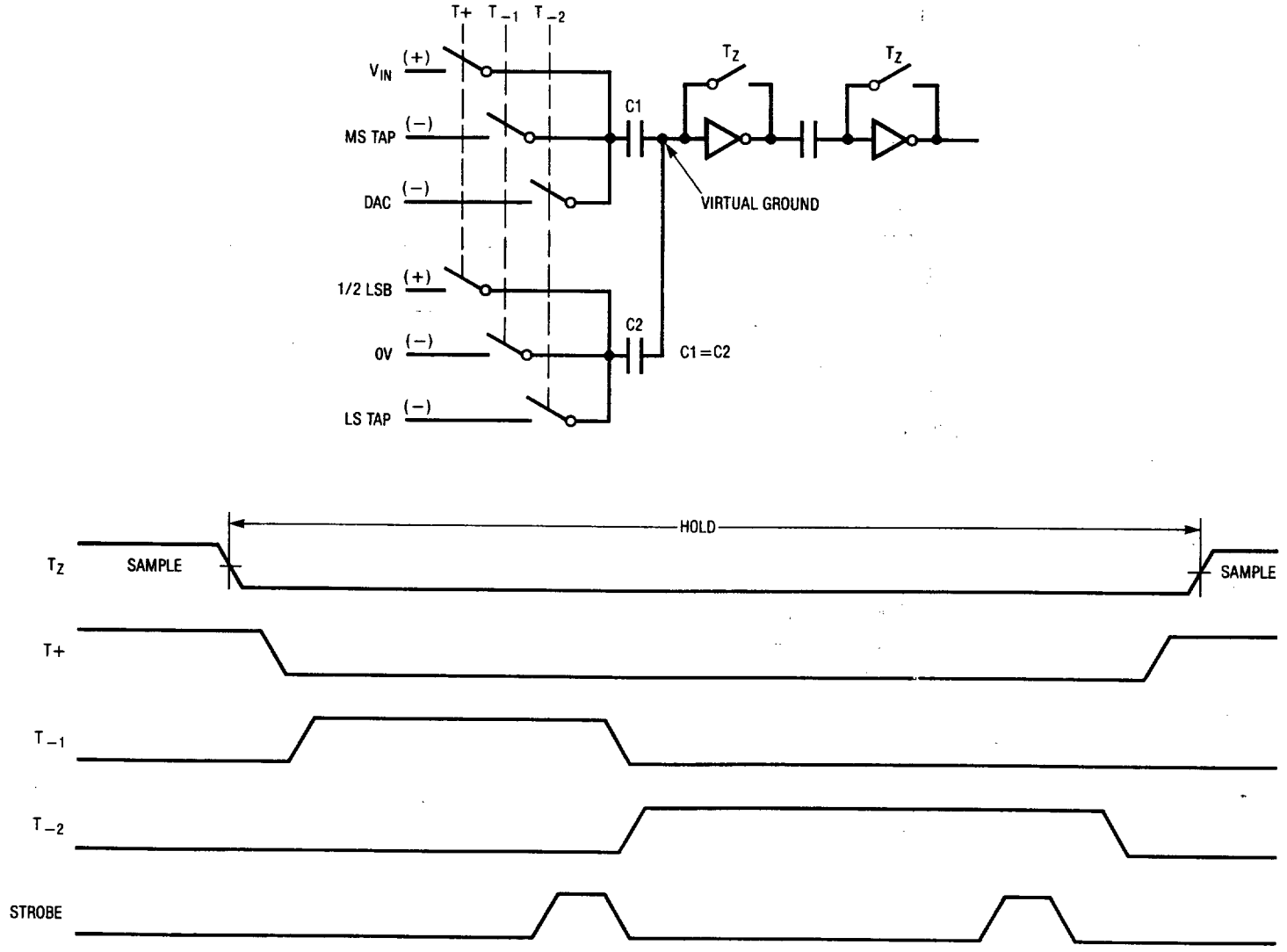


Figure 6. Six Input Switched Capacitor Comparator

FUNCTIONAL DESCRIPTION

The outputs of the 16 comparators are temporarily latched and drive the 4-bit DAC directly without need of decoding. This holds the DAC output constant for the next step — the LS conversion. The LS conversion is started when T_{-1} is opened and T_{-2} is closed. Capacitor C1 subtracts the 4-bit DAC approximation from V_{IN} and inputs the difference charge to the virtual ground node. The equation for each comparator is:

$$V_{IN} + 1/2LSB - V_{DAC} - LS_{TAP} = 0V$$

The 4-bit DAC approximation is input to all 16 comparators. The LS tap voltages are converted to charge by capacitor C2. LS taps vary from $V_{REF}/16V$ to 0V in 16 equal steps of $V_{REF}/256$. The comparators look at the net charge on the virtual ground node to perform the LS-Flash conversion. When this conversion is complete the 4 LSB's along with the 4 MSB's are transferred to the output latches. In this way all eight outputs will change simultaneously.

DIGITAL INTERFACE

The digital interface to the LTC1099 entails either controlling the conversion timing or reading data. There are two basic modes for controlling and reading the A/D — the WRITE-READ (WR-RD) mode and the READ (RD) mode.

WR-RD Mode (Pin 7 = High)

In the WR-RD mode a conversion sequence starts on the falling edge of $\overline{WR}$ with $\overline{CS}$ low (Figures 3A and 3B). This is an edge sensitive control function. The width of the $\overline{WR}$ input is not important. All timing functions are internal to the A/D.

The first thing to happen after the falling edge of $\overline{WR}$ is the internal S/H is switched to hold. This typically takes 110ns after $\overline{WR}$ falls and is the aperture time of the S/H.

Next the A/D conversion takes place. The conversion time is internally set at 2.5μs, but is user adjustable (see Adjusting the Conversion Time). The end of conversion is signaled by the high to low transition of $\overline{INT}$. The S/H is switched back to the acquire state as soon as the conversion is complete.

After the conversion is complete the 8-bit result is available on the three-state outputs. The outputs are active with $\overline{RD}$ and $\overline{CS}$ low. Output data is latched and, if no new conversion is initiated, is available indefinitely as long as the power is not turned off.

The WR-RD mode is also used for stand-alone operation. By tying $\overline{CS}$ and $\overline{RD}$ low the data outputs will be continuously active (Figure 4). The falling edge of $\overline{WR}$ starts the conversion sequence and when done new data will appear on the outputs. All outputs will be updated simultaneously. In stand-alone operation the outputs will never be in a high impedance state.

RD Mode (Pin 7 = Low)

In the RD mode a conversion sequence is initiated by the falling edge of $\overline{RD}$ when $\overline{CS}$ is low (Figure 2). The S/H is switched to the hold state 110ns after the falling edge of $\overline{RD}$. It is switched back to the acquire state at the end of conversion.

When $\overline{RD}$ goes low, with $\overline{CS}$ low, the result of the previous conversion is output. This data stays there until the ongoing conversion is complete ($\overline{INT}$ goes low). At this time the outputs are updated with new data.

As long as $\overline{CS}$ and $\overline{RD}$ stay low long enough, the receiving device will get the right data. Remember the receiving device reads data in on the rising edge of $\overline{RD}$. The RDY output facilitates making $\overline{RD}$ long enough.

In the RD mode the $\overline{WR}$ input becomes the RDY output. On the falling edge of $\overline{RD}$ the RDY goes low. It is an open drain output to allow a wired OR function so it requires a pull-up resistor. At the end of conversion the active pull-down is released and RDY goes high.

DIGITAL INTERFACE

The RDY output is designed to interface to the Ready In (RDYIN) function on many popular processors. RDYIN allows these processors to work with slow memory by stretching the $\overline{RD}$ strobe coming from the processor. $\overline{RD}$ will remain low as long as RDY is low. In the case of the LTC1099, RDY stays low until the conversion is complete and new data is available on the outputs. This greatly simplifies the programmers task. Each time data is required from the A/D a simple read is executed. The hardware interface makes sure the $\overline{RD}$ strobe is long enough.

Adjusting the Conversion Time

The conversion time of the LTC1099 is internally set at 2.5μs. If desired it can be adjusted by forcing a voltage on Pin 19. With Pin 19 left open the conversion time runs 2.5μs. A convenient way to force the voltage is with the circuit shown in Figure 7. To preset the conversion time to a fixed amount a resistor may be tied from Pin 19 to V_{CC} or GND. Tying it to V_{CC} slows down the conversion and tying it to GND will speed it up (see Typical Curves).

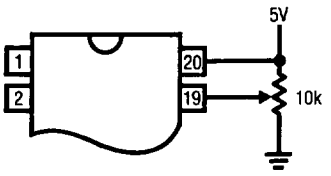


Figure 7. Adjusting the Conversion Time

ANALOG INTERFACE

The inclusion of a high quality sample-and-hold (S/H) simplifies the analog interface to the LTC1099. All of the error terms normally associated with an S/H (hold step, offset, gain, and droop errors) are included in the error specifications for the A/D. This makes it easy for the designer since all the error terms need not be taken into account individually.

S/H Timing

A falling edge on the $\overline{RD}$ or $\overline{WR}$ input switches the S/H from acquire to hold and starts the conversion. The aperture time is the delay from the falling edge to the actual instant when the S/H switches to hold. It is typically 110ns.

As soon as a conversion is complete (2.5μs typ.) the S/H switches back to the sample mode. Even though the acquisition time is only 240ns a new conversion cannot be started for 700ns (typ.) after a conversion is completed.

Analog Input

The input to the A/D looks like a 60pF capacitor in series with 550Ω (Figure 8).

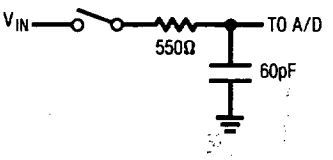


Figure 8. Equivalent Input Circuit

With this high input capacitance care must be taken when driving the inputs from a source amplifier. When the input switch closes an instantaneous capacitive load is applied to the amplifier output. This acts like an impulse into the amplifier and if it has poor phase margin the resulting ringing can cause a considerable loss of accuracy. If the amplifier is too slow the resulting settling tail will also cause a loss of accuracy. The amplifier should also have low open circuit output impedance. The LT1006 is an excellent amplifier in this regard. It also works with a single supply which fits nicely with the LTC1099.

Reference Inputs

Sixteen equal valued resistors are internally connected between REF+ and REF–. Each resistor is nominally 200Ω giving a total resistance of 3.2kΩ between the reference terminals. When V_{IN} equals REF+ the output code will be all ones. When V_{IN} equals REF– the output code will be all zeros.

ANALOG INTERFACE

Although it is most common to connect REF+ to a 5V reference and REF– to ground, any voltages can be used. The only restrictions are REF+ >REF– and REF+ and REF– must be within the supply rails. As the reference voltage is reduced the A/D will eventually lose accuracy. Accuracy is quite good for references down to 1V.

Even though the reference drives a resistive ladder a lot of capacitive switching is taking place internally. For this reason driving the reference has the same characteristics as driving V_{IN}. A fast low impedance source is necessary. The reference has the additional problem of presenting a DC load to the driving source. This requires the DC as well as the AC source impedance to be low.

Good Grounding

As with any precise analog system care must be taken to follow good grounding practices when using the LTC1099. The most noise free environment is obtained by using a ground plane with GND (Pin 10) and REF– (Pin 11) tied to it. Bypass capacitors from REF+ (Pin 12) and V_{CC} (Pin 20) with short leads are also required to prevent spurious switching noise from affecting the conversion accuracy.

If a ground plane is not practical, single point grounding techniques should be used. Ground for the A/D should not be mixed in with other noisy grounds.

APPLICATIONS

Analog Multiplier

The schematic Figure 9 shows the LTC1099 configured with a DAC to form a 2 quadrant analog multiplier. An input waveform is applied to the LTC1099 where it is digitized at a 300kHz rate. The digitized signal is fed to the DAC in "flow through" mode where another signal is input to the DAC reference input. In this way the two analog signals are multiplied to produce a Double Sideband Amplitude Modulated Output. Figure 10 shows a 3kHz sine wave multiplied by a 100Hz triangle.

Note that since this is only a 2 quadrant multiplier a carrier component (the input to the LTC1099) will appear in the output spectrum. Figure 11 shows the frequency spectrum of a 42.5kHz sine wave multiplied by a 5kHz sine wave. The depth of modulation is about 30dB. Figure 12 shows a 42.375kHz sine wave multiplied by a 30.875kHz sine wave. Note that at these higher frequencies, the depth of modulation is still about 30dB. The carrier feed through is seen in Figure 12.

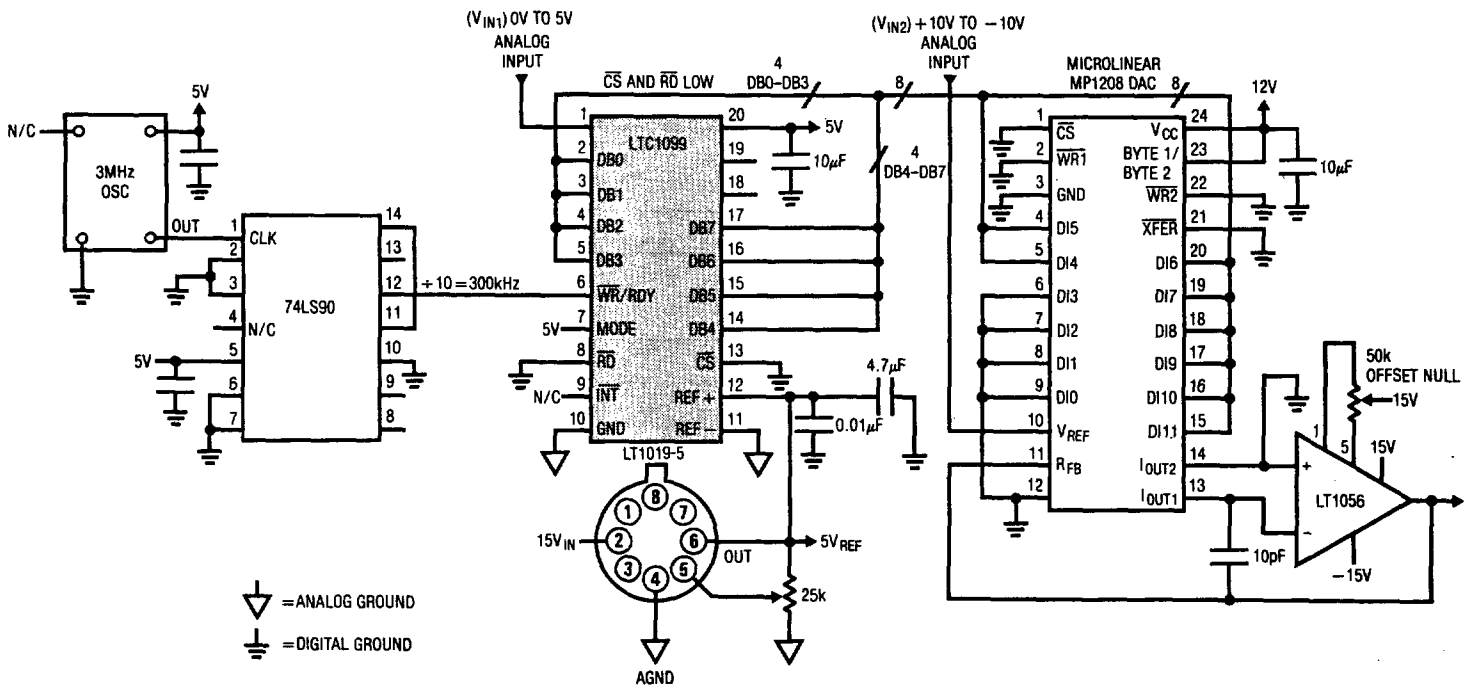


Figure 9.

ANALOG INTERFACE

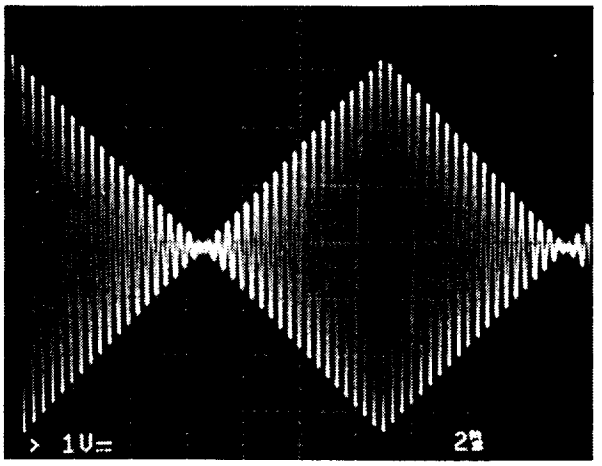


Figure 10.

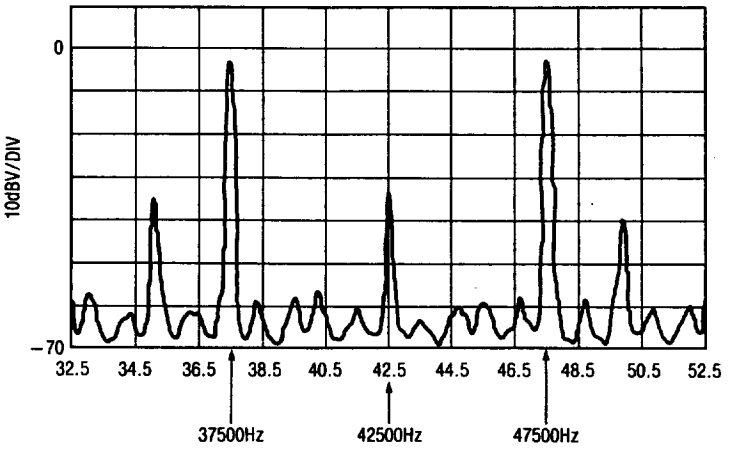


Figure 11. Two Quadrant Multiplier Output Spectrum with 0V to 4.5V at 42.5kHz into LTC1099 and ±2V at 5kHz into DAC

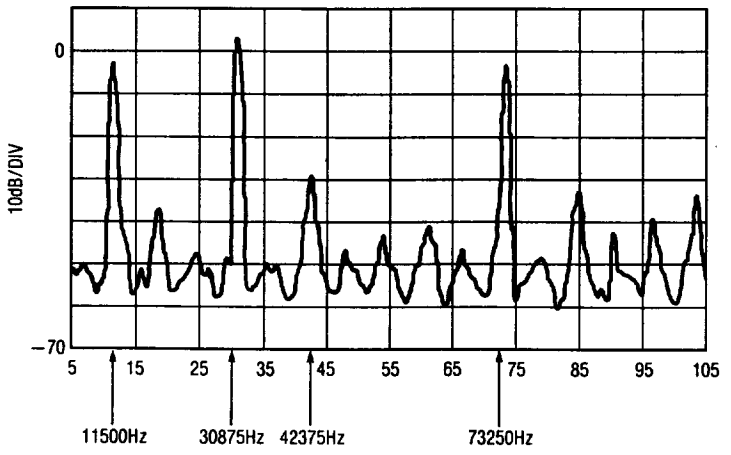
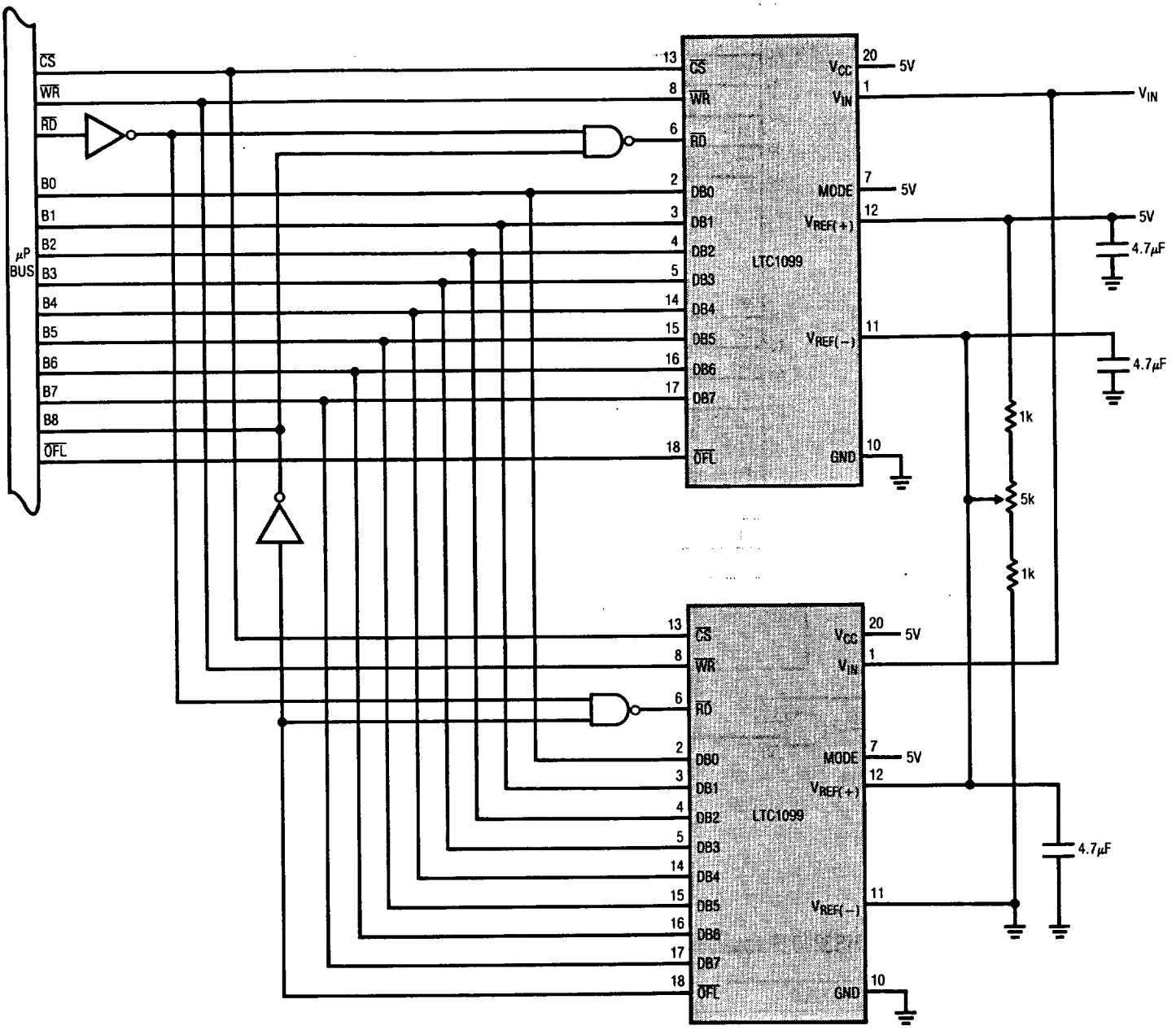


Figure 12. Two Quadrant Multiplier Output Spectrum with 0V to 4.5V at 42.375kHz into LTC1099 and ±2V at 30.875kHz into DAC

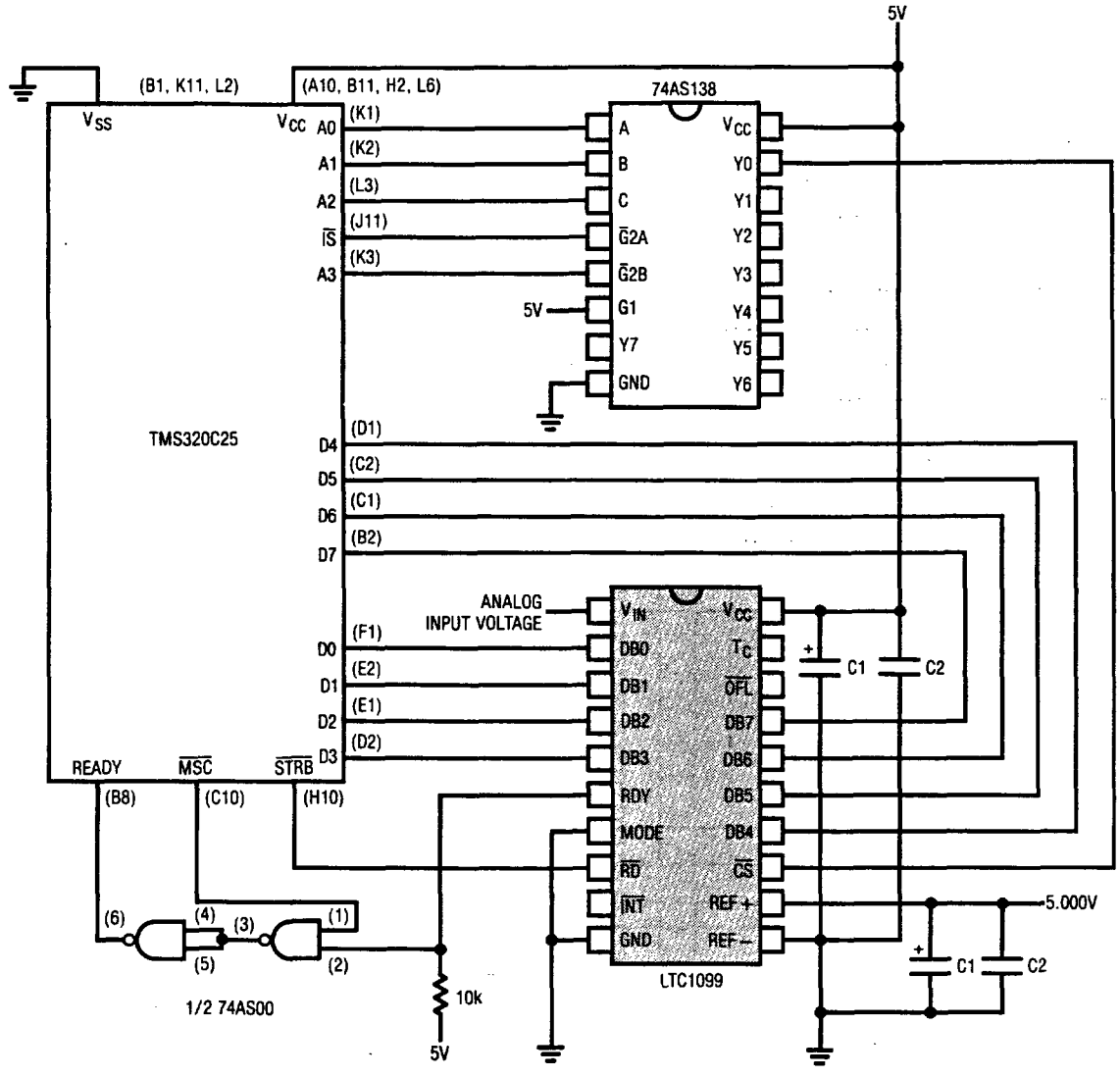
TYPICAL APPLICATIONS

Cascading for 9-Bit Resolution



TYPICAL APPLICATIONS

TMS320C25 Interface Using RD-Mode



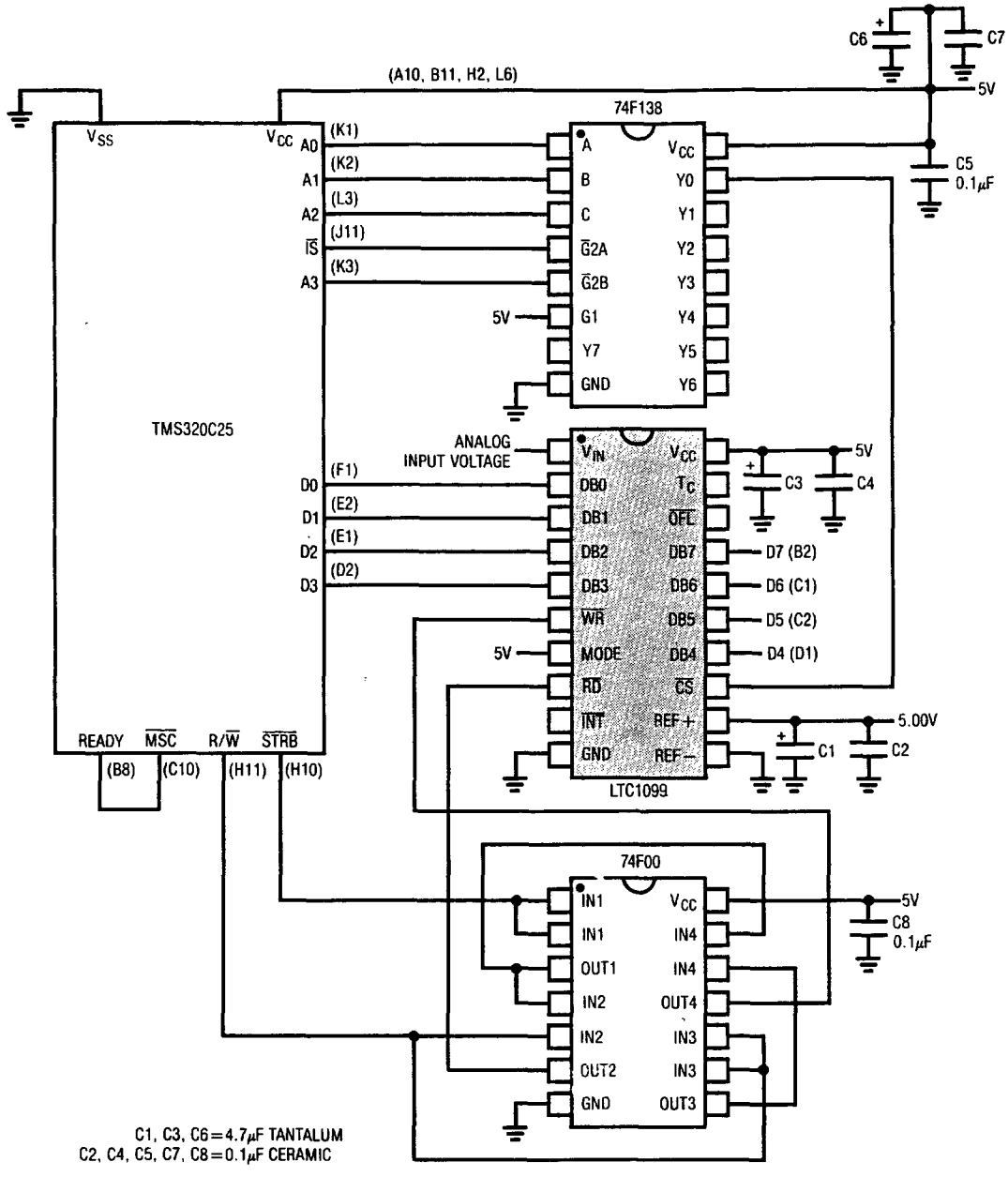
C1 = 4.7μF TANTALUM
C2 = 0.1μF CERAMIC

TMS320C25 Assembly Code for RD-Mode Interface to LTC1099

0001	0000					
0002	0032			AORG	>32	
0003	0032	CE01		DINT		Disable Interrupts
0004	0033	C800		LDPK	>00	Data Page Pointer is 0
0005	0034	8064	LOOP	IN	100,PA0	Input 1099 Data to Address 100
0006	0035	CB13		RPTK	12	Repeat Next Instruction 12 Times
0007	0036	5500		NOP		Don't Convert Again Too Soon
0008	0037	FF80		B	LOOP	Go for Another Conversion

TYPICAL APPLICATIONS

TMS320C25 Interface Using WR-RD Mode



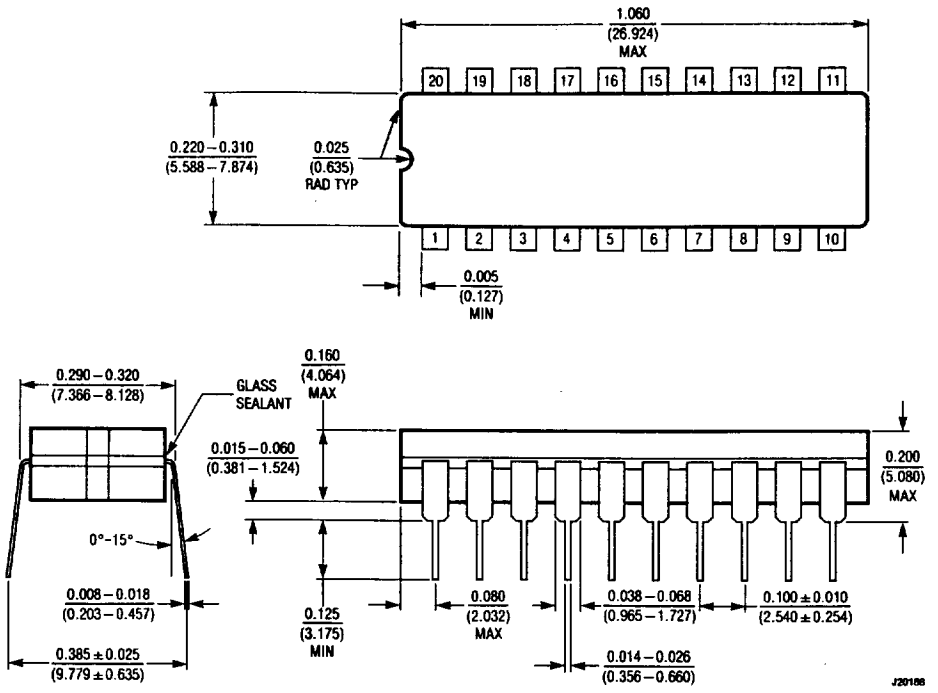
TMS320C25 Assembly Code for WR-RD-Mode Interface to LTC1099

0001	0032			AORG	>32	
0002	0032	CE01		DINT		Disable Interrupts
0003	0033	C800		LDPK	>0	Data Page Pointer is ϕ
0004	0034	E064	LOOP	OUT	>64.PA0	Start LTC1099 Conversion
0005	0035	CB20		RPTK	>12	Wait for Conversion to Finish
0006	0036	5500		NOP		
0007	0037	8064		IN	>64.PA0	Read LTC1099 Data; Store in >64
0008	0038	FF80		B	LOOP	Do Again

9

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

J Package
20-Lead Ceramic DIP



N Package
20-Lead Plastic DIP