

# MC33201 MC33202 MC33204

## Rail-to-Rail Operational Amplifiers

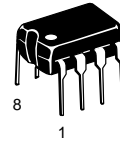
The MC33201/2/4 family of operational amplifiers provide rail-to-rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail-to-rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages ( $\pm 0.9$  V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over-driven Input Signals
- High Output Current ( $I_{SC} = 80$  mA, Typ)
- Low Supply Current ( $I_D = 0.9$  mA, Typ)
- 600  $\Omega$  Output Drive Capability
- Extended Operating Temperature Ranges ( $-40^\circ$  to  $+105^\circ\text{C}$  and  $-55^\circ$  to  $+125^\circ\text{C}$ )
- Typical Gain Bandwidth Product = 2.2 MHz
- Offered in New TSSOP Package Including Standard SOIC and DIP Packages

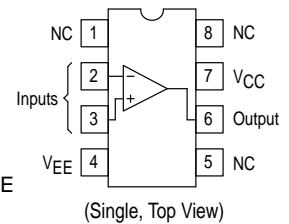
### ORDERING INFORMATION

Operational Amplifier Function	Device	Operating Temperature Range	Package
Single	MC33201D	$T_A = -40^\circ$ to $+105^\circ\text{C}$	SO-8
	MC33201P		Plastic DIP
	MC33201VD	$T_A = -55^\circ$ to $+125^\circ\text{C}$	SO-8
	MC33201VP		Plastic DIP
Dual	MC33202D	$T_A = -40^\circ$ to $+105^\circ\text{C}$	SO-8
	MC33202P		Plastic DIP
	MC33202VD	$T_A = -55^\circ$ to $+125^\circ\text{C}$	SO-8
	MC33202VP		Plastic DIP
Quad	MC33204D	$T_A = -40^\circ$ to $+105^\circ\text{C}$	SO-14
	MC33204DTB		TSSOP-14
	MC33204P		Plastic DIP
	MC33204VD	$T_A = -55^\circ$ to $+125^\circ\text{C}$	SO-14
	MC33204VDTB		TSSOP-14
	MC33204VP		Plastic DIP

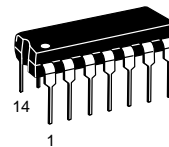
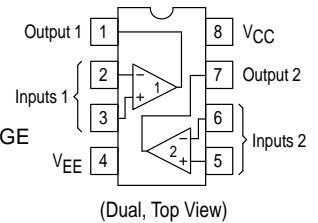
### LOW VOLTAGE RAIL-TO-RAIL OPERATIONAL AMPLIFIERS



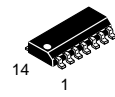
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626



**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751  
(SO-8)



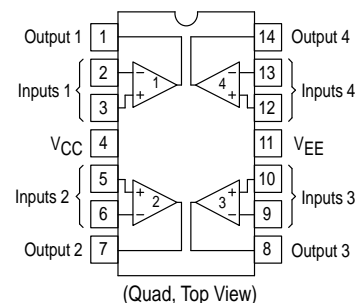
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646



**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751A  
(SO-14)



**DTB SUFFIX**  
PLASTIC PACKAGE  
CASE 948G  
(TSSOP-14)



# MC33201 MC33202 MC33204

## DC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

Characteristic	V <sub>CC</sub> = 2.0 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5.0 V	Unit
Input Offset Voltage V <sub>IO</sub> (max) MC33201 MC33202 MC33204	± 8.0 ±10 ±12	± 8.0 ±10 ±12	± 6.0 ± 8.0 ±10	mV
Output Voltage Swing V <sub>OH</sub> (R <sub>L</sub> = 10 kΩ) V <sub>OL</sub> (R <sub>L</sub> = 10 kΩ)	1.9 0.10	3.15 0.15	4.85 0.15	V <sub>min</sub> V <sub>max</sub>
Power Supply Current per Amplifier (I <sub>D</sub> )	1.125	1.125	1.125	mA

Specifications at V<sub>CC</sub> = 3.3 V are guaranteed by the 2.0 V and 5.0 V tests. V<sub>EE</sub> = Gnd.

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V <sub>CC</sub> to V <sub>EE</sub> )	V <sub>S</sub>	+13	V
Input Differential Voltage Range	V <sub>IDR</sub>	(Note 1)	V
Common Mode Input Voltage Range (Note 2)	V <sub>CM</sub>	V <sub>CC</sub> + 0.5 V to V <sub>EE</sub> - 0.5 V	V
Output Short Circuit Duration	t <sub>s</sub>	(Note 3)	sec
Maximum Junction Temperature	T <sub>J</sub>	+150	°C
Storage Temperature	T <sub>stg</sub>	- 65 to +150	°C
Maximum Power Dissipation	P <sub>D</sub>	(Note 3)	mW

- NOTES:**
1. The differential input voltage of each amplifier is limited by two internal parallel back-to-back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
  2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
  3. Power dissipation must be considered to ensure maximum junction temperature (T<sub>J</sub>) is not exceeded. (See Figure 2)

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = + 5.0 V, V<sub>EE</sub> = Ground, T<sub>A</sub> = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V <sub>CM</sub> = 0 V to 0.5 V, V <sub>CM</sub> = 1.0 V to 5.0 V) MC33201: T <sub>A</sub> = + 25°C T <sub>A</sub> = - 40° to +105°C T <sub>A</sub> = - 55° to +125°C MC33202: T <sub>A</sub> = + 25°C T <sub>A</sub> = - 40° to +105°C T <sub>A</sub> = - 55° to +125°C MC33204: T <sub>A</sub> = + 25°C T <sub>A</sub> = - 40° to +105°C T <sub>A</sub> = - 55° to +125°C	3	V <sub>IO</sub>	-	-	6.0 9.0 13 8.0 11 14 10 13 17	mV
Input Offset Voltage Temperature Coefficient (R <sub>S</sub> = 50 Ω) T <sub>A</sub> = - 40° to +105°C T <sub>A</sub> = - 55° to +125°C	4	ΔV <sub>IO</sub> /ΔT	-	2.0 2.0	-	μV/°C
Input Bias Current (V <sub>CM</sub> = 0 V to 0.5 V, V <sub>CM</sub> = 1.0 V to 5.0 V) T <sub>A</sub> = + 25°C T <sub>A</sub> = - 40° to +105°C T <sub>A</sub> = - 55° to +125°C	5, 6	I <sub>IB</sub>	-	80 100 -	200 250 500	nA
Input Offset Current (V <sub>CM</sub> = 0 V to 0.5 V, V <sub>CM</sub> = 1.0 V to 5.0 V) T <sub>A</sub> = + 25°C T <sub>A</sub> = - 40° to +105°C T <sub>A</sub> = - 55° to +125°C	-	I <sub>IO</sub>	-	5.0 10 -	50 100 200	nA
Common Mode Input Voltage Range	-	V <sub>ICR</sub>	V <sub>EE</sub>	-	V <sub>CC</sub>	V

## MC33201 MC33202 MC33204

**DC ELECTRICAL CHARACTERISTICS (continued)** ( $V_{CC} = +5.0\text{ V}$ ,  $V_{EE} = \text{Ground}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

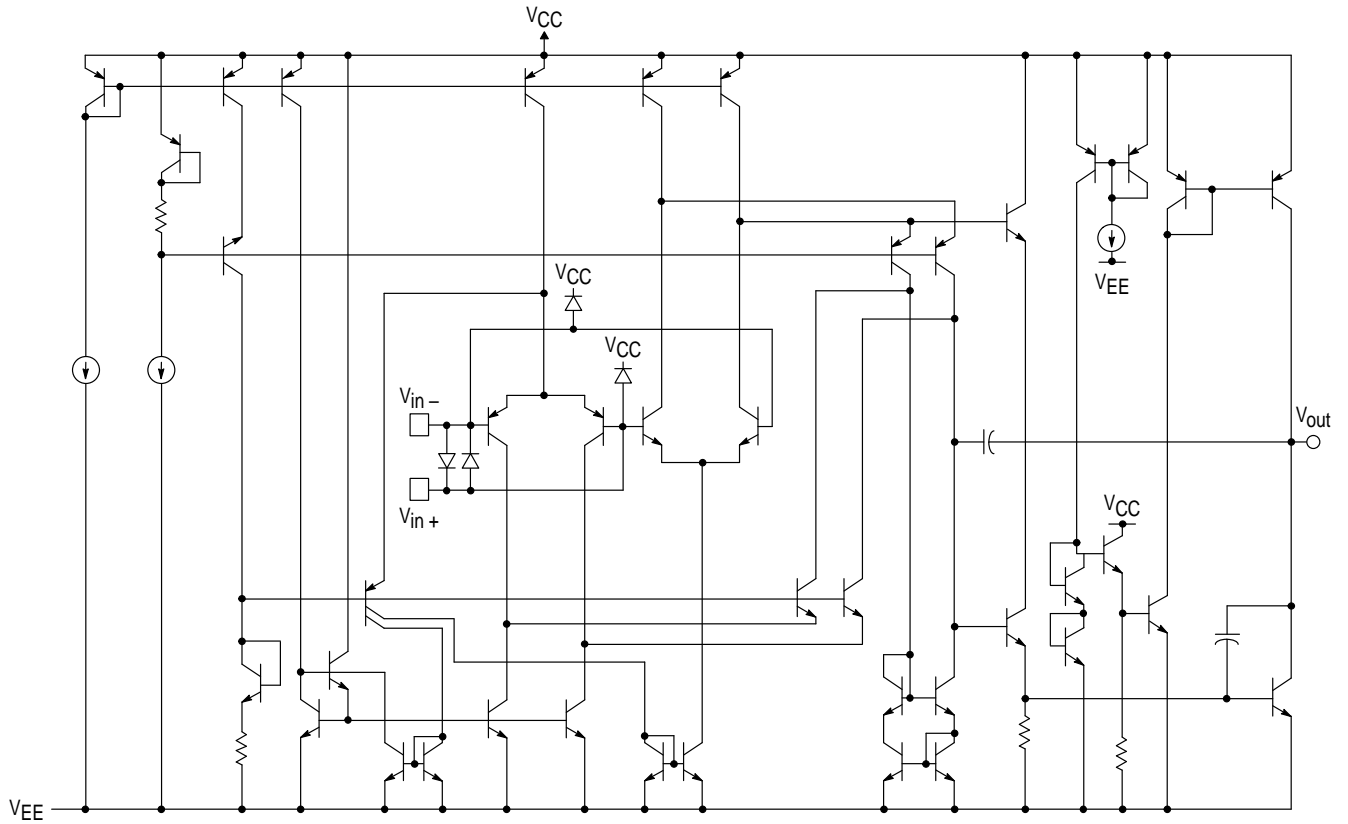
Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Large Signal Voltage Gain ( $V_{CC} = +5.0\text{ V}$ , $V_{EE} = -5.0\text{ V}$ ) $R_L = 10\text{ k}\Omega$ $R_L = 600\ \Omega$	7	$A_{VOL}$	50 25	300 250	– –	kV/V
Output Voltage Swing ( $V_{ID} = \pm 0.2\text{ V}$ ) $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 600\ \Omega$ $R_L = 600\ \Omega$	8, 9, 10	$V_{OH}$ $V_{OL}$ $V_{OH}$ $V_{OL}$	4.85 – 4.75 –	4.95 0.05 4.85 0.15	– 0.15 – 0.25	V
Common Mode Rejection ( $V_{in} = 0\text{ V}$ to $5.0\text{ V}$ )	11	CMR	60	90	–	dB
Power Supply Rejection Ratio $V_{CC}/V_{EE} = 5.0\text{ V/Gnd}$ to $3.0\text{ V/Gnd}$	12	PSRR	500	25	–	$\mu\text{V/V}$
Output Short Circuit Current (Source and Sink)	13, 14	$I_{SC}$	50	80	–	mA
Power Supply Current per Amplifier ( $V_O = 0\text{ V}$ ) $T_A = -40^\circ$ to $+105^\circ\text{C}$ $T_A = -55^\circ$ to $+125^\circ\text{C}$	15	$I_D$	– –	0.9 0.9	1.125 1.125	mA

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +5.0\text{ V}$ ,  $V_{EE} = \text{Ground}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate ( $V_S = \pm 2.5\text{ V}$ , $V_O = -2.0\text{ V}$ to $+2.0\text{ V}$ , $R_L = 2.0\text{ k}\Omega$ , $A_V = +1.0$ )	16, 26	SR	0.5	1.0	–	V/ $\mu\text{s}$
Gain Bandwidth Product ( $f = 100\text{ kHz}$ )	17	GBW	–	2.2	–	MHz
Gain Margin ( $R_L = 600\ \Omega$ , $C_L = 0\text{ pF}$ )	20, 21, 22	$A_M$	–	12	–	dB
Phase Margin ( $R_L = 600\ \Omega$ , $C_L = 0\text{ pF}$ )	20, 21, 22	$\phi_M$	–	65	–	Deg
Channel Separation ( $f = 1.0\text{ Hz}$ to $20\text{ kHz}$ , $A_V = 100$ )	23	CS	–	90	–	dB
Power Bandwidth ( $V_O = 4.0\text{ V}_{pp}$ , $R_L = 600\ \Omega$ , $\text{THD} \leq 1\%$ )		BWP	–	28	–	kHz
Total Harmonic Distortion ( $R_L = 600\ \Omega$ , $V_O = 1.0\text{ V}_{pp}$ , $A_V = 1.0$ ) $f = 1.0\text{ kHz}$ $f = 10\text{ kHz}$	24	THD	– –	0.002 0.008	– –	%
Open Loop Output Impedance ( $V_O = 0\text{ V}$ , $f = 2.0\text{ MHz}$ , $A_V = 10$ )		$ Z_O $	–	100	–	$\Omega$
Differential Input Resistance ( $V_{CM} = 0\text{ V}$ )		$R_{in}$	–	200	–	k $\Omega$
Differential Input Capacitance ( $V_{CM} = 0\text{ V}$ )		$C_{in}$	–	8.0	–	pF
Equivalent Input Noise Voltage ( $R_S = 100\ \Omega$ ) $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	25	$e_n$	– –	25 20	– –	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	25	$i_n$	– –	0.8 0.2	– –	pA/ $\sqrt{\text{Hz}}$

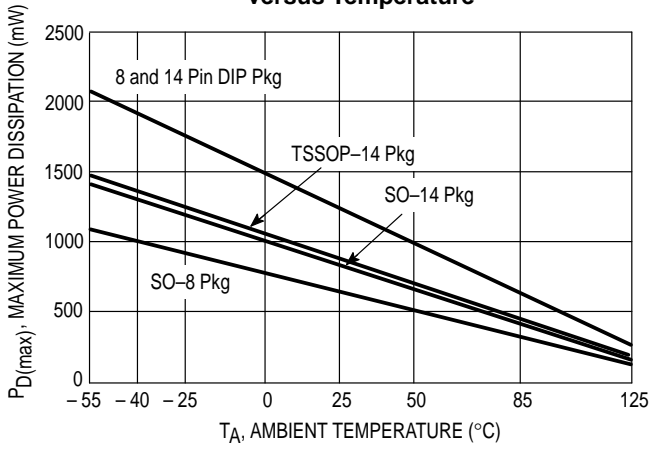
# MC33201 MC33202 MC33204

Figure 1. Circuit Schematic  
(Each Amplifier)

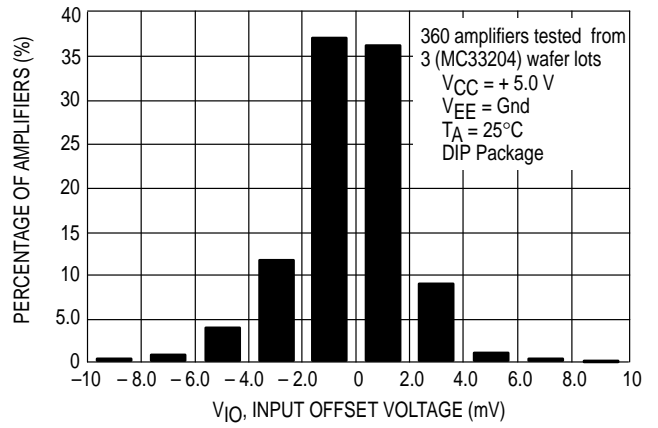


This device contains 70 active transistors (each amplifier).

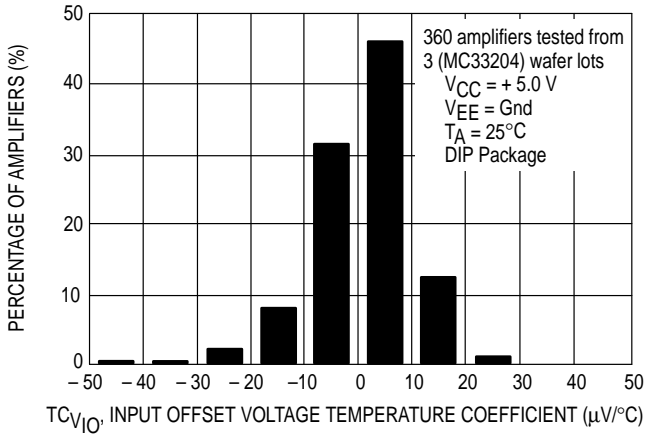
**Figure 2. Maximum Power Dissipation versus Temperature**



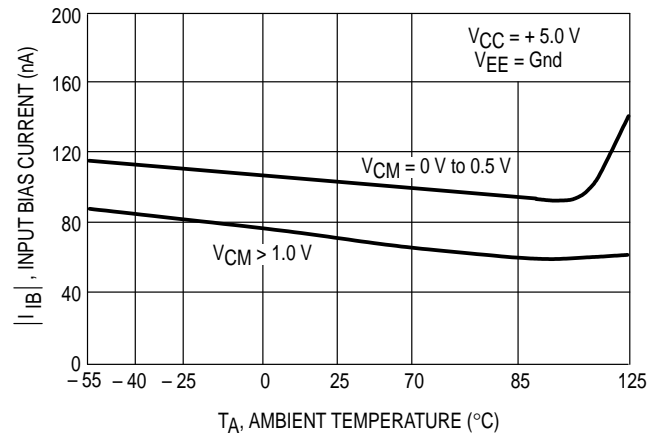
**Figure 3. Input Offset Voltage Distribution**



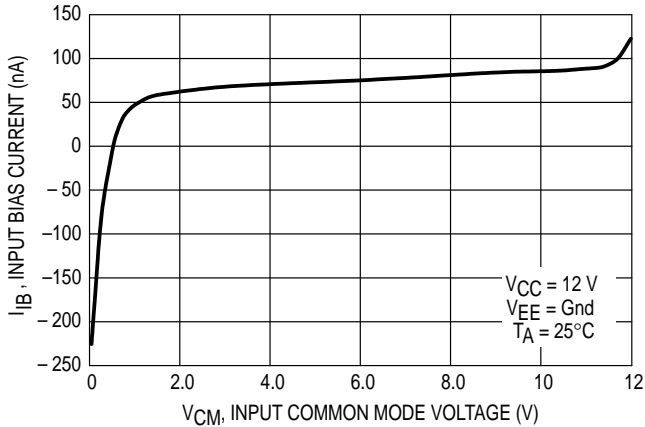
**Figure 4. Input Offset Voltage Temperature Coefficient Distribution**



**Figure 5. Input Bias Current versus Temperature**



**Figure 6. Input Bias Current versus Common Mode Voltage**



**Figure 7. Open Loop Voltage Gain versus Temperature**

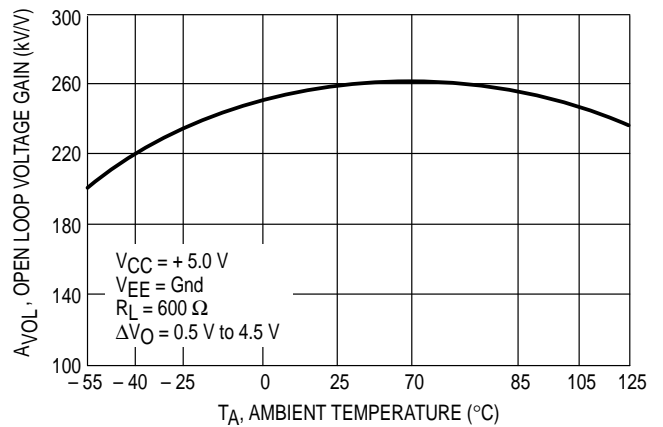


Figure 8. Output Voltage Swing versus Supply Voltage

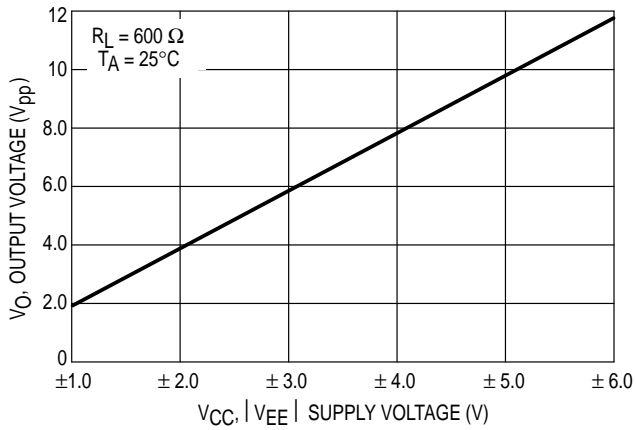


Figure 9. Output Saturation Voltage versus Load Current

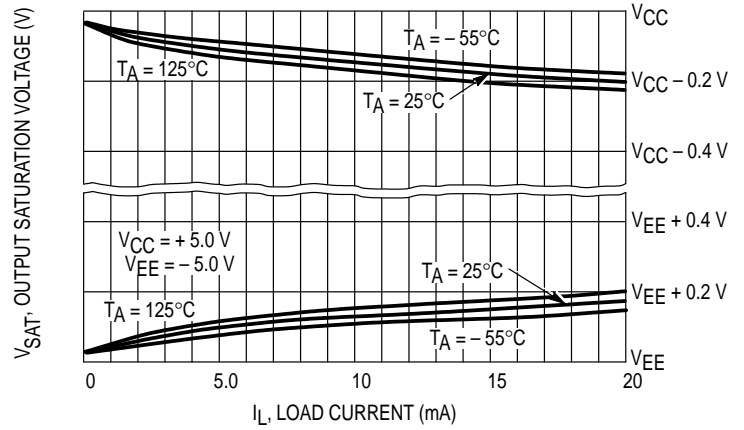


Figure 10. Output Voltage versus Frequency

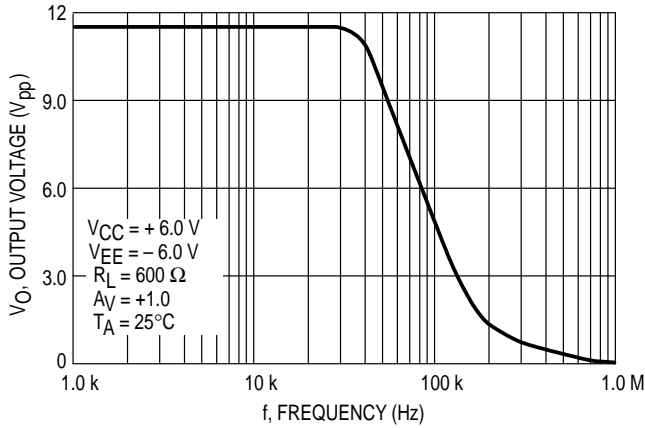


Figure 11. Common Mode Rejection versus Frequency

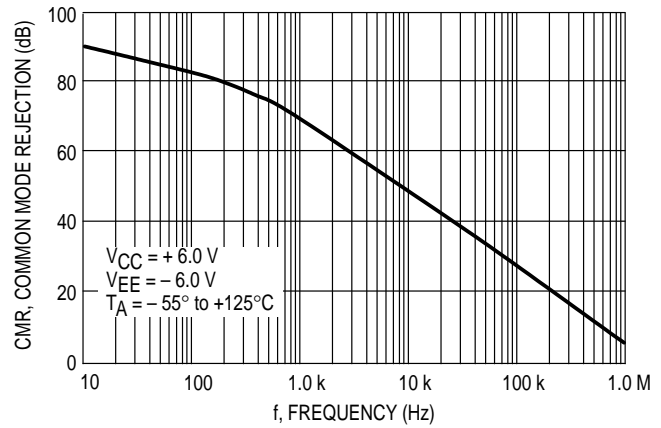


Figure 12. Power Supply Rejection versus Frequency

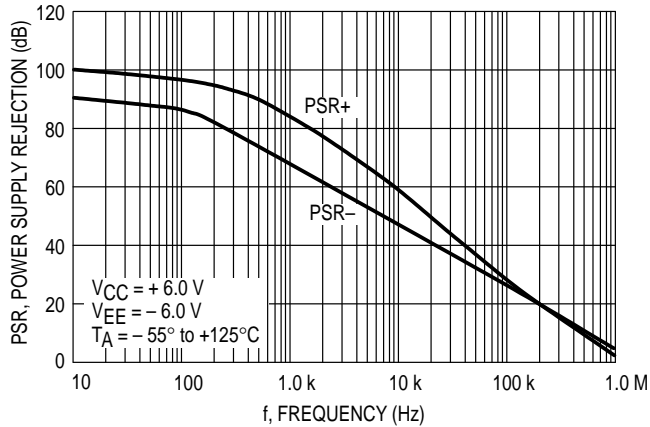


Figure 13. Output Short Circuit Current versus Output Voltage

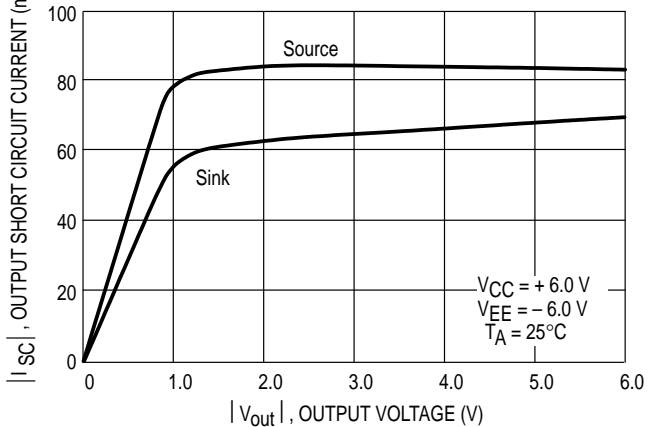


Figure 14. Output Short Circuit Current versus Temperature

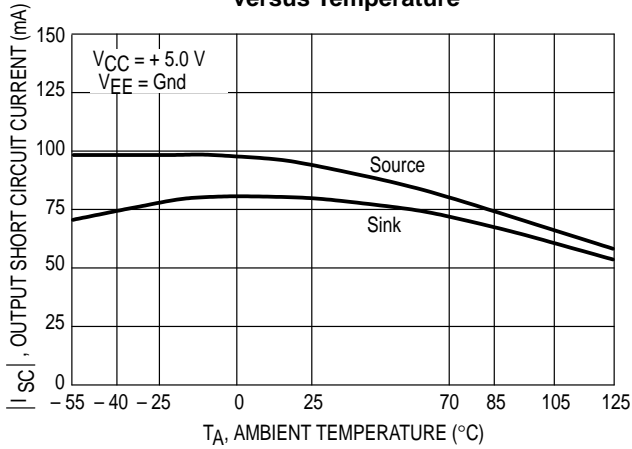


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

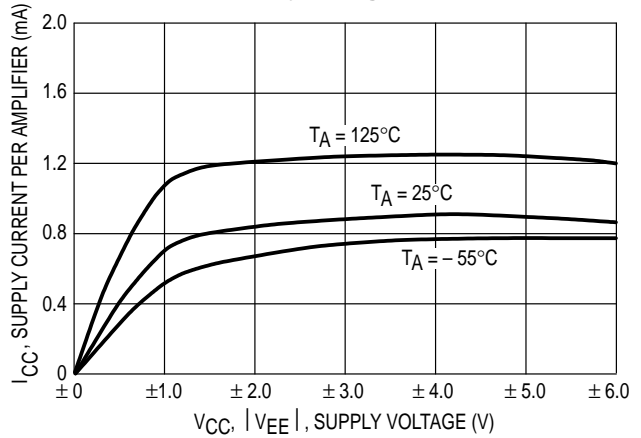


Figure 16. Slew Rate versus Temperature

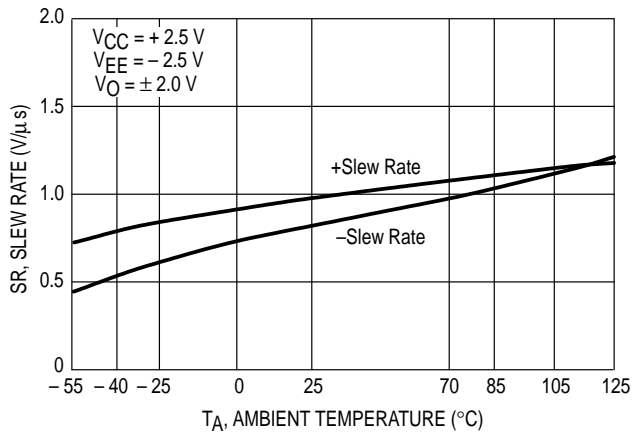


Figure 17. Gain Bandwidth Product versus Temperature

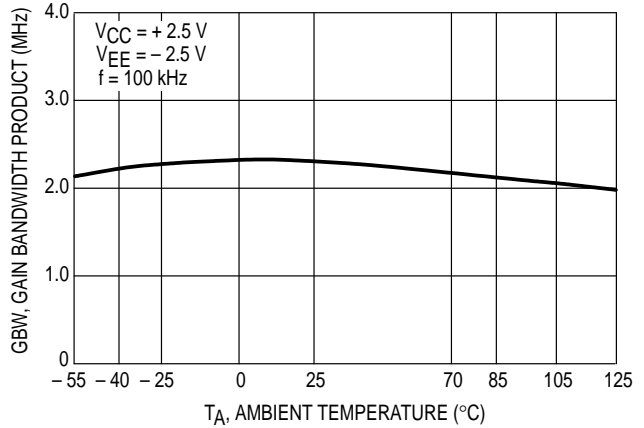


Figure 18. Voltage Gain and Phase versus Frequency

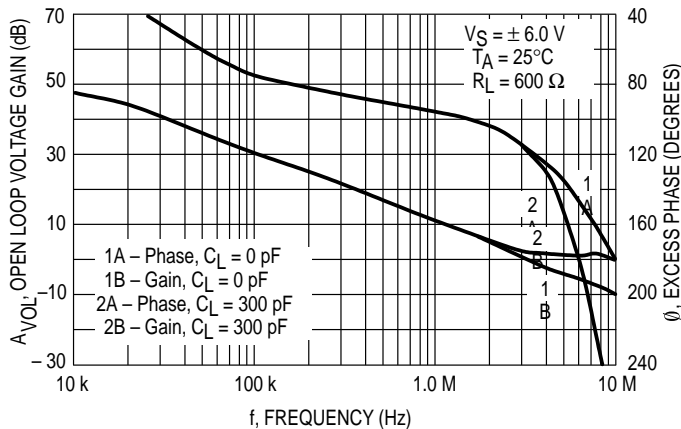


Figure 19. Voltage Gain and Phase versus Frequency

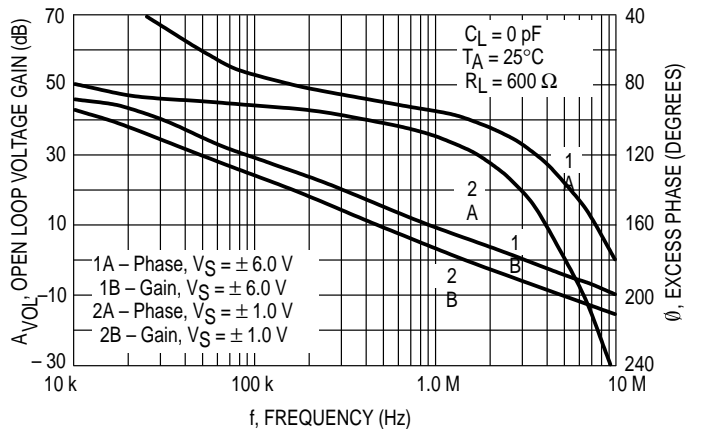


Figure 20. Gain and Phase Margin versus Temperature

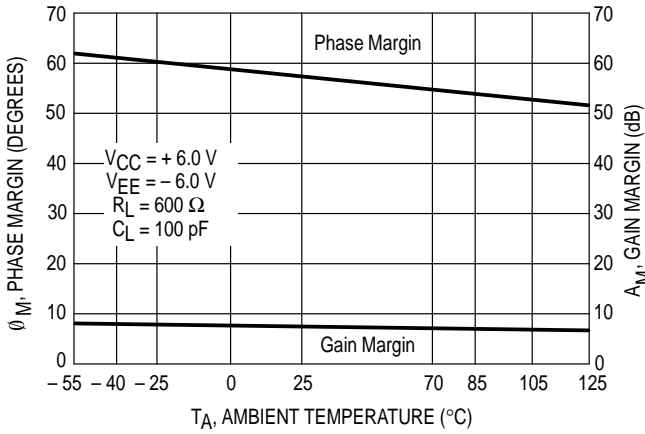


Figure 21. Gain and Phase Margin versus Differential Source Resistance

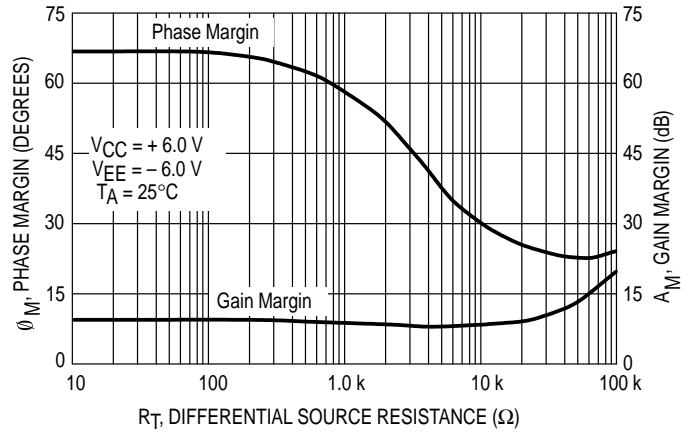


Figure 22. Gain and Phase Margin versus Capacitive Load

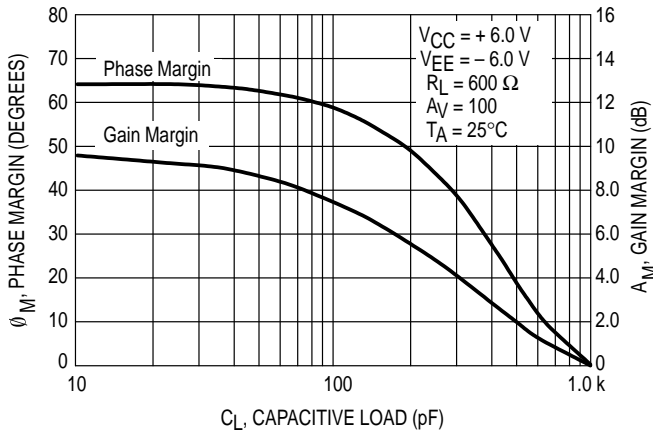


Figure 23. Channel Separation versus Frequency

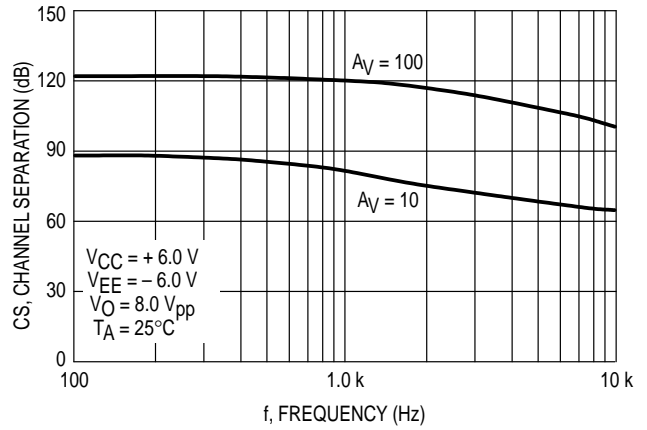


Figure 24. Total Harmonic Distortion versus Frequency

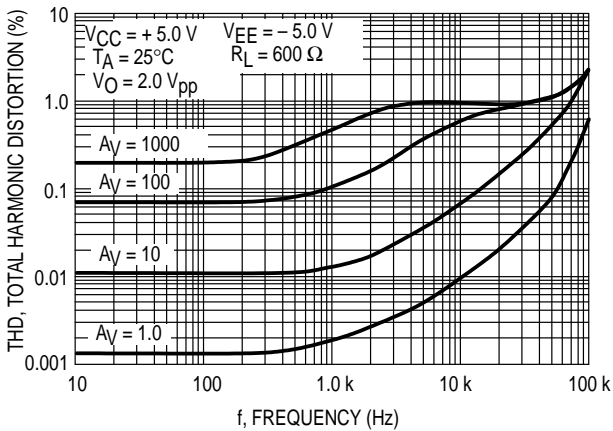
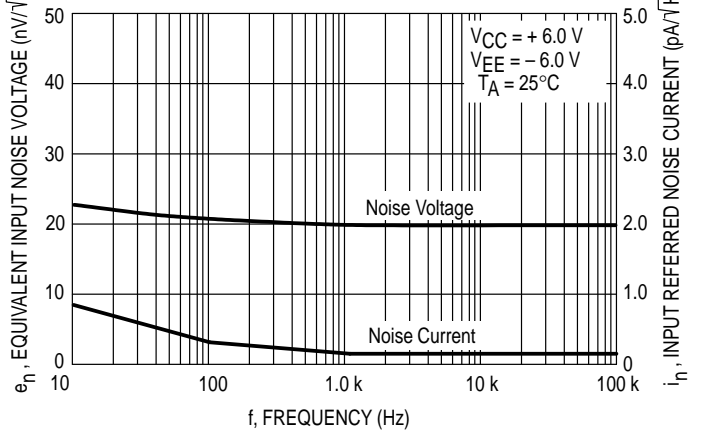


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency





General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail-to-rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from  $V_{CC}$  to  $V_{EE}$ , it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail-to-rail performance is achieved at the input of the amplifiers by using parallel NPN-PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than  $V_{EE}$ , the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross-coupling techniques have been used to keep this change to a minimum.

In addition to its rail-to-rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600  $\Omega$  loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

Figure 26. Noninverting Amplifier Slew Rate

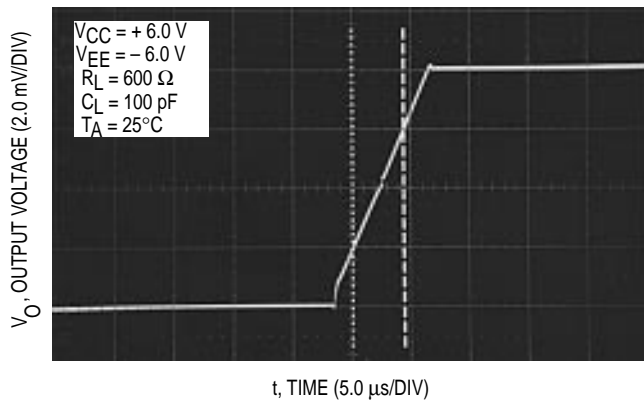


Figure 27. Small Signal Transient Response

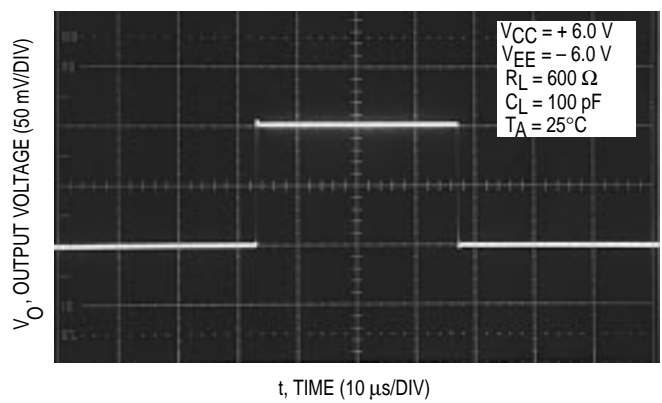
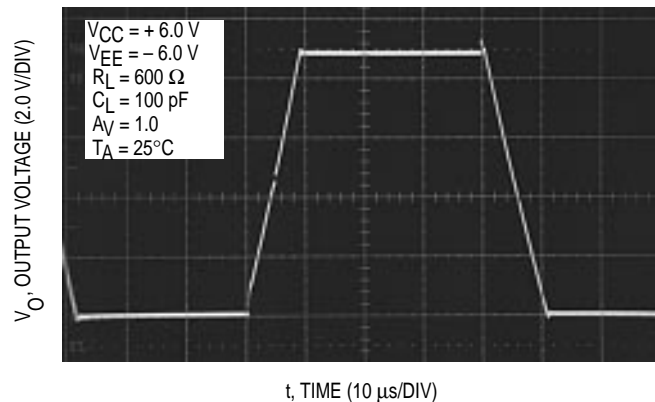

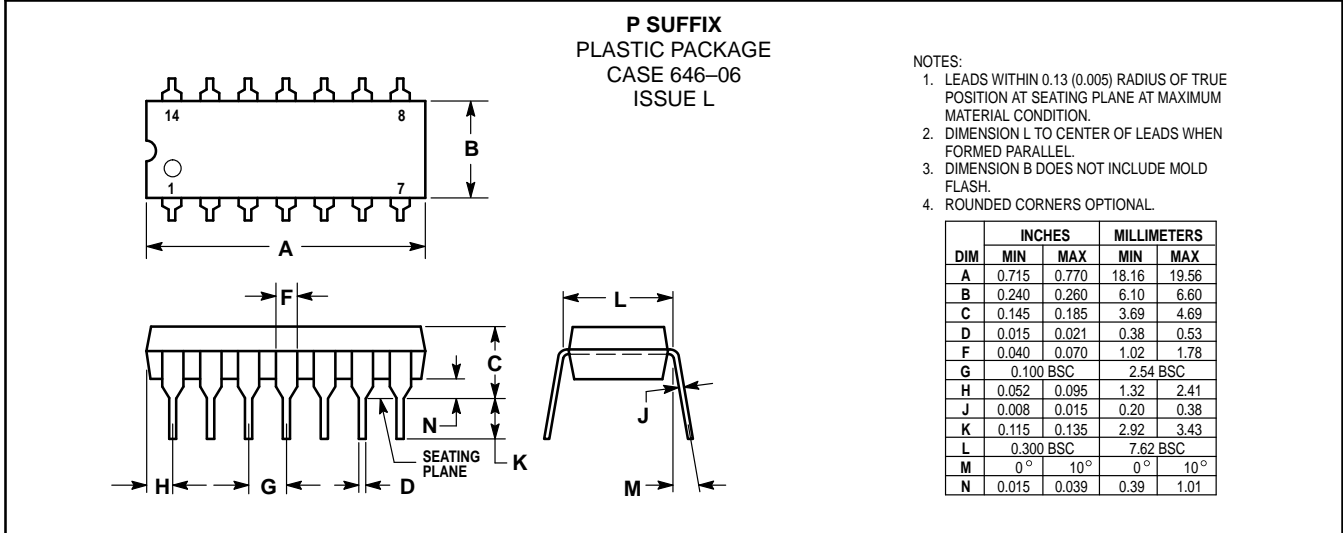
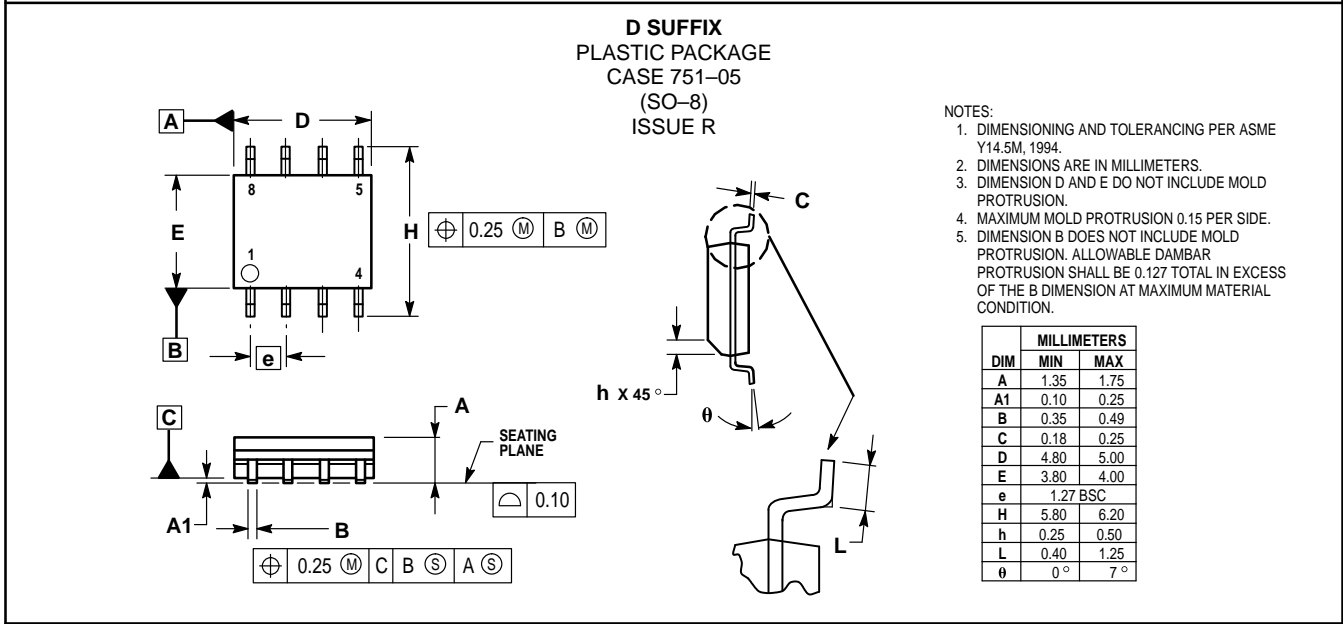
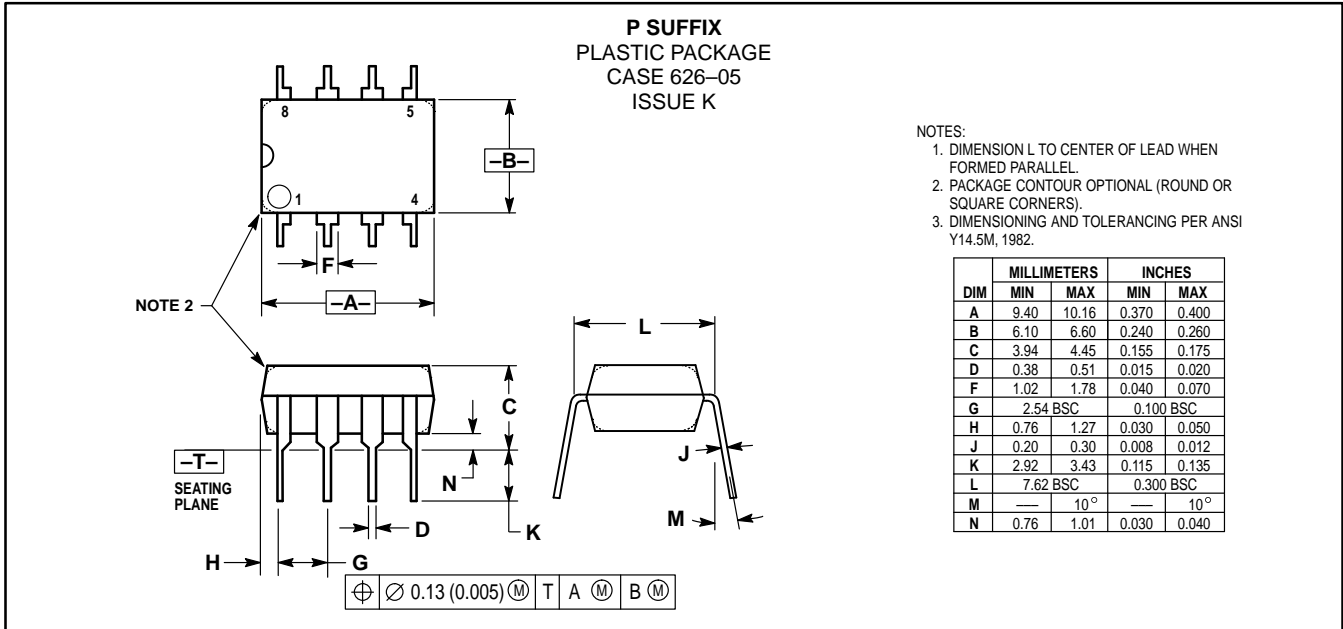


Figure 28. Large Signal Transient Response



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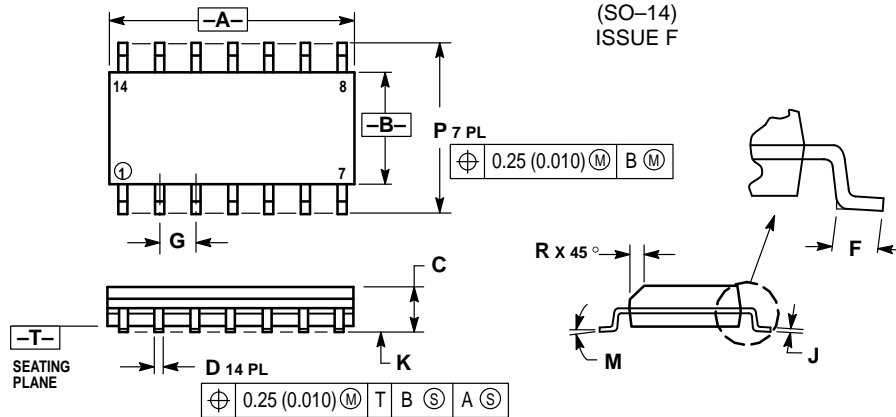
OUTLINE DIMENSIONS



# MC33201 MC33202 MC33204

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC PACKAGE CASE 751A-03 (SO-14) ISSUE F

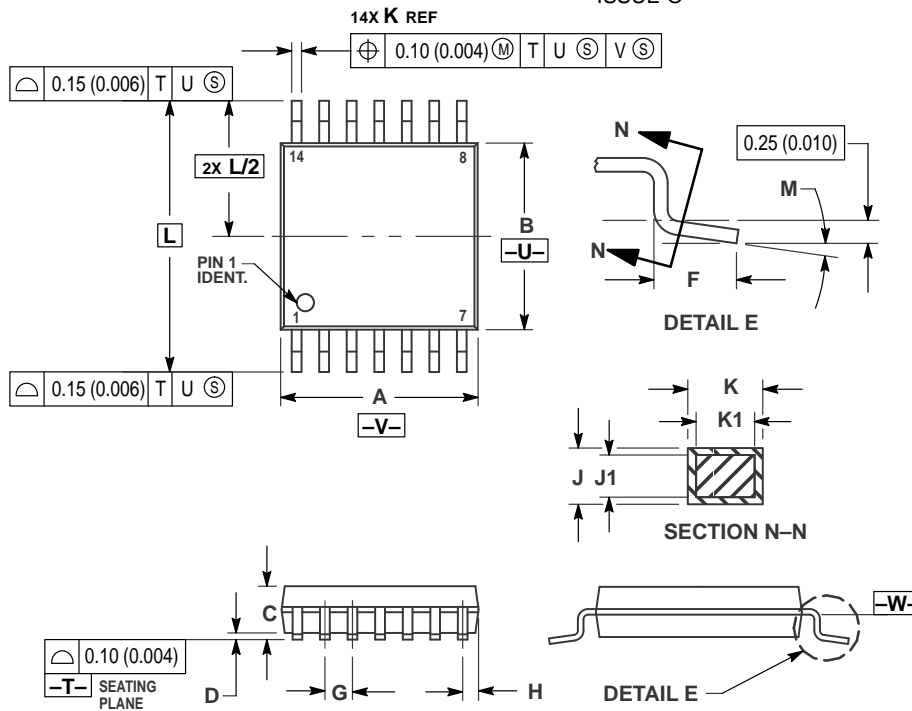


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

### DTB SUFFIX PLASTIC PACKAGE CASE 948G-01 (TSSOP-14) ISSUE O



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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