STK25C48

2K x 8 *AutoStore*™ nvSRAM *QuantumTrap*™ CMOS Nonvolatile Static RAM

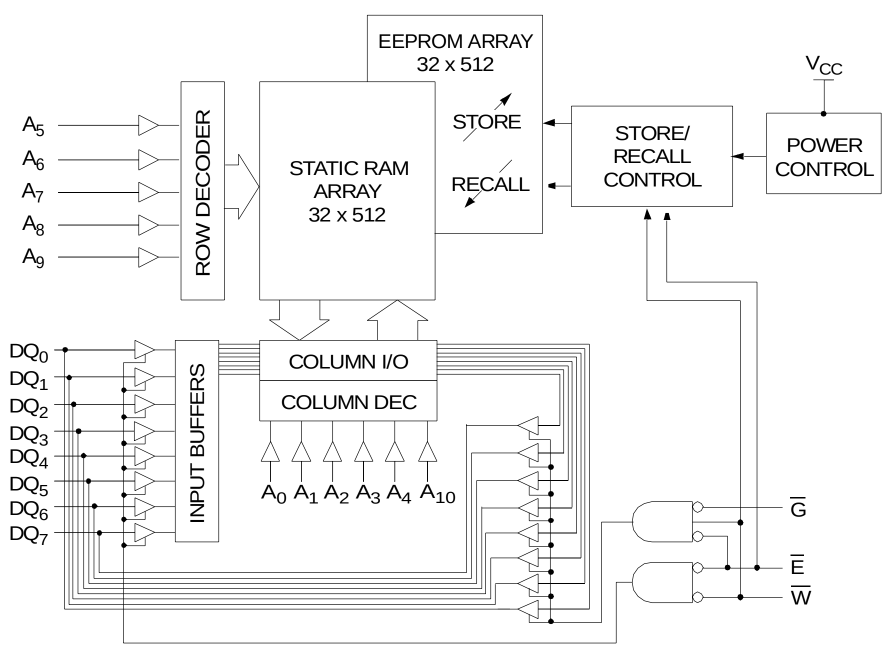
FEATURES

- **Nonvolatile Storage without Battery Problems**
- **Directly Replaces 2K x 8 Static RAM, Battery-Backed RAM or EEPROM**
- **20ns, 25ns, 35ns and 45ns Access Times**
- ***STORE* to EEPROM Initiated by *AutoStore*™ on Power Down**
- ***RECALL* to SRAM Initiated by Software or Power Restore**
- **10mA Typical I_{CC} at 200ns Cycle Time**
- **Unlimited READ, WRITE and *RECALL* Cycles**
- **1,000,000 *STORE* Cycles to EEPROM**
- **100-Year Data Retention over Full Industrial Temperature Range**
- **Commercial and Industrial Temperatures**
- **24-Pin 600 PDIP Package**

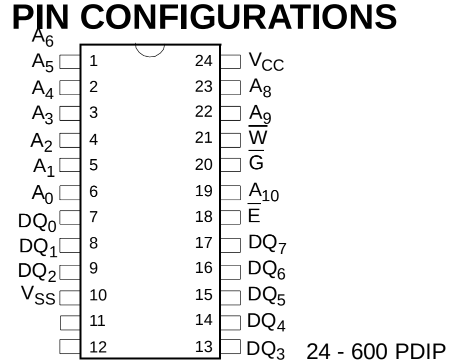
DESCRIPTION

The STK25C48 is a fast SRAM with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in the EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) can take place automatically on power down using charge stored in system capacitance. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. The nvSRAM can be used in place of existing 2K x 8 SRAMs and also matches the pinout of 2K x 8 battery-backed SRAMs, EPROMs and EEPROMs, allowing direct substitution while enhancing performance. There is no limit on the number of read or write cycles that can be executed, and no support circuitry is required for microprocessor interfacing.

BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

A_0 - A_{10}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Power (+ 5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to V_{SS} . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on $DQ_{0\text{-}7}$ . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . –55°C to 125°C
Storage Temperature . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)[b]

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[c]	Average V_{CC} Current		95 85 75 65		N/A 90 75 65	mA mA mA mA	t_{AVAV} = 20ns t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC_2}[d]	Average V_{CC} Current during *STORE*		3		3	mA	All Inputs Don't Care, V_{CC} = max
I_{CC_3}[c]	Average V_{CC} Current at t_{AVAV} = 200ns 5V, 25°C, Typical		10		10	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All Others Cycling, CMOS Levels
I_{CC_4}[d]	Average V_{CAP} Current during *AutoStore*™ Cycle		2		2	mA	All Inputs Don't Care
I_{SB_1}[e]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		30 25 21 18		N/A 26 22 19	mA mA mA mA	t_{AVAV} = 20ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$
I_{SB_2}[e]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1.5		1.5	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All Others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = – 4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: The STK25C48-20 requires V_{CC} = 5.0V ± 5% supply to operate at specified speed.
Note c: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note d: I_{CC_2} and I_{CC_4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note e: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input Pulse Levels . . . . 0V to 3V
Input Rise and Fall Times . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . See Figure 1

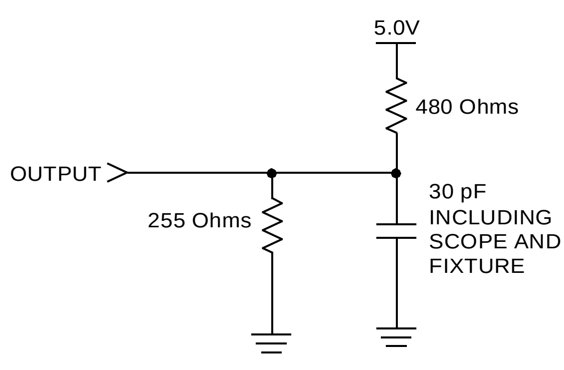


Figure 1: AC Output Loading

CAPACITANCE[f]

(T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.

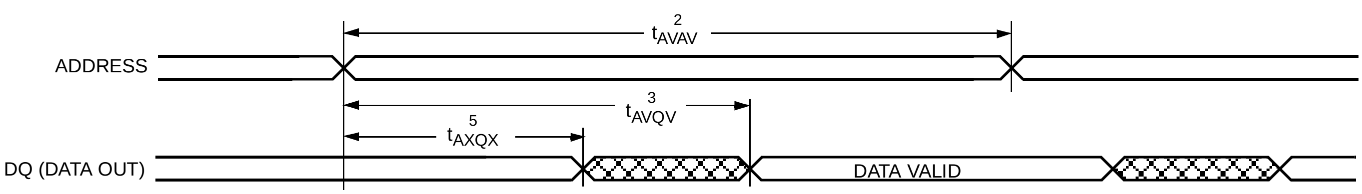
SRAM READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[b]

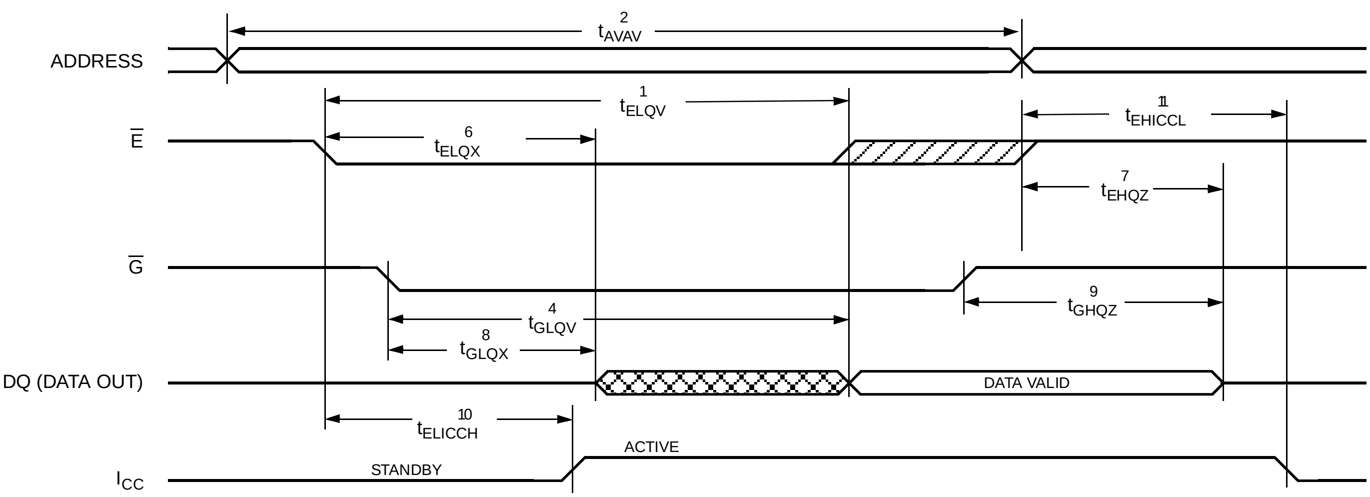
NO.	SYMBOLS		PARAMETER	STK25C48-20		STK25C48-25		STK25C48-35		STK25C48-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		20		25		35		45	ns
2	t_{AVAV}[g]	t_{RC}	Read Cycle Time	20		25		35		45		ns
3	t_{AVQV}[h]	t_{AA}	Address Access Time		22		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		8		10		15		20	ns
5	t_{AXQX}[h]	t_{OH}	Output Hold after Address Change	5		5		5		5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns
7	t_{EHQZ}[i]	t_{HZ}	Chip Disable to Output Inactive		7		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		0		ns
9	t_{GHQZ}[i]	t_{OHZ}	Output Disable to Output Inactive		7		10		13		15	ns
10	t_{ELICCH}[f]	t_{PA}	Chip Enable to Power Active	0		0		0		0		ns
11	t_{EHICCL}[e, f]	t_{PS}	Chip Disable to Power Standby		25		25		35		45	ns

Note g: $\overline{W}$ must be high during SRAM READ cycles and low during SRAM WRITE cycles.
Note h: I/O state assumes $\overline{E}$, $\overline{G} \le V_{IL}$ and $\overline{W} \ge V_{IH}$; device is continuously selected.
Note i: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[g, h]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[g]



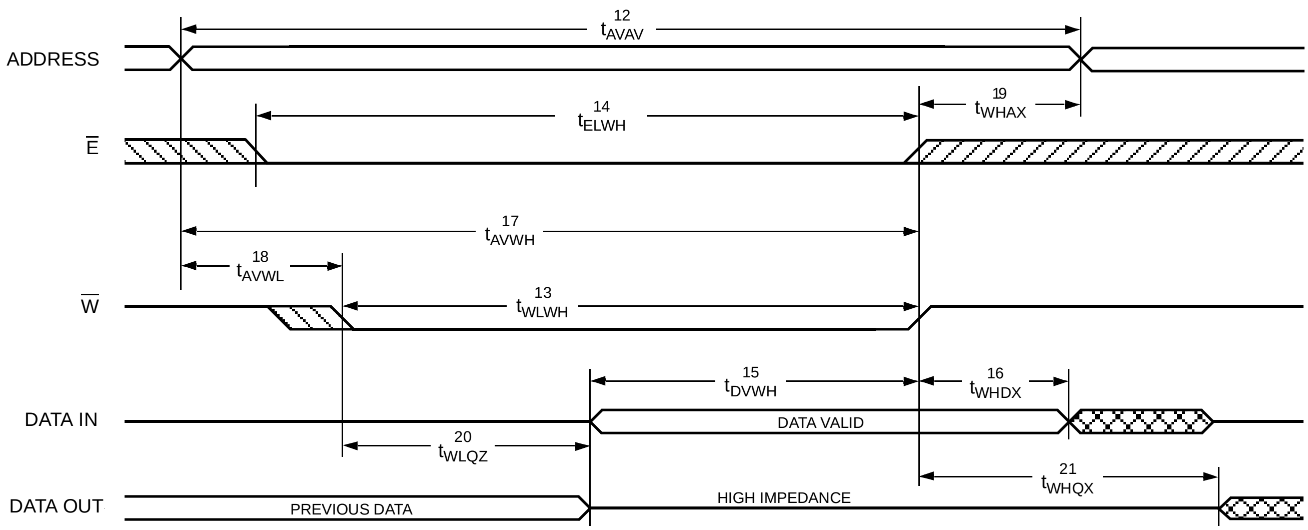
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)[b]

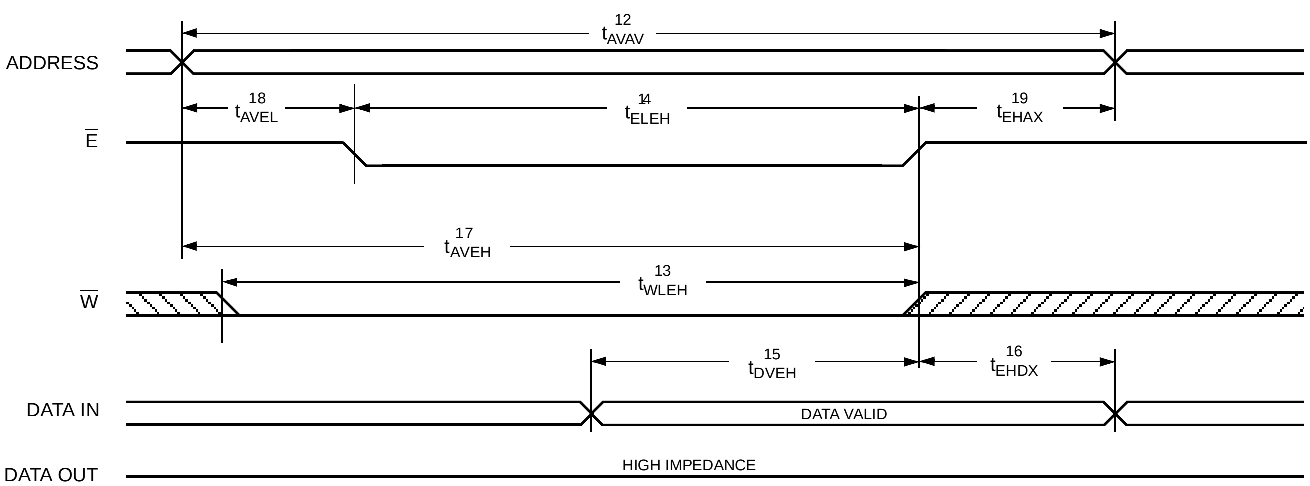
NO.	SYMBOLS #1	SYMBOLS #2	SYMBOLS Alt.	PARAMETER	STK25C48-20 MIN	STK25C48-20 MAX	STK25C48-25 MIN	STK25C48-25 MAX	STK25C48-35 MIN	STK25C48-35 MAX	STK25C48-45 MIN	STK25C48-45 MAX	UNITS
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	20		25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	15		20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	8		10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	15		20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		0		ns
20	t_{WLQZ}[i, j]		t_{WZ}	Write Enable to Output Disable		7		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		5		ns

Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[k]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[k]

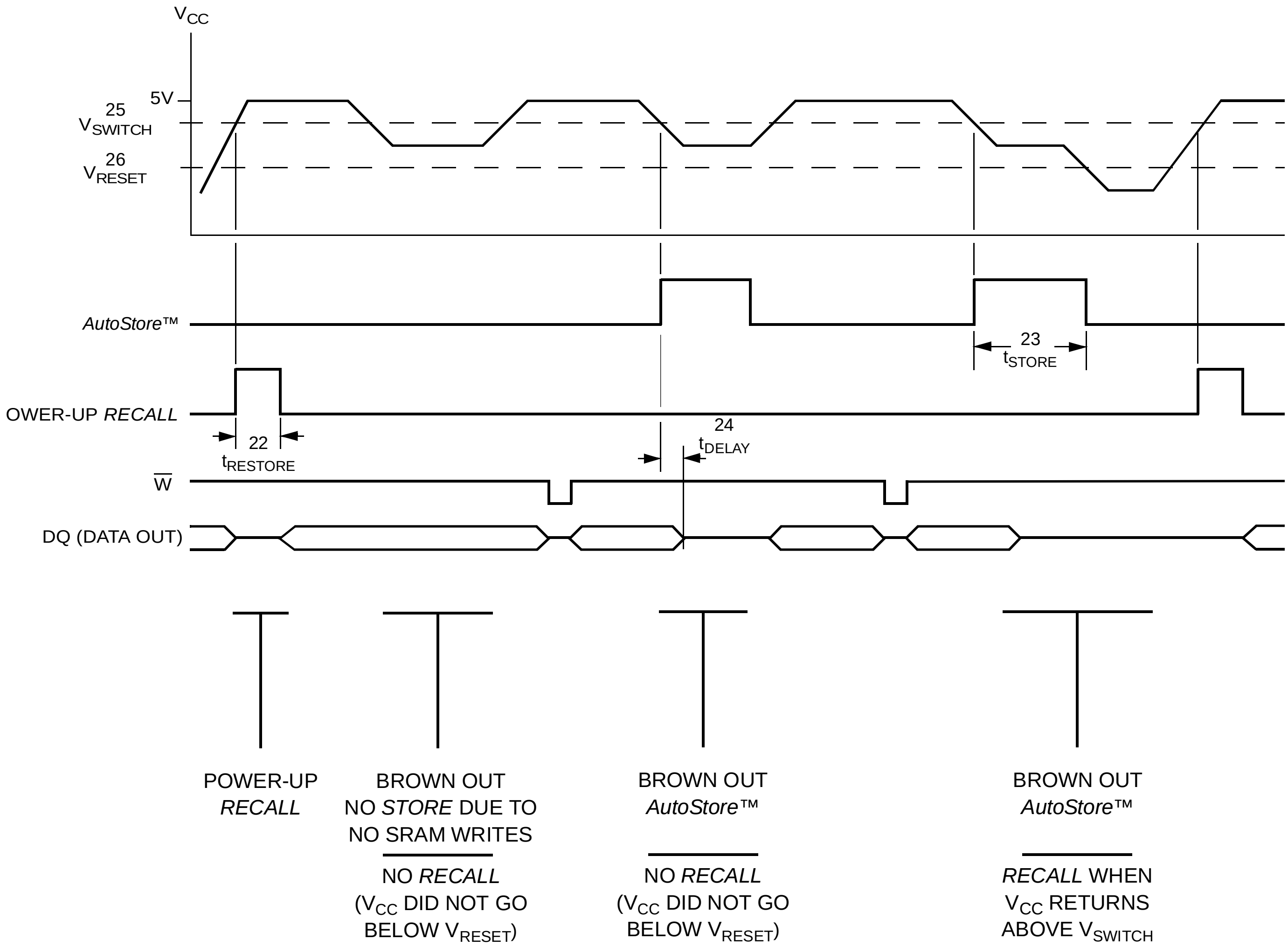


AutoStore™/POWER-UP *RECALL* (V_{CC} = 5.0V ± 10%)[b]

NO.	SYMBOLS	PARAMETER	STK25C48		UNITS	NOTES
	Standard		MIN	MAX		
22	$t_{RESTORE}$	Power-up *RECALL* Duration		550	µs	l
23	t_{STORE}	*STORE* Cycle Duration		10	ms	h
24	t_{DELAY}	Time Allowed to Complete SRAM Cycle	1		µs	h
25	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	
26	V_{RESET}	Low Voltage Reset Level		3.6	V	f

Note l: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

AutoStore™/POWER-UP *RECALL*



DEVICE OPERATION

The STK25C48 is a versatile memory chip that provides several modes of operation. The STK25C48 can operate as a standard 8K x 8 SRAM. It has an 8K x 8 EEPROM shadow to which the SRAM information can be copied, or from which the SRAM can be updated in nonvolatile mode.

NOISE CONSIDERATIONS

Note that the STK25C48 is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK25C48 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-10} determines which of the 2,048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high or $\overline{W}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

AutoStore™ OPERATION

The STK25C48 uses the intrinsic system capacitance to perform an automatic store on power down. As long as the system power supply takes at least t_{STORE} to decay from V_{SWITCH} down to 3.6V, the STK25C48 will safely and automatically store the SRAM data in EEPROM on power down.

In order to prevent unneeded *STORE* operations, automatic *STORE* will be ignored unless at least one WRITE operation has taken place since the most recent *STORE* or *RECALL* cycle.

POWER-UP *RECALL*

During power up, or after any low-power condition ($V_{CC} < V_{RESET}$), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK25C48 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

HARDWARE PROTECT

The STK25C48 offers hardware protection against inadvertent *STORE* operation and SRAM WRITEs during low-voltage conditions. When $V_{CC} < V_{SWITCH}$, *STORE* operations and SRAM WRITEs are inhibited.

LOW AVERAGE ACTIVE POWER

The STK25C48 draws significantly less current when it is cycled at times longer than 50ns. Figure 2 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK25C48 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

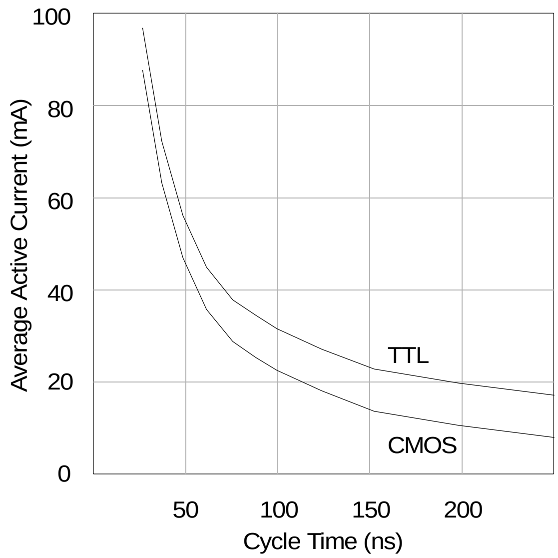


Figure 2: I_{CC} (max) Reads

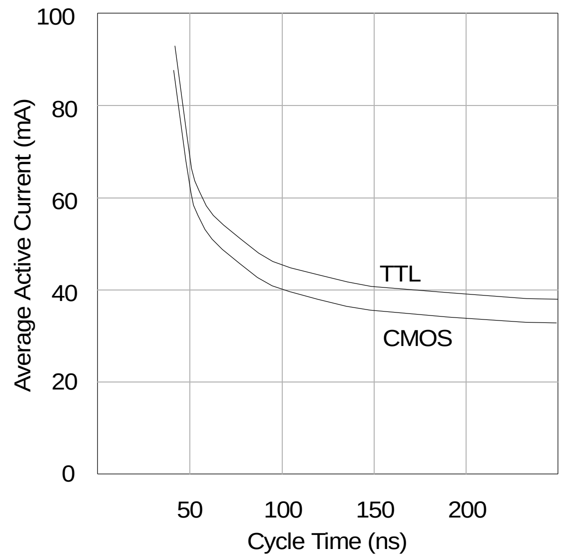


Figure 3: I_{CC} (max) Writes

ORDERING INFORMATION

STK25C48 - W 25 I

Temperature Range
- Blank = Commercial (0 to 70°C)
- I = Industrial (–40 to 85°C)

Access Time
- 20 = 20ns (Commercial only)
- 25 = 25ns
- 35 = 35ns
- 45 = 45ns

Package
- W = Plastic 24-pin 600 mil DIP