Data Sheet August 1999 File Number 4771

100MHz, Single and Dual Low Noise, Precision Operational Amplifier

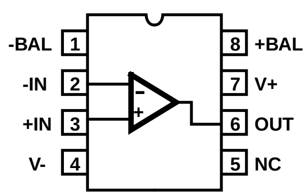
The HCA10009 is a high performance dielectrically isolated, op amp, featuring precision DC characteristics while providing excellent AC characteristics. Designed for audio, video, and other demanding applications, noise (3.4nV/$\sqrt{Hz}$ at 1kHz), total harmonic distortion (<0.005%), and DC errors are kept to a minimum.

The precision performance is shown by low offset voltage (0.3mV), low bias currents (40nA), low offset currents (15nA), and high open loop gain (128dB). The combination of these excellent DC characteristics with the fast settling time (0.4µs) make the HCA10009 ideally suited for precision signal conditioning.

The unique design of the HCA10009 gives it outstanding AC characteristics not normally associated with precision op amps, high unity gain bandwidth (35MHz) and high slew rate (25V/µs). Other key specifications include high CMRR (95dB) and high PSRR (100dB). The combination of these specifications will allow the HCA10009 to be used in RF signal conditioning as well as video amplifiers.

Pinout

HCA10009
(SOIC)
TOP VIEW



Features

- Gain Bandwidth Product. 100MHz
- Unity Gain Bandwidth. 25MHz
- Slew Rate 25V/µs
- Low Offset Voltage 0.3mV
- High Open Loop Gain. 128dB
- Channel Separation at 10kHz 110dB
- Low Noise Voltage at 1kHz. . . . . 3.4nV/$\sqrt{Hz}$
- High Output Current 56mA
- Low Supply Current per Amplifier. 8mA

Applications

- Precision Test Systems
- Active Filtering
- Small Signal Video
- Accurate Signal Processing
- RF Signal Conditioning

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HCA10009	0 to 75	8 Ld SOIC	M8.15

Absolute Maximum Ratings

Supply Voltage Between V+ and V- Terminals 35V
Differential Input Voltage (Note 1) 5V
Output Current Short Circuit Duration . . . . Indefinite

Operating Conditions

Temperature Range . . . .
HCA10009 . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} ($^oC/W$)
8 Ld SOIC Package 157
Maximum Junction Temperature (Plastic Package) . . . . 150^oC
Maximum Storage Temperature Range . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input is protected by back-to-back zener diodes. See applications section.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	HCA10009			UNITS
			MIN	TYP	MAX	
INPUT CHARACTERISTICS						
Input Offset Voltage		25	-	0.30	0.75	mV
		Full	-	0.35	1.5	mV
Average Offset Voltage Drift		Full	-	0.5	-	$\mu V/^oC$
Input Bias Current		25	-	40	100	nA
		Full	-	70	200	nA
Input Offset Current		25	-	15	100	nA
		Full	-	30	150	nA
Input Offset Voltage Match		25	-	400	750	μV
		Full	-	-	1500	μV
Common Mode Range		25	±12	-	-	V
Differential Input Resistance		25	-	70	-	kΩ
Input Noise Voltage	f = 0.1Hz to 10Hz	25	-	0.25	-	μV_{P-P}
Input Noise Voltage	f = 10Hz	25	-	6.2	10	$nV/\sqrt{Hz}$
Density (Notes 3, 12)	f = 100Hz	25	-	3.6	6	$nV/\sqrt{Hz}$
	f = 1000Hz	25	-	3.4	4.0	$nV/\sqrt{Hz}$
Input Noise Current	f = 10Hz	25	-	4.7	8.0	$pA/\sqrt{Hz}$
Density (Notes 3, 12)	f = 100Hz	25	-	1.8	2.8	$pA/\sqrt{Hz}$
	f = 1000Hz	25	-	0.97	1.8	$pA/\sqrt{Hz}$
THD+N	Note 4	25	-	<0.005	-	%
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	Note 5	25	106	128	-	dB
		Full	100	120	-	dB
CMRR	$V_{CM} = \pm10V$	Full	86	95	-	dB
Unity Gain Bandwidth	-3dB	25	-	35	-	MHz
Gain Bandwidth Product	1kHz to 400kHz	25	-	100	-	MHz
Minimum Stable Gain		Full	1	-	-	V/V

Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HCA10009 MIN	HCA10009 TYP	HCA10009 MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 333Ω	Full	±10	-	-	V
	R_L = 1kΩ	25	±12	±12.5	-	V
	R_L = 1kΩ	Full	±11.5	±12.1	-	V
Output Current	V_{OUT} = ±10V	Full	±30	±56	-	mA
Output Resistance		25	-	10	-	Ω
Full Power Bandwidth	Note 6	25	239	398	-	kHz
TRANSIENT RESPONSE (Note 10)						
Slew Rate	Notes 7, 11	Full	15	25	-	V/µs
Rise Time	Notes 8, 11	Full	-	13	20	ns
Overshoot	Notes 8, 11	Full	-	28	50	%
Settling Time (Note 9)	0.1%	25	-	0.4	-	µs
	0.01%	25	-	1.5	-	µs
POWER SUPPLY						
PSRR	V_S = ±10V to ±20V	Full	86	100	-	dB
Supply Current		Full	-	8	11	mA/Op Amp

NOTES:

3. Refer to typical performance curve in data sheet.
4. A_{VCL} = 10, f_O = 1kHz, V_O = $5V_{RMS}$, R_L = 600Ω, 10Hz to 100kHz, Minimum resolution of test equipment is 0.005%.
5. V_{OUT} = 0 to ±10V, R_L = 1kΩ, C_L = 50pF.
6. Full Power Bandwidth is calculated by: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}, V_{PEAK} = 10V$.
7. V_{OUT} = ±2.5V, R_L = 1kΩ, C_L = 50pF.
8. V_{OUT} = ±100mV, R_L = 1kΩ, C_L = 50pF.
9. Settling time is specified for a 10V step and A_V = -1.
10. See Test Circuits.
11. Guaranteed by characterization.

Test Circuits and Waveforms

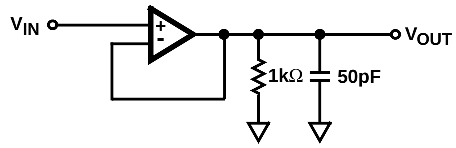
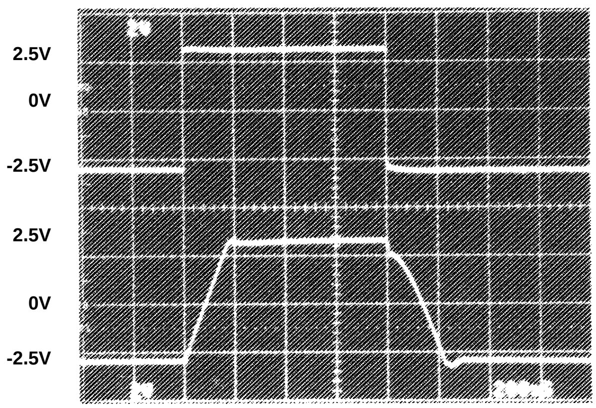
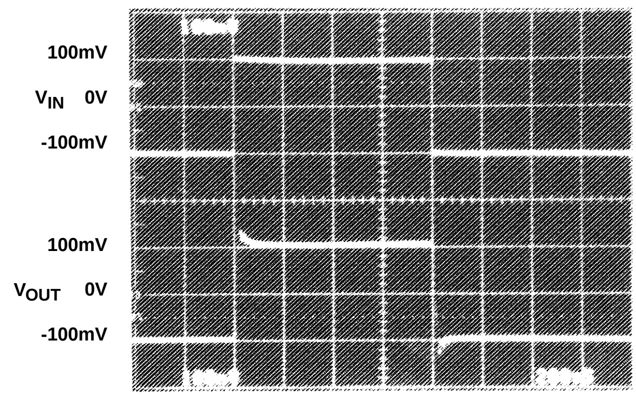


FIGURE 1. TRANSIENT RESPONSE TEST CIRCUIT



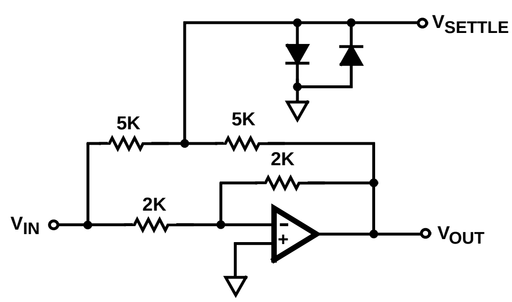
V_{OUT} = 2.5V
Vertical Scale = 2V/Div.,
Horizontal Scale = 200ns/Div.

FIGURE 2. LARGE SIGNAL RESPONSE



V_{OUT} = ±100mV
Vertical Scale = 100mV/Div.,
Horizontal Scale = 200ns/Div.

FIGURE 3. SMALL SIGNAL RESPONSE



NOTES:

12. A_V = -1.
13. Feedback and summing resistors must be matched (0.1%).
14. HP5082-2810 clipping diodes recommended.
15. Tektronix P6201 FET probe used at settling point.

FIGURE 4. SETTLING TIME TEST CIRCUIT

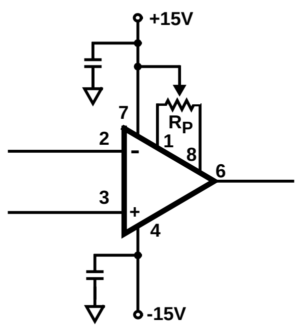
Application Information

Operation at Various Supply Voltages

The HCA10009 operates over a wide range of supply voltages with little variation in performance. The supplies may be varied from ±5V to ±15V. See Typical Performance Curves for variations in supply current, slew rate and output voltage swing.

Offset Adjustment

The following diagram shows the offset voltage adjustment configuration for the HCA10009. By moving the potentiometer wiper towards pin 8 (+BAL), the op amps output voltage will increase; towards pin 1 (-BAL) decreases the output voltage. A 20kΩ trim pot will allow an offset voltage adjustment of about 10mV.



Capacitive Loading Considerations

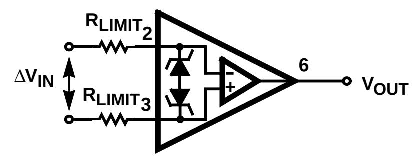
When driving capacitive loads >80pF, a small resistor, 50Ω to 100Ω, should be connected in series with the output and inside the feedback loop.

Saturation Recovery

When an op amp is over driven, output devices can saturate and sometimes take a long time to recover. By clamping the input, output saturation can be avoided. If output saturation can not be avoided, the maximum recovery time when overdriven into the positive rail is 10.6µs. When driven into the negative rail the maximum recovery time is 3.8µs.

Input Protection

The HCA10009 has built in back-to-back protection diodes which limit the maximum allowable differential input voltage to approximately 5V. If the HCA10009 will be used in circuits where the maximum differential voltage may be exceeded, then current limiting resistors must be used. The input current should be limited to a maximum of 10mA.



PC Board Layout Guidelines

When designing with the HCA10009, good high frequency (RF) techniques should be used when building a PC board. Use of ground plane is recommended. Power supply decoupling is very important. A 0.01µF to 0.1µF high quality ceramic capacitor at each power supply pin with a 2.2µF to 10µF tantalum close by will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and basically no lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance.

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$

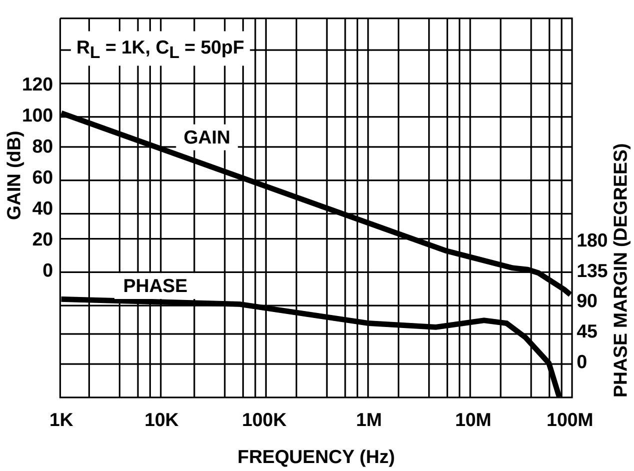


FIGURE 5. OPEN LOOP GAIN AND PHASE vs FREQUENCY

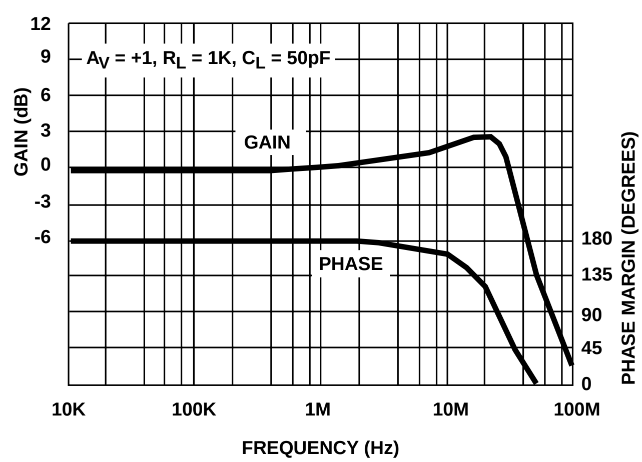


FIGURE 6. CLOSED LOOP GAIN vs FREQUENCY

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$ **(Continued)**

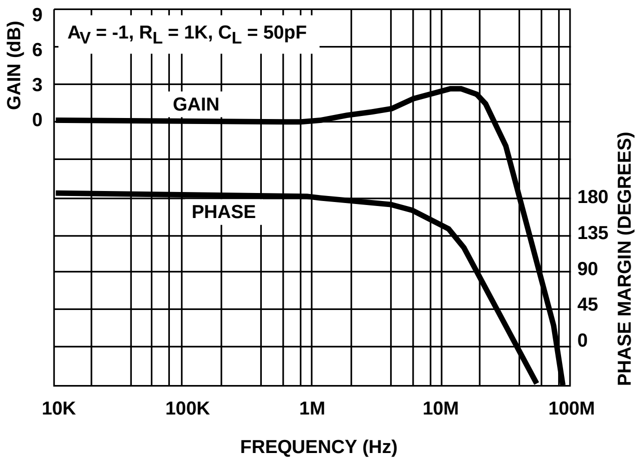


FIGURE 7. CLOSED LOOP GAIN vs FREQUENCY

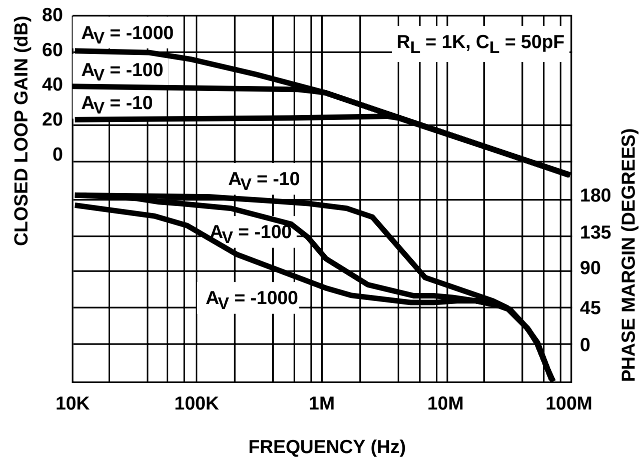


FIGURE 8. VARIOUS CLOSED LOOP GAINS vs FREQUENCY

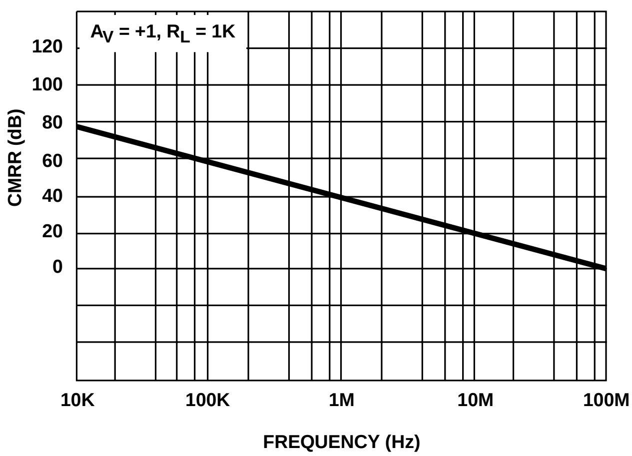


FIGURE 9. CMRR vs FREQUENCY

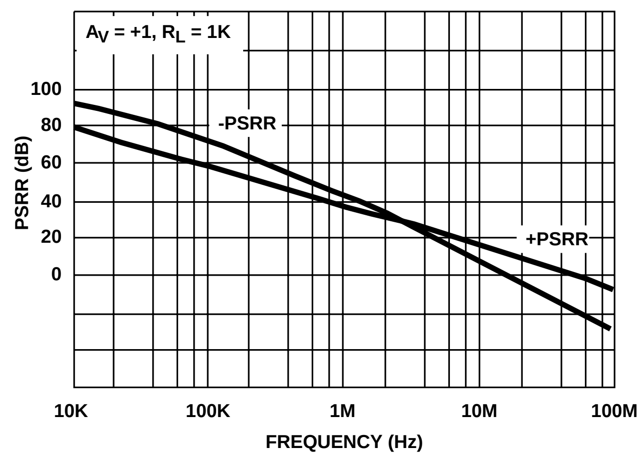


FIGURE 10. PSRR vs FREQUENCY

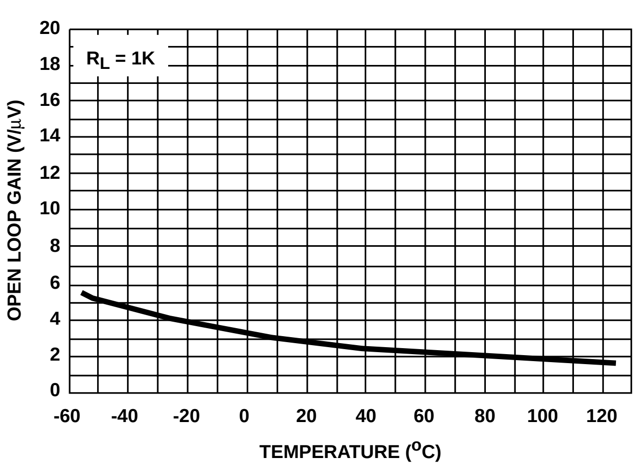


FIGURE 11. OPEN LOOP GAIN vs TEMPERATURE

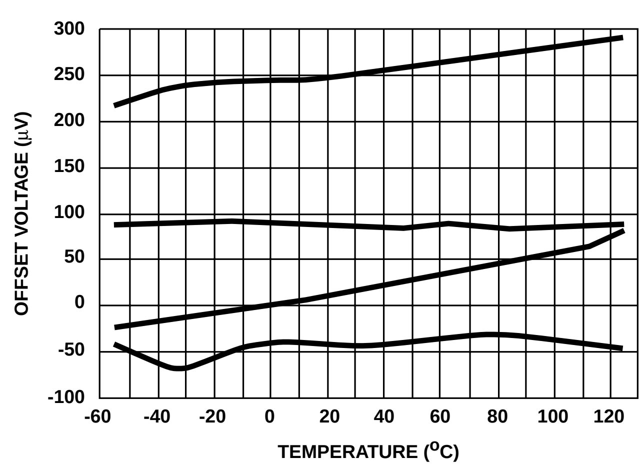


FIGURE 12. OFFSET VOLTAGE vs TEMPERATURE (4 REPRESENTATIVE UNITS)

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$ **(Continued)**

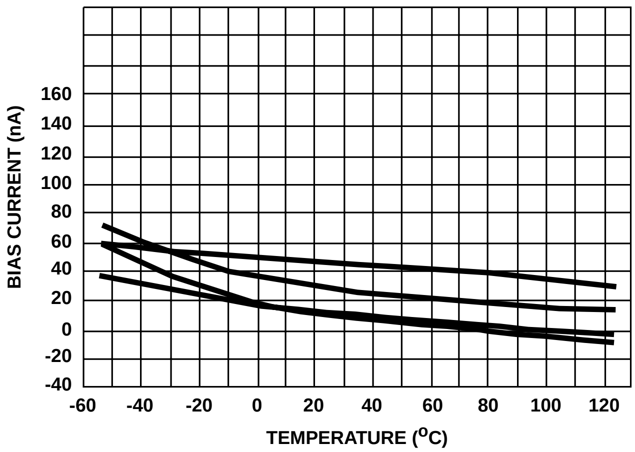


FIGURE 13. BIAS CURRENT vs TEMPERATURE (4 REPRESENTATIVE UNITS)

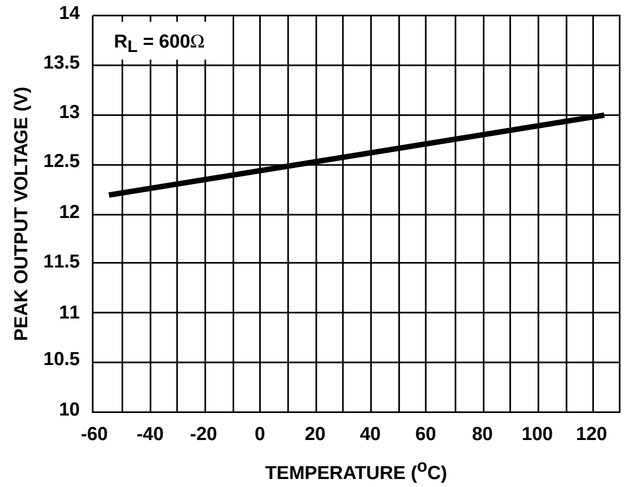


FIGURE 14. OUTPUT VOLTAGE SWING vs TEMPERATURE

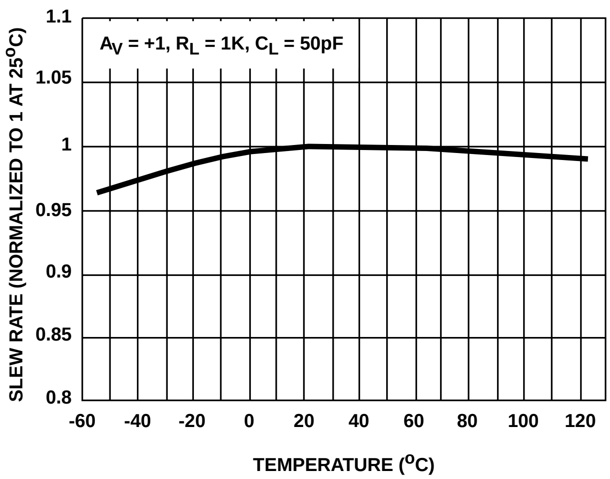


FIGURE 15. SLEW RATE vs TEMPERATURE

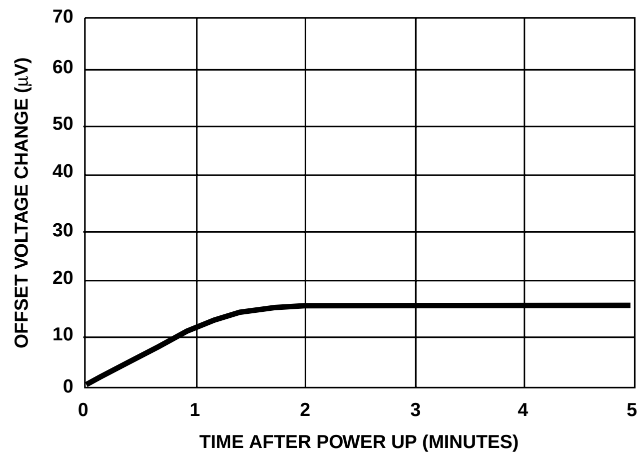


FIGURE 16. OFFSET VOLTAGE WARM-UP DRIFT

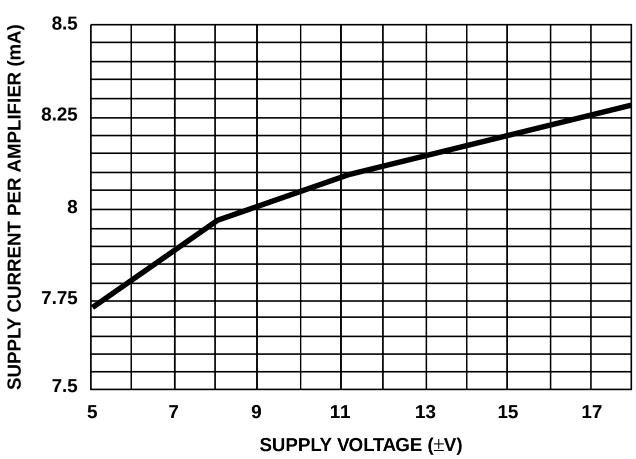


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

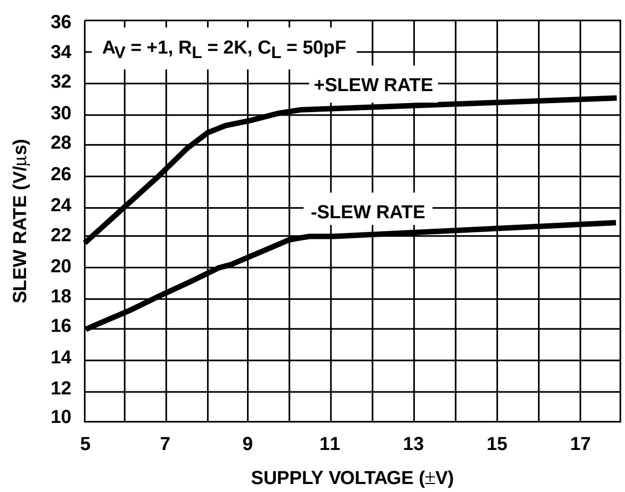


FIGURE 18. SLEW RATE vs SUPPLY VOLTAGE

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$ (Continued)

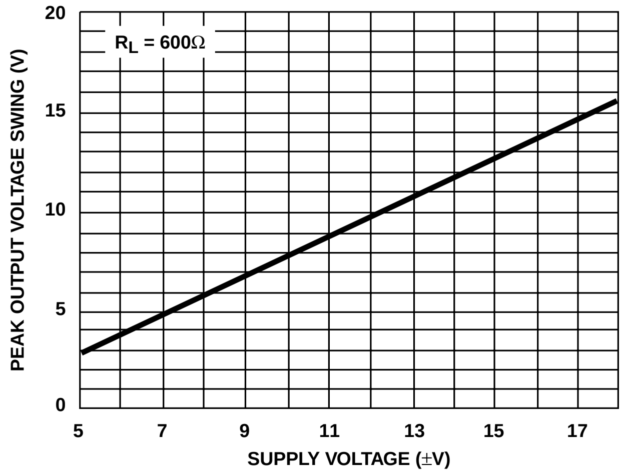


FIGURE 19. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

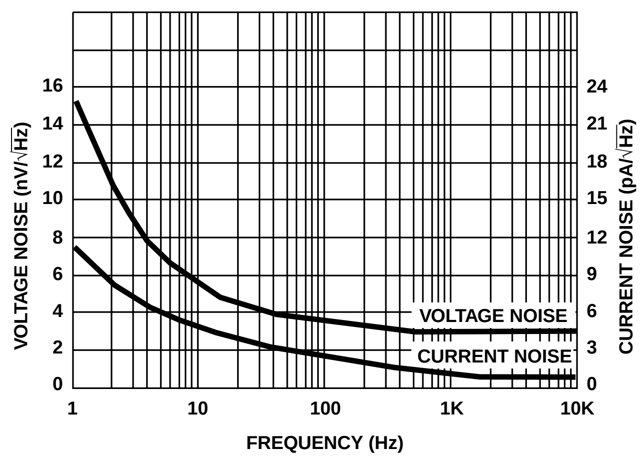


FIGURE 20. NOISE CHARACTERISTICS

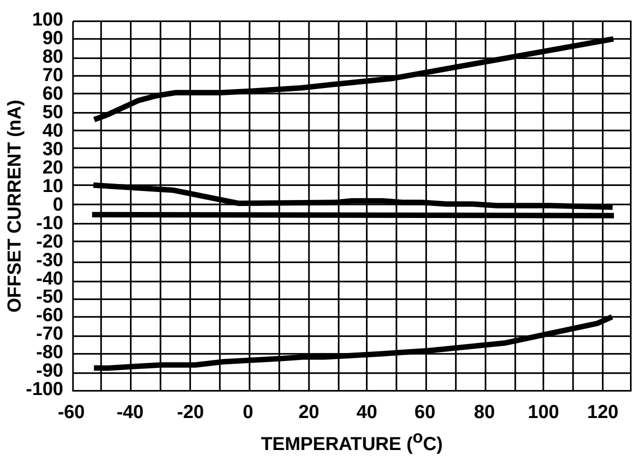


FIGURE 21. OFFSET CURRENT vs TEMPERATURE (4 REPRESENTATIVE UNITS)

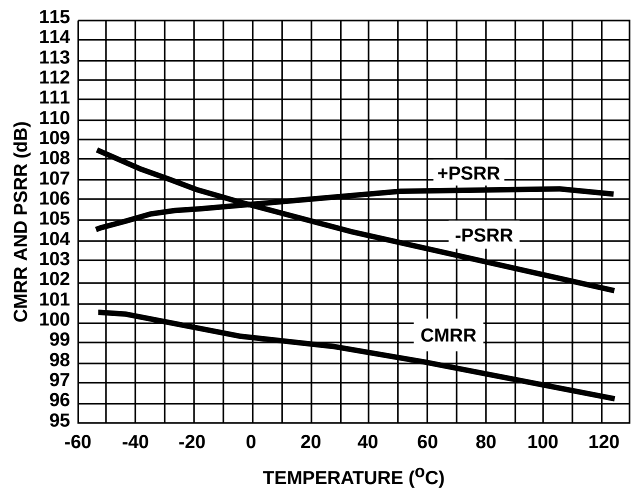


FIGURE 22. CMRR AND PSRR vs TEMPERATURE

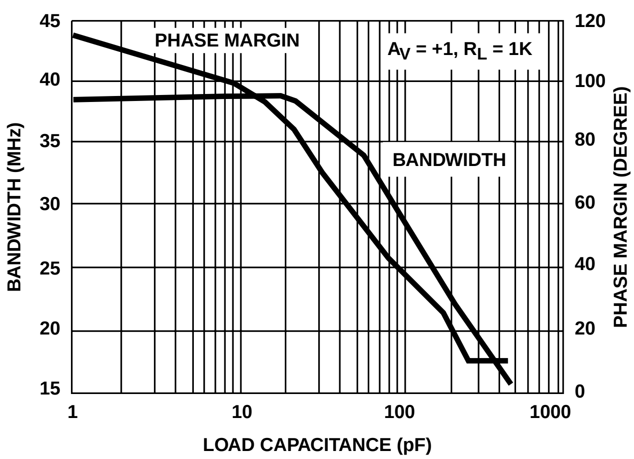


FIGURE 23. BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

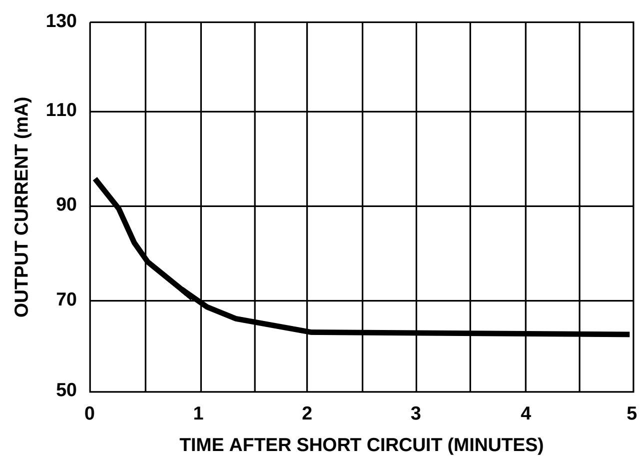
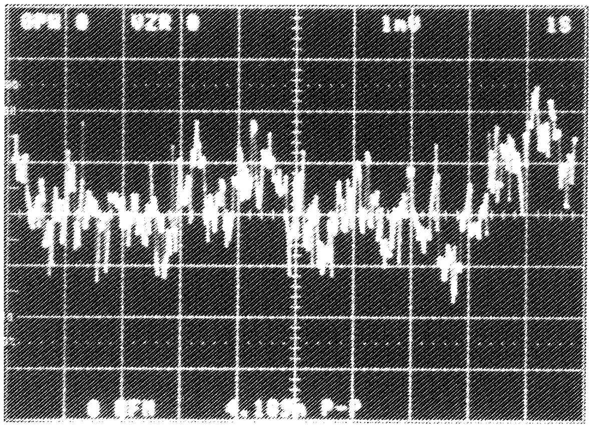


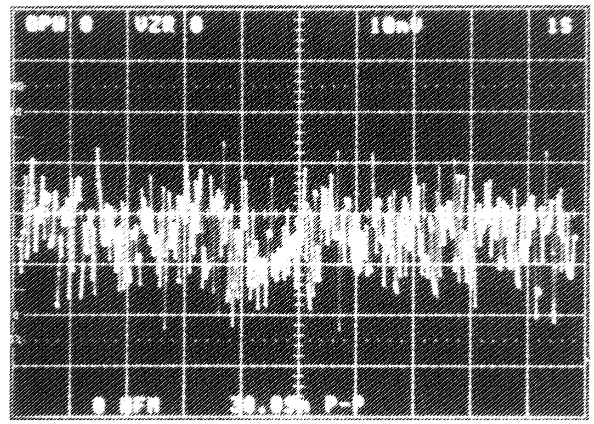
FIGURE 24. SHORT CIRCUIT OUTPUT CURRENT vs TIME

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$ **(Continued)**



Vertical Scale = 1mV/Div.; Horizontal Scale = 1s/Div.
A_V = +25,000; E_N = 0.168µV_{P-P} RTI

FIGURE 25. 0.1Hz TO 10Hz NOISE



Vertical Scale = 10mV/Div.; Horizontal Scale = 1s/Div.
A_V = +25,000; E_N = 1.5µV_{P-P} RTI

FIGURE 26. 0.1Hz TO 1MHz

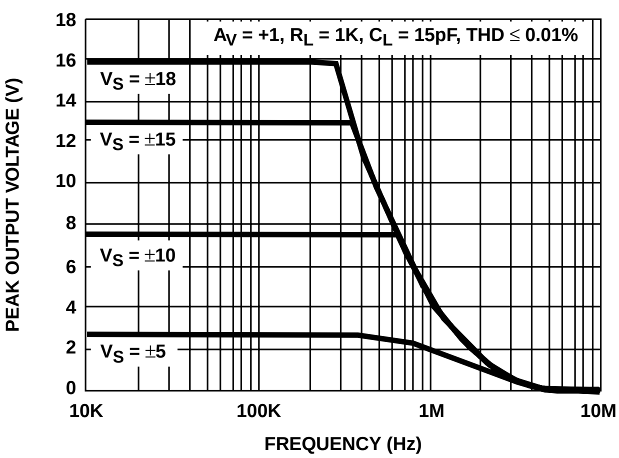


FIGURE 27. OUTPUT VOLTAGE SWING vs FREQUENCY

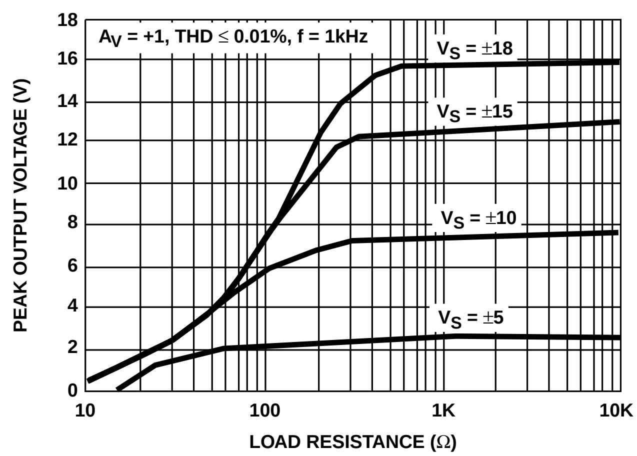


FIGURE 28. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

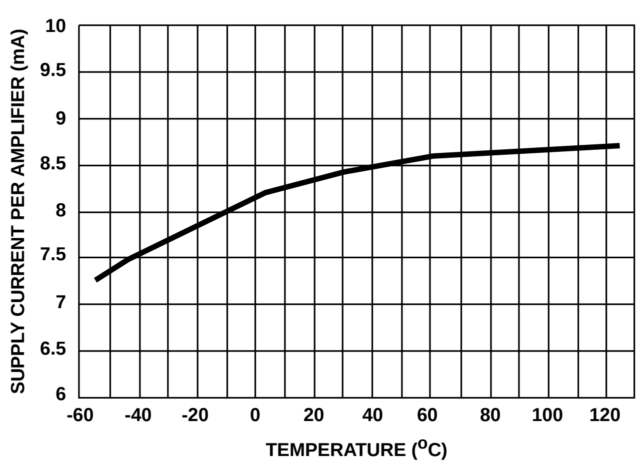
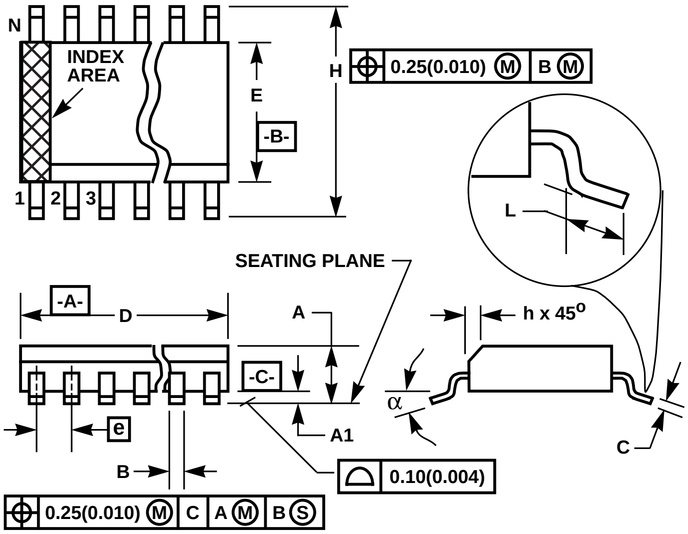


FIGURE 29. SUPPLY CURRENT/AMPLIFIER vs TEMPERATURE

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 **(JEDEC MS-012-AA ISSUE C)**
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

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