



Integrated Device Technology, Inc.

# CMOS STATIC RAM 64K (64K x 1-BIT)

IDT7187S  
IDT7187L

### FEATURES:

- High speed (equal access and cycle time)
  - Military: 25/35/45/55/70/85ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin ceramic DIP, 22-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B

### DESCRIPTION:

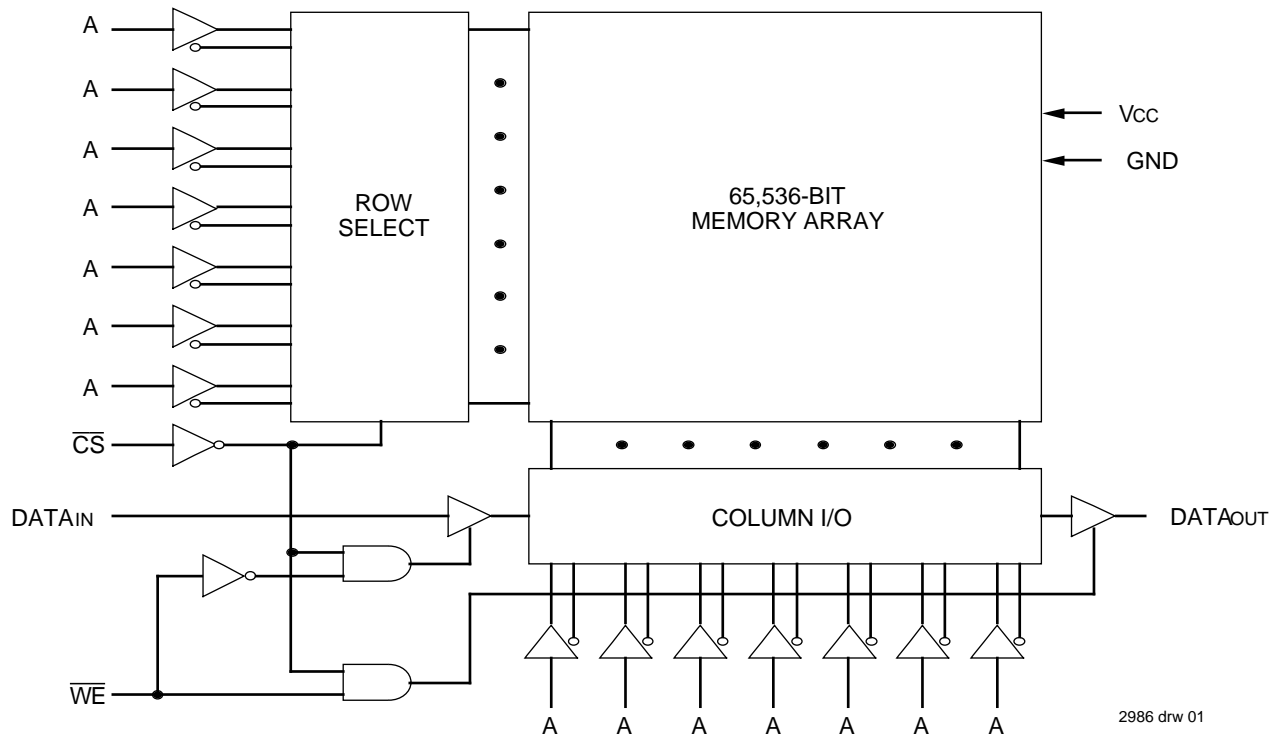
The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability CMOS technology. Access times as fast as 25ns are available.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—ISB and ISB1. ISB provides low-power operation; ISB1 provides ultra-low-power operation. The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30μW.

Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil ceramic DIP, or 22-pin leadless chip carriers.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

### FUNCTIONAL BLOCK DIAGRAM

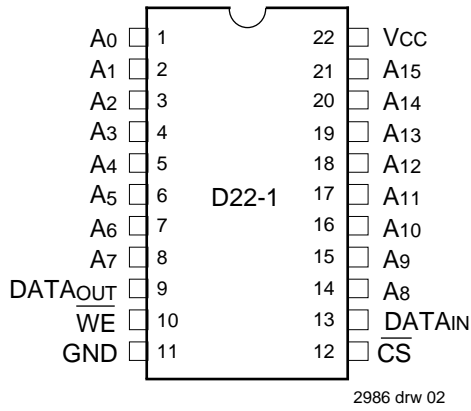


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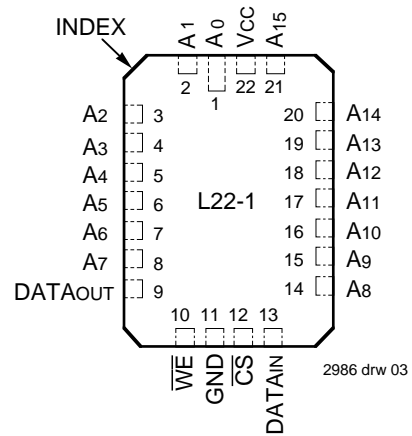
**MILITARY TEMPERATURE RANGE**

**AUGUST 1996**

## PIN CONFIGURATIONS



**DIP  
TOP VIEW**



**22-PIN LCC  
TOP VIEW**

## PIN DESCRIPTIONS

Name	Description
A0–A15	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
VCC	Power
DATAIN	Data Input
DATAOUT	Data Output
GND	Ground

2986 tbl 01

## TRUTH TABLE<sup>(1)</sup>

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DOUT	Active
Write	L	L	High-Z	Active

**NOTE:**

1. H =  $V_{IH}$ , L =  $V_{IL}$ , X = don't care.

2986 tbl 02

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

**NOTE:** 2986 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	pF

**NOTE:** 2986 tbl 04

- This parameter is determined by device characterization, but is not production tested.

### RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:** 2986 tbl 05

- V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns, once per cycle.

### RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V <sub>CC</sub>
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2986 tbl 06

### DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7187S		IDT7187L		Unit	
			Min.	Max.	Min.	Max.		
I <sub>L</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	MIL.	—	10	—	5	μA
			COM'L.	—	5	—	2	
I <sub>O</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>	MIL.	—	10	—	5	μA
			COM'L.	—	5	—	2	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 10mA, V <sub>CC</sub> = Min.	—	0.5	—	0.5	V	
		I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	—	0.4	—	0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	—	2.4	—	V	

2986 tbl 07

### DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

(VCC = 5V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	Power	7187S25 7187L25		7187S35 7187L35		7187S45 7187L45		7187S55/70 7187L55/70		7187S85 7187L85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current CS = VIL, Outputs Open VCC = Max., f = 0 <sup>(2)</sup>	S	—	105	—	105	—	105	—	105	—	105	mA
		L	—	85	—	85	—	85	—	85	—	85	
ICC2	Dynamic Operating Current CS = VIL, Outputs Open VCC = Max., f = fMAX <sup>(2)</sup>	S	—	130	—	120	—	120	—	120	—	120	mA
		L	—	110	—	100	—	95	—	90	—	90	
ISB	Standby Power Supply Current (TTL Level) CS ≥ VIH, VCC = Max., Outputs Open, f = fMAX <sup>(2)</sup>	S	—	55	—	50	—	50	—	50	—	50	mA
		L	—	50	—	40	—	35	—	30/28	—	28	
ISB1	Full Standby Power Supply Current (CMOS Level) CS ≥ VHC, VCC = Max., VIN ≥ VHC or VIN ≤ VLC, f = 0 <sup>(2)</sup>	S	—	20	—	20	—	20	—	20	—	20	mA
		L	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

**NOTES:**

- All values are maximum guaranteed values.
- At f = fMAX address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.

2986 tbl 08

### DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) VHC = VCC - 0.2V, VLC = 0.2V

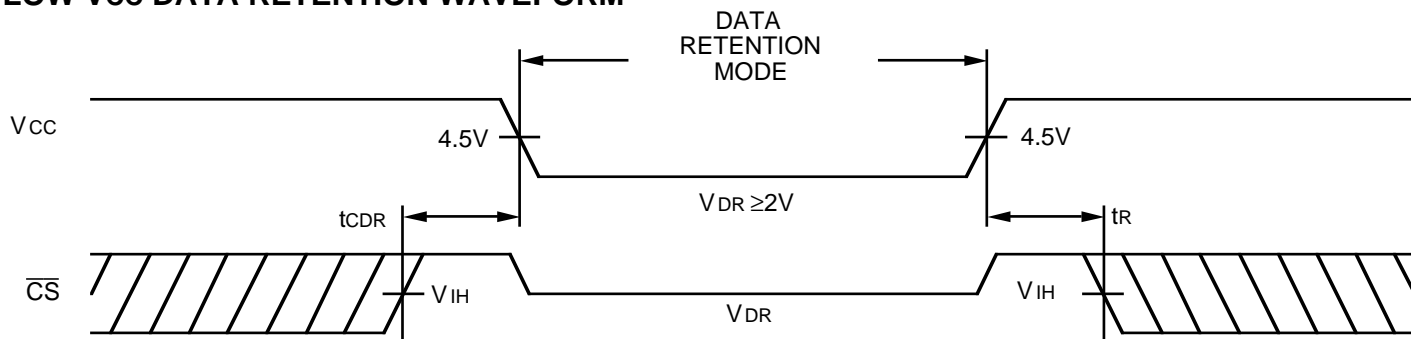
Symbol	Parameter	Test Condition	Min.	Typ. <sup>(1)</sup> Vcc @		Max. Vcc @		Unit
				2.0v	3.0V	2.0V	3.0V	
VDR	VCC for Data Retention	—	2.0	—	—	—	—	V
ICCDR	Data Retention Current	MIL. COM'L.	—	10	15	600	900	μA
			—	10	15	150	225	
tCDR <sup>(3)</sup>	Chip Deselect to Data Retention Time	CS ≥ VHC VIN ≥ VHC or ≤ VLC	0	—	—	—	—	ns
tr <sup>(3)</sup>	Operation Recovery Time		trc <sup>(2)</sup>	—	—	—	—	ns
ILI  <sup>(3)</sup>	Input Leakage Current		—	—	—	2	2	μA

**NOTES:**

- TA = +25°C.
- trc = Read Cycle Time.
- This parameter is guaranteed, but not tested.

2986 tbl 09

### LOW VCC DATA RETENTION WAVEFORM



2986 drw 04

### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2986 tbl 10

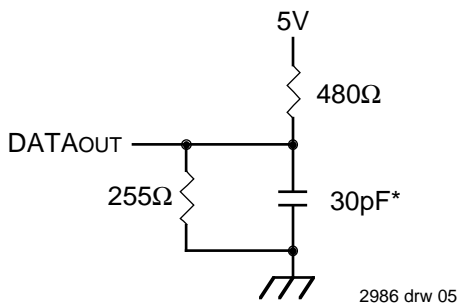


Figure 1. AC Test Load

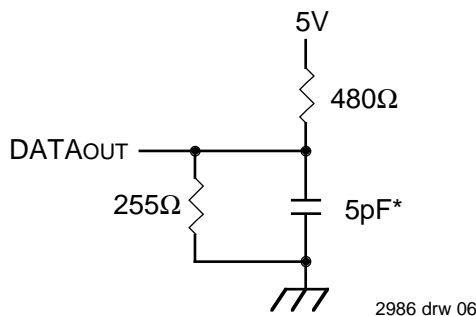


Figure 2. AC Test Load  
(for tHZ, tLZ, twz and tow)

\*Includes scope and jig capacitances

### AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%, All Temperature Ranges)

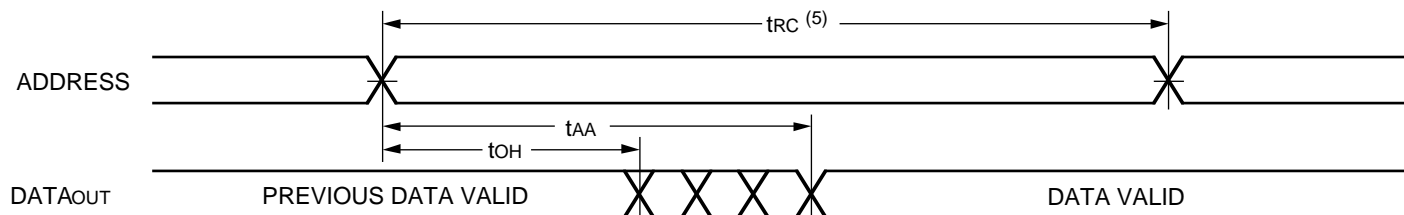
Symbol	Parameter	7187S25 7187L25		7187S35/45 <sup>(1)</sup> 7187L35/45 <sup>(1)</sup>		7187S55 <sup>(1)</sup> 7187L55 <sup>(1)</sup>		7187S70 <sup>(1)</sup> 7187L70 <sup>(1)</sup>		7187S85 <sup>(1)</sup> 7187L85 <sup>(1)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	25	—	35/45	—	55	—	70	—	85	—	ns
t <sub>AA</sub>	Address Access Time	—	25	—	35/45	—	55	—	70	—	85	ns
t <sub>ACS</sub>	Chip Select Access Time	—	25	—	35/45	—	55	—	70	—	85	ns
t <sub>OH</sub>	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t <sub>LZ</sub> <sup>(2)</sup>	Output Selection to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
t <sub>HZ</sub> <sup>(2)</sup>	Chip Deselect to Output in High-Z	—	12	—	17/20	—	30	—	30	—	40	ns
t <sub>PU</sub> <sup>(2)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(2)</sup>	Chip Deselect to Power-Down Time	—	20	—	30/35	—	35	—	35	—	40	ns

**NOTES:**

1. -55°C to +125°C temperature range only.
2. This parameter guaranteed but not tested.

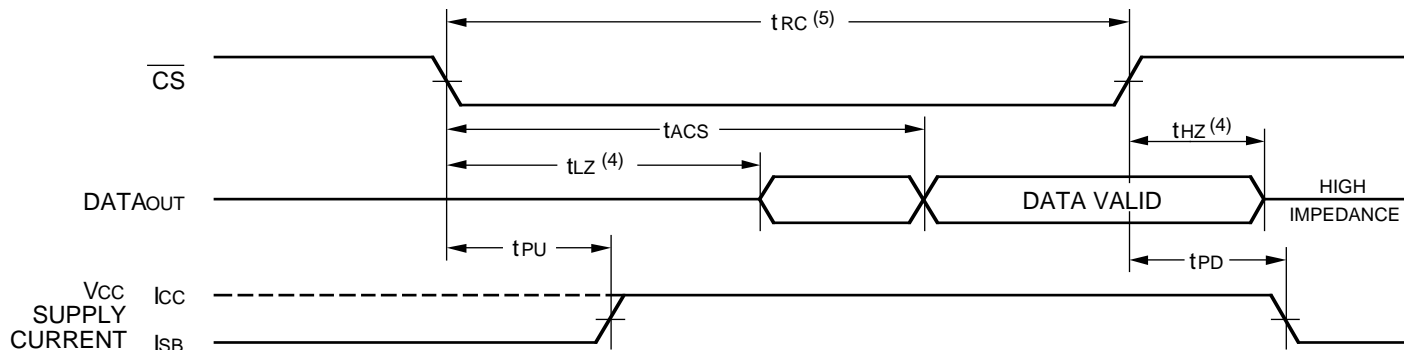
2986 tbl 11

### TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



2986 drw 07

### TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)



2986 drw 08

**NOTES:**

1.  $\overline{WE}$  is HIGH for Read cycle.
2.  $\overline{CS}$  is LOW for Read cycle.
3. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.
4. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with specified loading in Figure 2.
5. All Read cycle timings are referenced from the last valid address to the first transitioning address.

### AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0\text{V} \pm 10\%$ , All Temperature Ranges)

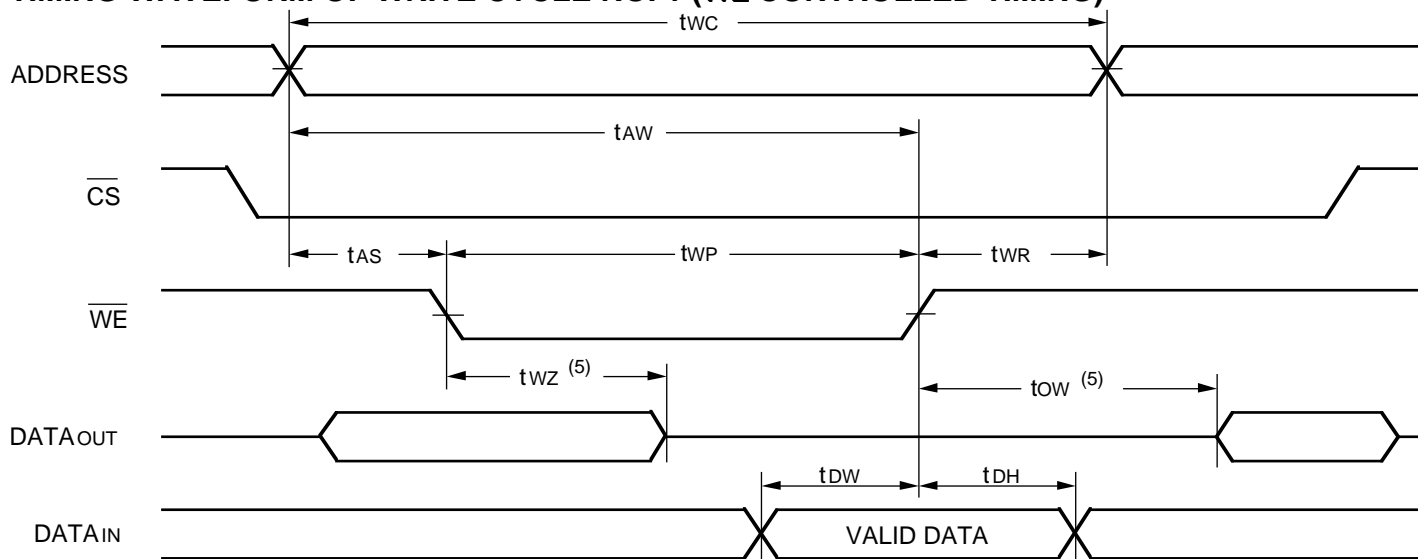
Symbol	Parameter	7187S25		7187S35/45 <sup>(1)</sup>		7187S55 <sup>(1)</sup>		7187S70 <sup>(1)</sup>		7187S85 <sup>(1)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Cycle</b>												
tWC	Write Cycle Time	25	—	35/45	—	55	—	70	—	85	—	ns
tCW	Chip Select to End-of-Write	20	—	25/40	—	50	—	55	—	65	—	ns
tAW	Address Valid to End-of-Write	20	—	25/40	—	50	—	55	—	65	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	20/25	—	35	—	40	—	45	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15/25	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	5	—	5	—	5	—	5	—	5	—	ns
tWZ <sup>(2)</sup>	Write Enable to Output in High-Z	—	12	—	15/30	—	30	—	30	—	40	ns
tOW <sup>(2)</sup>	Output Active from End-of-Write	0	—	0	—	0	—	0	—	0	—	ns

**NOTES:**

1.  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range only.
2. This parameter guaranteed but not tested.

2986 tbl 12

### TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$ CONTROLLED TIMING)<sup>(1,2,3,4)</sup>

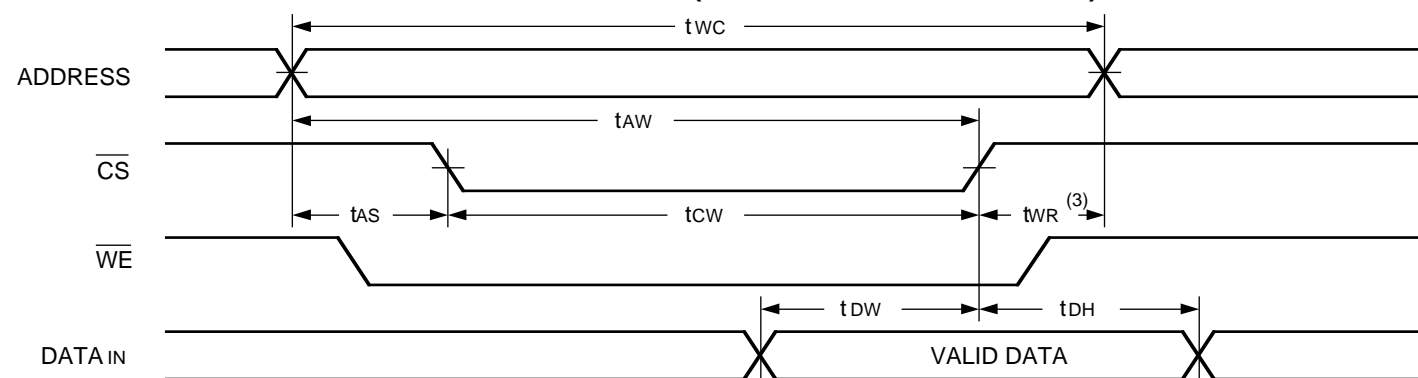


2986 drw 09

**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of the write cycle.
4. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in the high-impedance state.
5. Transition is measured  $\pm 200\text{mV}$  from steady state with a 5pF load (including scope and jig).

### TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$ CONTROLLED TIMING)<sup>(1,2,4)</sup>

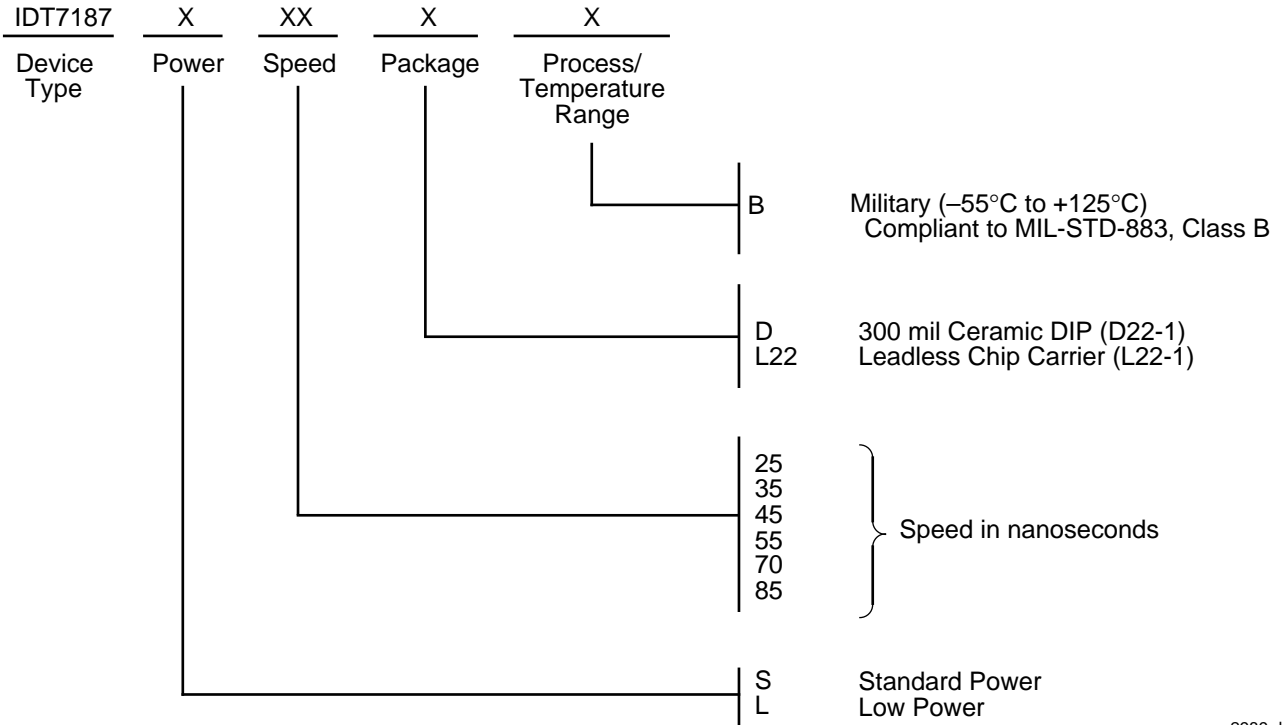


2986 drw 10

**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of the write cycle.
4. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in the high-impedance state.
5. Transition is measured  $\pm 200\text{mV}$  from steady state with a 5pF load (including scope and jig).

**ORDERING INFORMATION**



2989 drw 11