Ordering number : ENN6675

CMOS IC

LC72147V

PLL Frequency Synthesizer for Electronic Tuning in Car Audio Systems

Overview

The LC72147V is a PLL frequency synthesizer for car audio systems. It can implement high-performance multifunction tuners and features a crystal oscillator circuit that supports AM up-conversion, a fast locking circuit, an A/D converter, and an LA1783/1750 IF counter buffer control pin.

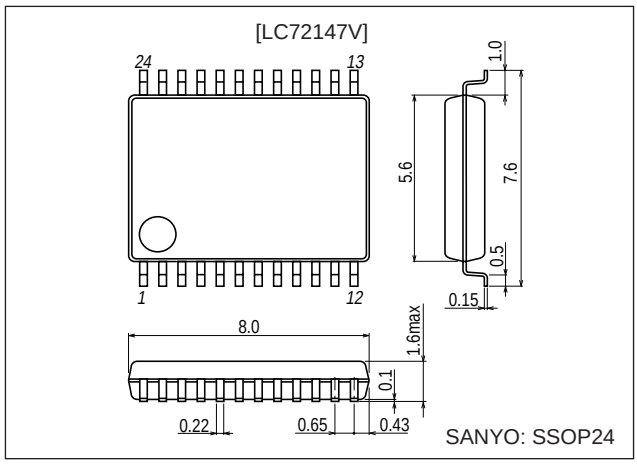
Functions

- High-speed programmable divider
  - — FMIN: 10 to 180 MHz: Pulse swallower type
- IF counter
  - — HCTR: 0.4 to 25 MHz: Frequency measurement
- Crystal oscillator: One of the following 4 frequencies may be selected: 10.35, 10.25, 7.2, and 4.5 MHz
  Reference frequency
  - — One of 12 frequencies may be selected (when a 7.2 or 4.5 MHz crystal is used)
    100*1, 50, 30*2, 25, 12.5, 6.25, 3.125, 10, 9*2, 5, 3*2, 1 kHz
    Notes: 1. Cannot be used when a 10.35 or 10.25 MHz crystal is used
    2. Cannot be used when a 10.25 MHz crystal is used
- Phase comparator
  - — Supports dead band control
  - — Built-in unlock detection circuit
  - — Sub-charge pump for fast locking
  - — Built-in deadlock clearing circuit
- Built-in MOS transistor for forming an active low-pass filter
- I/O ports — General-purpose I/O: 5 pins
  - — Output: n-channel: 3 pins, CMOS: 2 pins
  - — IFBC pin (LA1783/1750 IF counter buffer control pin)
- Serial data I/O
  - — Supports communication with the controller in the CCB format.
- Operating ranges
  - — Supply voltage (V_{DD}): 4.5 to 6.5 V
  - — Built-in regulator voltage (Vreg): 3.0 V (±10%)
  - — Operating temperature: –40 to +85°C
- Package
  - — SSOP-24

Package Dimensions

unit: mm

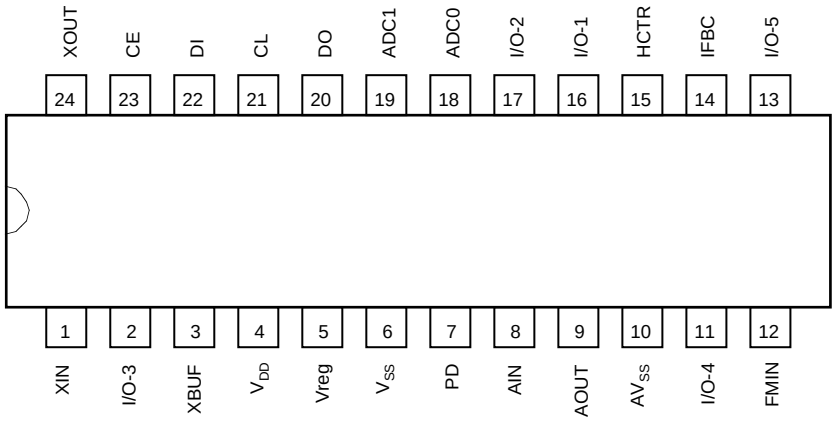
3175A-SSOP24



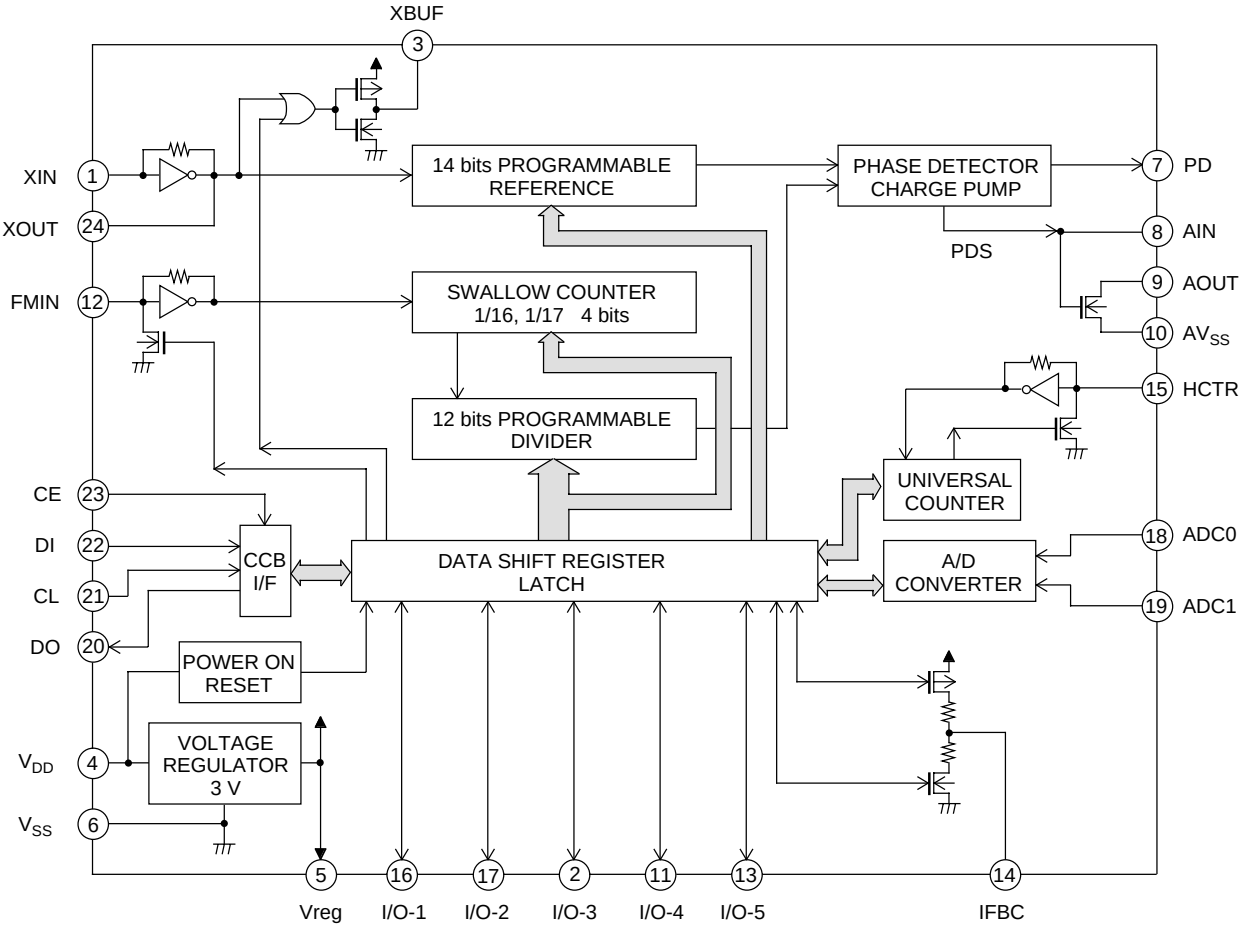
- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignment



Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Pin	Conditions	Ratings	Unit
Supply voltage	V_{DD} max	V_{DD}		–0.3 to +7.0	V
Maximum input voltage	V_{IN}1 max	CE, CL, DI, AIN		–0.3 to +7.0	V
	V_{IN}2 max	XIN, FMIN, HCTR, I/O-4, I/O-5, ADC0, ADC1		–0.3 to Vreg + 0.3	
	V_{IN}3 max	I/O-1 to I/O-3		–0.3 to +15	
Maximum output voltage	V_O1 max	DO		–0.3 to +7.0	V
	V_O2 max	XOUT, IFBC, I/O-4, I/O-5, PD, XBUF		–0.3 to Vreg + 0.3	
	V_O3 max	I/O-1 to I/O-3, AOUT		–0.3 to +15	
Maximum output current	I_O1 max	IFBC		0 to 1.0	mA
	I_O2 max	I/O-4, I/O-5, XBUF		0 to 3.0	
	I_O3 max	DO		0 to 6.0	
	I_O4 max	I/O-1 to I/O-3		0 to 10	
	I_O5 max	AOUT		0 to 35	
Allowable power dissipation	Pd max		Ta ≤ 85°C	150	mW
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–55 to +125	°C

Note: Power supply V_{DD} - V_{SS}, Vreg - V_{SS}: Capacitors of at least 2000 pF must be inserted between these pins when this device is used.

Allowable Operating Ranges at Ta = –40 to 85°C, V_{SS} = 0 V

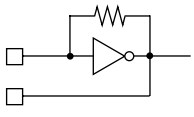
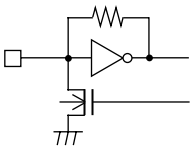
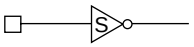
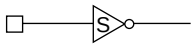
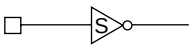
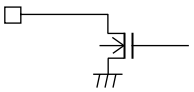
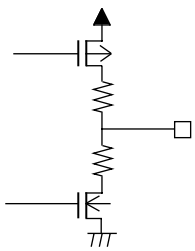
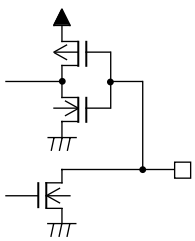
Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	V_{DD}1	V_{DD}		4.5		6.5	V
	V_{DD}2	V_{DD}	Serial data retention voltage	2.5			
Regulator output voltage	Vreg	Vreg	4.5 ≤ V_{DD} ≤ 6.5 V	2.7	3.0	3.3	V
High-level input voltage	V_{IH}1	CE, CL, DI, I/O-1 to I/O-3		2.2		6.5	V
	V_{IH}2	I/O-4, I/O-5		2.2		Vreg	
Low-level input voltage	V_{IL}	CE, CL, DI, I/O-1 to I/O-5		0		0.8	V
Output voltage	V_O1	DO		0		6.5	V
	V_O2	I/O-1 to I/O-3		0		13	
Input frequency	f_{IN}1	XIN	Sine wave, capacitance coupled	1.0		8.0	MHz
	f_{IN}2	FMIN	Sine wave, capacitance coupled	10		180	
	f_{IN}3	HCTR	Sine wave, capacitance coupled	0.4		25	
Guaranteed crystal oscillator frequency ranges	X'tal1	XIN, XOUT	*1	4.0		7.0	MHz
	X'tal2	XIN, XOUT	*1	7.1		10.5	
Input amplitude	V_{IN}1	XIN		200		900	mVrms
	V_{IN}2-1	FMIN	10 ≤ f < 130 MHz *2	40		900	
	V_{IN}2-2	FMIN	130 ≤ f ≤ 180 MHz *2	70		900	
	V_{IN}3-1	HCTR	0.4 ≤ f ≤ 25 MHz *3	70		900	
	V_{IN}3-2	HCTR	8 ≤ f ≤ 12 MHz *4	100		900	
Input voltage range	V_{IN}4	ADC0, ADC1		0		Vreg	V
Data setup time	t_{SU}	DI, CL	*5	0.45			µs
Data hold time	t_{HD}	DI, CL	*5	0.45			µs
Clock low-level period	t_{CL}	CL	*5	0.45			µs
Clock high-level period	t_{CH}	CL	*5	0.45			µs
CE wait time	t_{EL}	CE, CL	*5	0.45			µs
CE setup time	t_{ES}	CE, CL	*5	0.45			µs
CE hold time	t_{EH}	CE, CL	*5	0.45			µs
Data latch change time	t_{LC}		*5			0.45	µs
Data output time	t_{DC}	DO, CL	Depends on the value of the pull-up resistor used.			0.2	µs
	t_{DH}	DO, CE					

Notes: 1. Recommended crystal oscillator CI values
CI ≤ 120 Ω (Crystal: 4.5 MHz), CI ≤ 70 Ω (Crystal: 7.2, 10.25, or 10.35 MHz)
Note that the crystal oscillator circuit characteristics depend on the printed circuit board and the particular components used. We recommend consulting the manufacturer of the crystal when designing this circuit.
2. Refer to the description of the structure of the programmable divider.
3. Serial data: CTC = 0
4. Serial data: CTC = 1
5. See the timing chart for serial data transfers.

Electrical Characteristics in the Allowable Operating Ranges

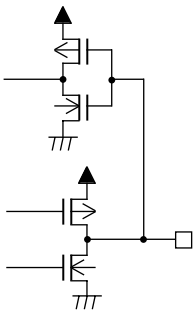
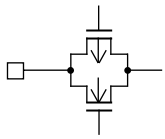
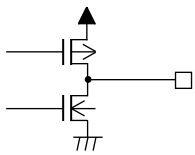
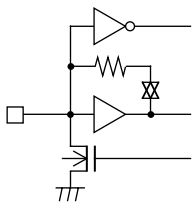
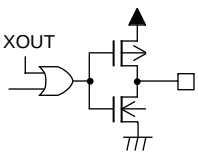
Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Internal feedback resistance	Rf1	XIN			1.0		MΩ
	Rf2	FMIN			500		kΩ
	Rf3	HCTR			250		
Hysteresis	V_{HIS}	CE, CL, DI			0.1 Vreg		V
High-level output voltage	$V_{OH}1$	I/O-4, I/O-5	I_O = – 0.5 mA	Vreg – 0.5			V
			I_O = – 1 mA	Vreg – 1.0			
	$V_{OH}2$	PD, AIN	I_O = – 1 mA	Vreg – 0.5			
			I_O = – 2 mA	Vreg – 1.0			
	$V_{OH}3$	XBUF	I_O = – 0.5 mA	Vreg – 0.5			V
	$V_{OH}4$	IFBC	I_O = – 0.1 mA	Vreg – 0.5			V
Low-level output voltage	$V_{OL}1$	I/O-4, I/O-5	I_O = 0.5 mA			0.5	V
			I_O = 1 mA			1.0	
	$V_{OL}2$	PD, AIN	I_O = 1 mA			0.5	V
			I_O = 2 mA			1.0	
	$V_{OL}3$	XBUF	I_O = 0.5 mA			0.5	V
	$V_{OL}4$	IFBC	I_O = 0.1 mA			0.5	V
	$V_{OL}5$	I/O-1 to I/O-3	I_O = 1 mA			0.2	V
			I_O = 2.5 mA			0.5	
			I_O = 5 mA			1.0	
			I_O = 9 mA			1.8	
	$V_{OL}6$	DO	I_O = 5 mA			1.0	V
	$V_{OL}7$	AOUT	I_O = 30 mA, AIN = 2.0 V			1.5	V
Mid-level output voltage	V_{OM}	IFBC	I_O = 20 µA	1.2	1.5	1.8	V
High-level input current	$I_{IH}1$	CE, CL, DI	V_I = 6.5 V			5.0	µA
	$I_{IH}2$	I/O-1 to I/O-3	V_I = 13 V			5.0	
	$I_{IH}3$	I/O-4, I/O-5, ADC0, ADC1, HCTR	V_I = Vreg			5.0	
	$I_{IH}4$	XIN	V_I = Vreg	1.3		7	
	$I_{IH}5$	FMIN	V_I = Vreg	2.5		14	
	$I_{IH}6$	HCTR	V_I = Vreg	5.0		28	
	$I_{IH}7$	AIN	V_I = Vreg			200	nA
Low-level input current	$I_{IL}1$	CE, CL, DI	V_I = 0 V			5.0	µA
	$I_{IL}2$	I/O-1 to I/O-3	V_I = 0 V			5.0	
	$I_{IL}3$	I/O-4, I/O-5, ADC0, ADC1, HCTR	V_I = 0 V			5.0	
	$I_{IL}4$	XIN	V_I = 0 V	1.3		7	
	$I_{IL}5$	FMIN	V_I = 0 V	2.5		14	
	$I_{IL}6$	HCTR	V_I = 0 V	5.0		28	
	$I_{IL}7$	AIN	V_I = 0 V			200	nA
Output off leakage current	$I_{OFF}1$	I/O-1 to I/O-3	V_O = 13 V			5.0	µA
	$I_{OFF}2$	DO	V_O = 6.5 V			5.0	
High-level 3-state off leakage current	I_{OFFH}	PD	V_O = Vreg		0.01	200	nA
Low-level 3-state off leakage current	I_{OFFL}	PD	V_O = 0 V		0.01	200	nA
Input capacitance	C_{IN}	FMIN			6		PF
A/D converter linearity error	Err	ADC0, ADC1		–1/2		1/2	LSB
Pull-down transistor on resistance	Rpd	FMIN		80	200	600	kΩ
Supply current	I_{DD}	V_{DD}	X'tal = 10.35 MHz $f_{IN}2$ = 180 MHz $V_{IN}2$ – 2 = 70 mVrms $f_{IN}3$ = 25 MHz $V_{IN}3$ – 1 = 70 mVrms		12		mA

Pin Functions

Pin No.	Symbol	Usage	Function	Pin circuit
1 24	XIN XOUT	X'tal OSC	• Crystal oscillator connection. (4.5, 7.2, 10.25, or 10.35 MHz)	
12	FMIN	Local oscillator signal input	• FMIN is selected by setting DVS in the control data to 1. • Input frequency: 10 to 180 MHz • The signal is transmitted to the swallow counter. • The divisor can be set to a value in the range 272 to 65,535.	
23	CE	Chip enable	• This pin must be set to the high level when inputting serial data to the LC72147V DI pin and when outputting serial data from the DO pin.	
21	CL	Clock	• Data synchronization clock signal used when inputting serial data to the LC72147V DI pin and when outputting serial data from the DO pin.	
22	DI	Input data	• Serial data input for transferring data from the controller to the LC72147V.	
20	DO	Output data	• Serial data output for transferring data from the LC72147V to the controller.	
4	V_{DD}	Power	• LC72147V power supply. A voltage in the range 4.5 to 6.5 V must be provided when the PLL circuit is operating. • The power-on reset circuit operates when power is first applied.	———
5	Vreg	Regulator output	• Regulator output. A capacitor must be inserted between Vreg and V_{SS}. • The output voltage (3.0 V ±10%) is supplied to internal circuits.	———
6	V_{SS}	Ground	• LC72147V ground.	———
14	IFBC	IF buffer control	• The LC72147V can control the LA1783/1750 IF buffer output. • This is a 3-state output. (0 V, Vreg/2 = 1.5 V, and Vreg = 3 V)	
16 17 2	I/O-1 I/O-2 I/O-3	General-purpose I/O ports	• General-purpose I/O ports. • The outputs are open-drain circuits. • After the power-on reset, I/O-1 and I/O-2 function as input ports. I/O-3 functions as an output port fixed at the low level. • The input/output state of these ports can be set using the I/O-1 to I/O-3 bits in the serial data sent from the controller.	

Continued on next page.

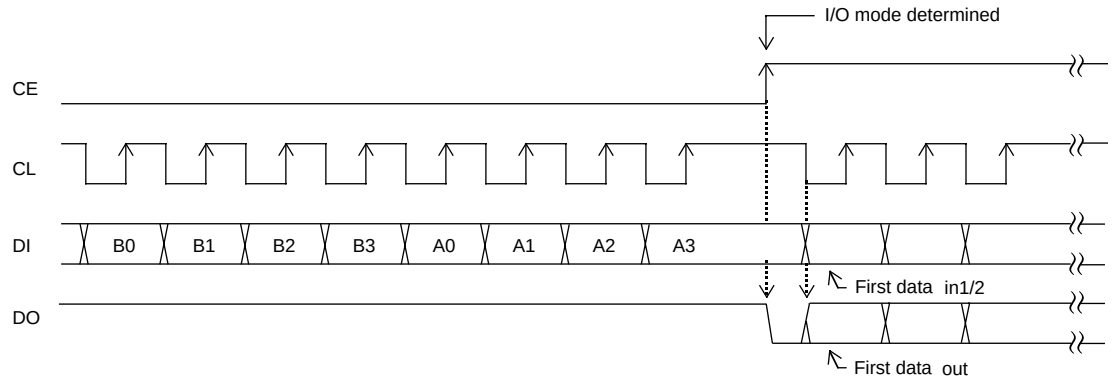
Continued from preceding page.

Pin No.	Symbol	Usage	Function	Pin circuit
11 13	I/O-4 I/O-5	General-purpose I/O ports	• General-purpose I/O ports. • The outputs are complementary output circuits. • After the power-on reset, these ports function as input ports. • The input/output state of these ports can be set using the I/O-4 and I/O-5 bits in the serial data sent from the controller.	
18 19	ADC0 ADC1	A/D converter input	• A/D converter input The A/D converter is a 6-bit successive-approximation circuit. See the item on the structure of the A/D converter for details.	
7	PD	Charge pump output	• PLL charge pump output When the frequency created by dividing the local oscillator signal frequency by N is higher than the reference frequency, a high level is output from the PD pin. When lower, a low level is output. The PD pin goes to the high-impedance state when the frequencies match.	
15	HCTR	General-purpose counter	• HCTR is selected by setting CTS in the control data to 1. Input frequency: 0.4 to 25 MHz The signal is input to a divide-by-2 circuit and the result is input to a general-purpose counter. This counter can also be used as an integrating counter. The counter value is output as the result of the count, MSB first, from the DO pin. See the item describing the structure of the general-purpose counter for details.	
3	XBUF	Crystal oscillator buffer	• Output buffer for the crystal oscillator circuit • When XB in the serial data is set to 1, the output buffer operates and the crystal oscillator signal (a pulse signal) is output. When XB is 0, XBUF outputs a low level. (After the power-on reset, XB is set to 0 and the output buffer is fixed at the low level.)	

Serial Data I/O Methods

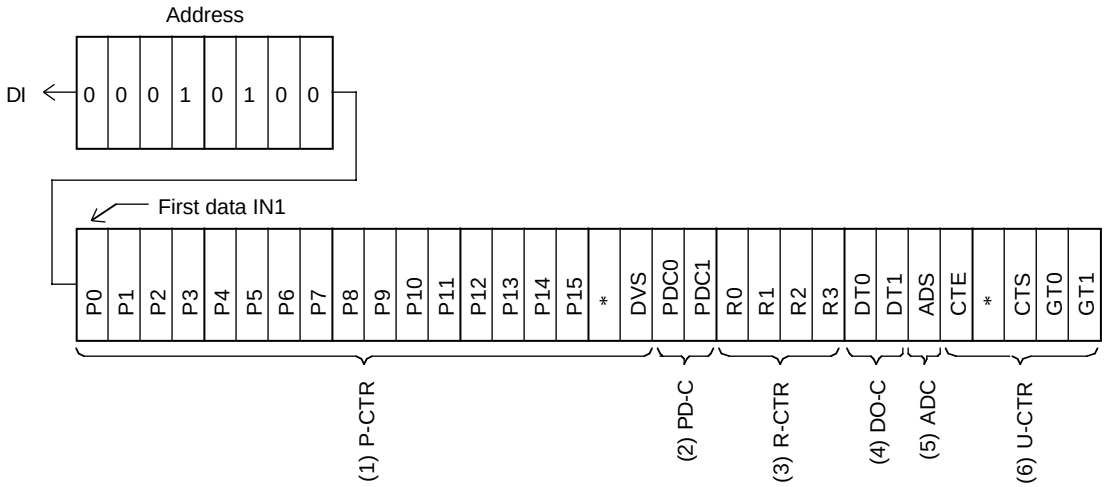
Data is input to and output from the LC72147V using the Sanyo CCB (Computer Control Bus) format, which is the serial bus format used by Sanyo audio ICs. This IC adopts a CCB format with an 8-bit address.

	I/O mode	Address								Content
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1 (82)	0	0	0	1	0	0	1	0	• Control data input (serial input) mode. • 32 bits of data are input. • See the “DI Control Data (Serial Data Input) Structure” item for details on the content of the input data.
[2]	IN2 (92)	1	0	0	1	0	0	1	0	• Control data input (serial input) mode. • 32 bits of data are input. • See the “DI Control Data (Serial Data Input) Structure” item for details on the content of the input data.
[3]	OUT (A2)	0	1	0	1	0	0	1	0	• Data output (serial data output) mode. • The number of bits output is equal to the number of clock cycles. • See the “DO Output Data (Serial Data Output) Structure” item for details on the content of the output data.

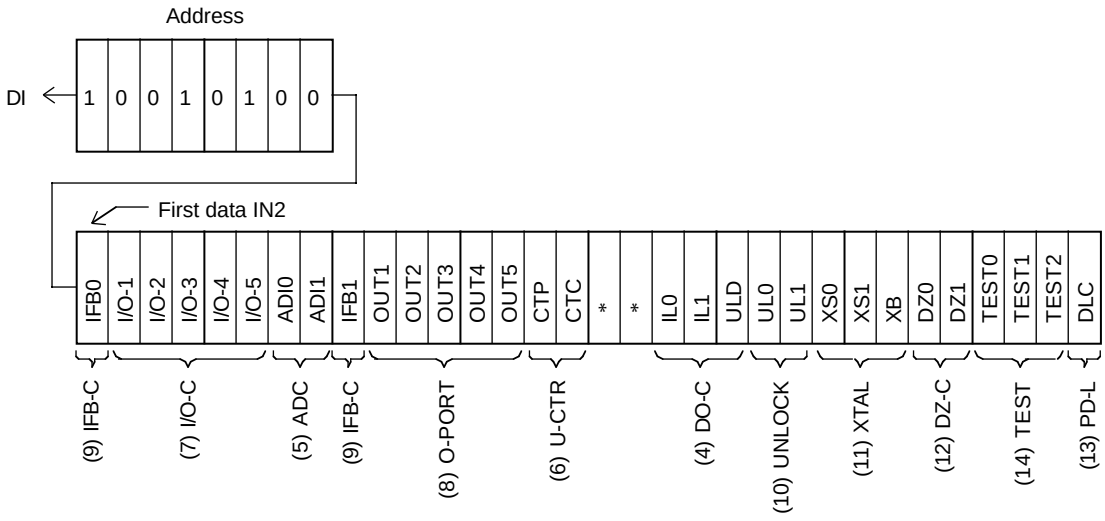


DI control data (serial data input) structure

(1) IN1



(2) IN2



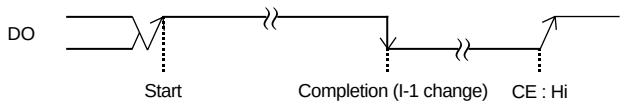
*: Don't care

DI control data description

<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15
DVS</td><td>• This data sets the divisor for the programmable divider
P0 is the LSB, and P15 is the MSB of this binary value.
DVS = 0: The FMIN pin is pulled down.
1: Selects the FMIN pin.
Divisor setting (N): 272 to 65,536
Input frequency range: 10 to 180 MHz
*: See the “Programmable Divider Structure” item for details.</td><td></td></tr>
<tr><td>(2)</td><td>Sub-charge pump control data
PDC0, PDC1</td><td>• This data controls the sub-charge pump.
<table>
<tr><th>PDC1</th><th>PDC0</th><th>Sub-charge pump state</th></tr>
<tr><td>0</td><td>*</td><td>High impedance</td></tr>
<tr><td>1</td><td>0</td><td>Charge pump operating (PLL unlocked)</td></tr>
<tr><td>1</td><td>1</td><td>Charge pump operating (normal operation)</td></tr>
</table>
(* : don’t care)
*: The sub-charge pump output is connected internally to the gate of the transistor used for low-pass filter formation. The sub-charge pump can be used in conjunction with the PD pin (main charge pump pin) to form a high-speed locking circuit.
See the “Charge Pump Structure” item for details.</td><td>UL0, UL1, DLC</td></tr>
<tr><td>(3)</td><td>Reference divider data
R0 to R3</td><td>• Reference frequency selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency (kHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100 *1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9 *2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3 *2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>30 *2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>*3 PLL inhibit + X’tal OSC stop</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>*3 PLL inhibit</td></tr>
</table>
Notes: 1. Illegal value when a crystal oscillator frequency of 10.25 or 10.35 MHz is selected.
2. Illegal value when a crystal oscillator frequency of 10.25 MHz is selected.
3. PLL inhibit (backup mode)
The programmable divider block is stopped, the FMIN pin is pulled down to ground, and the charge pump output is set to the floating state.</td><td></td></tr>
</table>

Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(4)</td><td>DO, I/O-5 pin control data
ULD
DT0, DT1
IL0, IL1</td><td>
• Data that determines the output of the DO and I/O-5 pins
<table>
<tr><th>ULD</th><th>DT1</th><th>DT0</th><th>DO pin</th><th>I/O-5 pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Low when unlocked</td><td rowspan="4">OUT5 *2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>end-AD</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IN *1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td><td rowspan="4">Low when unlocked *2</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>end-AD</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>end-UC</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>IN *1</td></tr>
</table>
end-AD: A/D converter operation completion
end-UC: General-purpose counter operation completion


Note: 1.
<table>
<tr><th>IL1</th><th>IL0</th><th>IN</th></tr>
<tr><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>I-1 (pin state)</td></tr>
<tr><td>1</td><td>0</td><td>I-2 (pin state)</td></tr>
<tr><td>1</td><td>1</td><td>DO goes low when I-1 changes. *</td></tr>
</table>
However, if I/O-1 and I/O-2 are set to output mode, they go to the open state.
Note: 2. Invalid if the I/O-5 pin is set to input mode.
Caution: Cannot be used in crystal oscillator stop mode (The DO pin will not change state.)
[When the reference divider data is R3 = R2 = R1 = 1, and R0 = 0.]
</td><td>OUT5
I/O-1
I/O-2
I/O-5</td></tr>
<tr><td>(5)</td><td>A/D converter control data
ADS
ADI0
ADI1</td><td>
• A/D converter conversion start data
ADS = 1: Resets and starts the A/D converter
ADS = 0: Resets the A/D converter
<table>
<tr><th>ADI1</th><th>ADI0</th><th>A/D converter input pin</th></tr>
<tr><td>1</td><td>1</td><td>Stopped</td></tr>
<tr><td>1</td><td>0</td><td>ADC0</td></tr>
<tr><td>0</td><td>1</td><td>ADC1</td></tr>
<tr><td>0</td><td>0</td><td>ADC0, ADC1</td></tr>
</table>
If both the ADC0 and ADC1 pins are specified as A/D converter inputs, the levels are converted sequentially in the order ADC0 first and the ADC1. See the “A/D Converter Structure” item for details.
</td><td></td></tr>
</table>

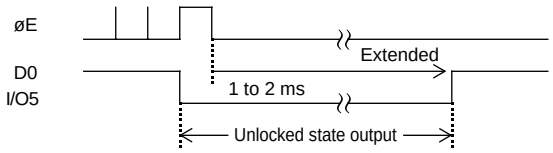
Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(6)</td><td>General-purpose counter
control data
CTS, CTE
GT0, GT1
CTP
CTC</td><td>
• Selects the general-purpose counter input pin (HCTR).
CTS = 1: Selects the HSTR pin.
CTS = 0: Pulls down the HCTR pin.
• General-purpose counter measurement start data
CTE = 1: Starts the counter.
CTE = 0: Resets the counter.
• Determines the measurement time (frequency mode) and number of periods (period mode).
<table>
<tr><th rowspan="2">GT1</th><th rowspan="2">GT0</th><th colspan="3">Frequency measurement</th><th rowspan="2">Period measurement mode</th></tr>
<tr><th rowspan="2">Measurement time</th><th colspan="2">Wait time</th></tr>
<tr><th>CTP = 0</th><th>CTP = 1</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td><td>1 to 2 ms</td><td>One period</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4 ms</td><td>1 to 2 ms</td><td>One period</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8 ms</td><td>1 to 2 ms</td><td>Two periods</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8 ms</td><td>1 to 2 ms</td><td>Two periods</td></tr>
</table>
• CTP = 0: When the counter has been reset (CTE = 0), pulls down the general-purpose counter input.
CTP = 1: When the counter has been reset (CTE = 0), does not pull down the general-purpose counter input, and shortens the wait time.
However, immediately after CTP is set to 1, the counter start must be delayed until the general-purpose counter input pin has been biased.
• The input sensitivity is reduced when CTC is set to 1. (Sensitivity: 10 to 30 mV rms)
</td><td></td></tr>
<tr><td>(7)</td><td>I/O port control data
IO-1 to I/O-5</td><td>
• Data that specifies the I/O direction of the I/O ports.
[Data] = 0: Input port
1: Output port
*: After the power-on reset, the I/O-1, I/O-2, I/O-4, and I/O-5 are set up as input ports. I/O-3 is set up as an output port.
</td><td>OUT1 to OUT5
ULD</td></tr>
<tr><td>(8)</td><td>Output port data
OUT1 to OUT5</td><td>
• Data that determines the output from output ports O-1 to O-5.
[Data] = 1: Open or high level.
0: Low
*: Invalid when the corresponding port is set up as an input port or as the unlock state indicator output.
</td><td>I/O-1 to I/O-5
ULD</td></tr>
<tr><td>(9)</td><td>IFBC port control data
IFB0, IFB1</td><td>
• Determines the 3-value output of the IFBC port.
<table>
<tr><th>IFB0</th><th>IFB1</th><th>IFBC output</th></tr>
<tr><td>0</td><td>0</td><td>Mid (Vreg/2 = 1.5 V)</td></tr>
<tr><td>0</td><td>1</td><td>Low (0 V)</td></tr>
<tr><td>1</td><td>0</td><td>Mid (Vreg/2 = 1.5 V)</td></tr>
<tr><td>1</td><td>1</td><td>High (Vreg = 3.0 V)</td></tr>
</table>
*: When PLL inhibit and crystal oscillator stop mode (R0 = 0, R1 = R2 = R3 = 1), the IFBC output is set to the open state. This output goes to the mid level after the power-on reset.
</td><td></td></tr>
</table>

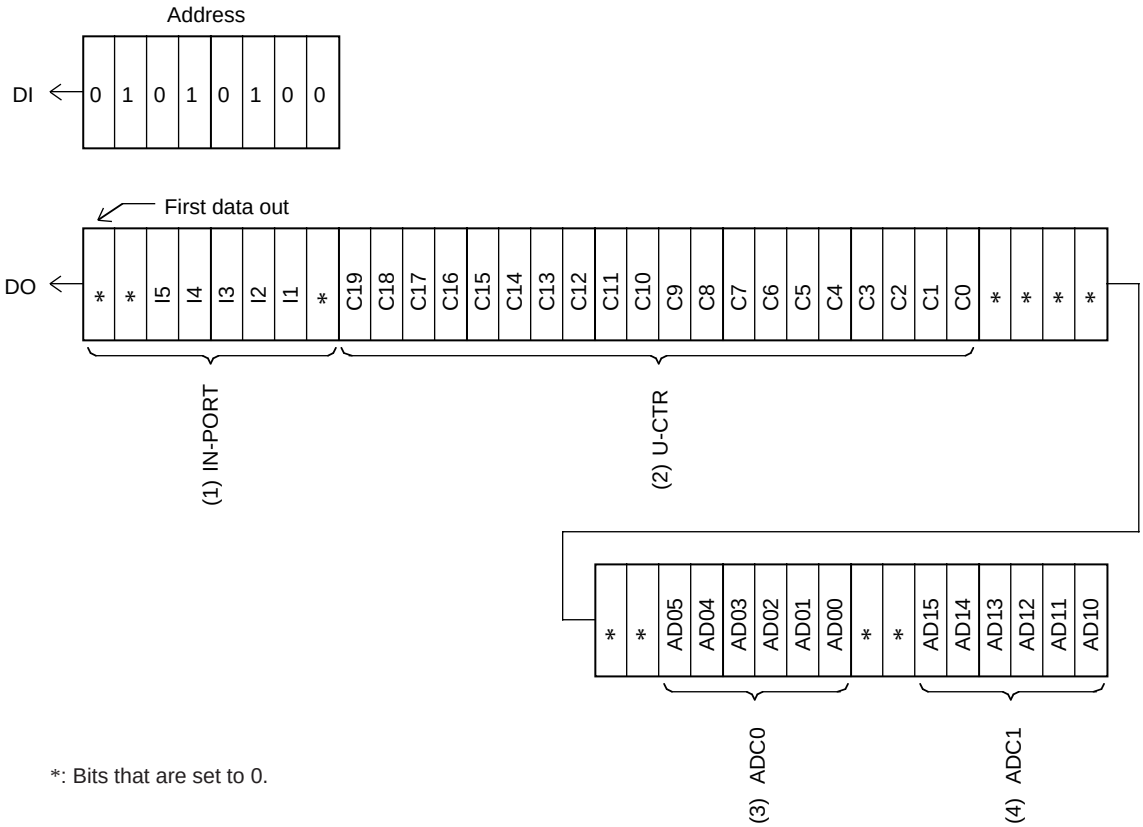
Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(10)</td><td>Unlock state detection data
UL0, UL1</td><td>• Width selection for the phase error (øE) detection function used to determine the PLL locked/unlocked state. When a phase error greater than the øE detection width from the table occurs, the PLL circuit is seen as in the unlocked state. When unlocked, the detection pin (DO or I/O-5) goes to the low state.
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detection pin output</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>øE is output directly</td></tr>
<tr><td>1</td><td>0</td><td>±0.5 µs</td><td>øE is extended by 1 to 2 ms.</td></tr>
<tr><td>1</td><td>1</td><td>±1 µs</td><td>øE is extended by 1 to 2 ms.</td></tr>
</table>

</td><td>ULD
DT0, DT1</td></tr>
<tr><td>(11)</td><td>Crystal oscillator circuit
XS0, XS1
XB</td><td>• Crystal oscillator selection data
<table>
<tr><th>XS1</th><th>XS0</th><th>X'tal OSC</th></tr>
<tr><td>0</td><td>0</td><td>4.5 MHz</td></tr>
<tr><td>0</td><td>1</td><td>7.2 MHz</td></tr>
<tr><td>1</td><td>0</td><td>10.25 MHz</td></tr>
<tr><td>1</td><td>1</td><td>10.35 MHz</td></tr>
</table>
*: After the power-on reset, 10.25 MHz is selected.
• Crystal oscillator buffer (XBUF) output control data
XB = 0: Buffer output is turned off. (This mode is selected after the power-on reset.)
XB = 1: Buffer output is turned on.</td><td>R0 to R3</td></tr>
<tr><td>(12)</td><td>Phase comparator control data
DZ0, DZ1</td><td>• Controls the phase comparator dead band.
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead band mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
*: The phase comparator operates in DZA mode after the power-on reset.</td><td></td></tr>
<tr><td>(13)</td><td>Charge pump control data
DLC</td><td>• Bit that forcible sets the charge pump output to the low level.
DLC = 1: Low level
DLC = 0: Normal operation
*: If a deadlock occurs due to the VCO control voltage (Vtune) going to zero and stopping the VCO oscillator, set the charge pump output to the low level and set Vtune to V_{CC} to escape from the deadlocked state. Normal operation is selected after the power-on reset.</td><td></td></tr>
<tr><td>(14)</td><td>IC test data
TEST0
TEST1
TEST2</td><td>• IC test control data
These bits must be set as follows during normal operation.
TEST0 = 0
TEST1 = 0
TEST2 = 0
*: After the power-on reset, the test data is all set to zero.</td><td></td></tr>
</table>

Structure of the DO Output Data (serial output data)

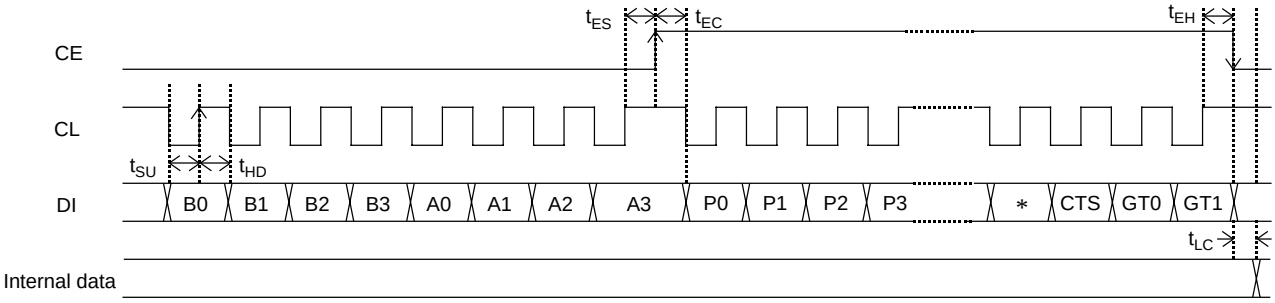
(3) OUT



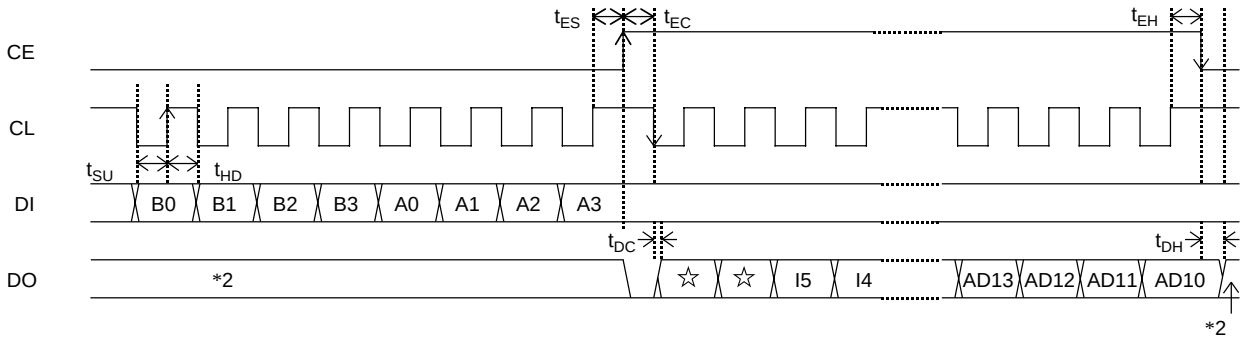
*: Bits that are set to 0.

No.	Control block/data	Content	Related data
(1)	I/O port data I5 to I1	• The bits I1 to I5 are set to the latched states of the I/O pins I/O-1 to I/O-5. These states are latched at the point the IC enters data output mode. The pin states are latched regardless of the pin mode (input or output). Pin state = high: 1 low: 0	I/O-1 to I/O-5
(2)	General-purpose counter binary data C19 to C0	• The bits C19 to C0 are set to the latched content of the 20-bit binary general-purpose counter. C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTS0 CTS1 CTE
(3)	A/D converter ADC0 data AD05 to AD00	• The bits AD05 to AD00 are set to the latched result of the A/D conversion of the ADC0 pin input signal. AD05 ← MSB AD00 ← LSB	ADI0 ADI1 ADS
(4)	A/D converter ADC1 data AD15 to AD10	• The bits AD15 to AD10 are set to the latched result of the A/D conversion of the ADC1 pin input signal. AD15 ← MSB AD10 ← LSB	ADI0 ADI1 ADS

Serial data input (IN1/IN2) t_{SU}, t_{HD}, t_{ES}, t_{EC}, t_{EH}, > 0.45 µs t_{LC} < 0.45 µs

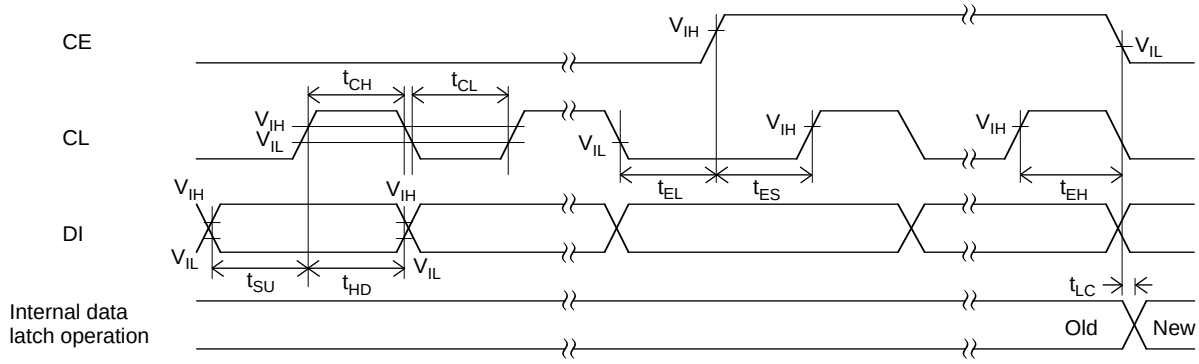


Serial data output (OUT) t_{SU}, t_{HD}, t_{ES}, t_{EC} > 0.45 µs t_{DC}, t_{DH} < 0.2 µs *1

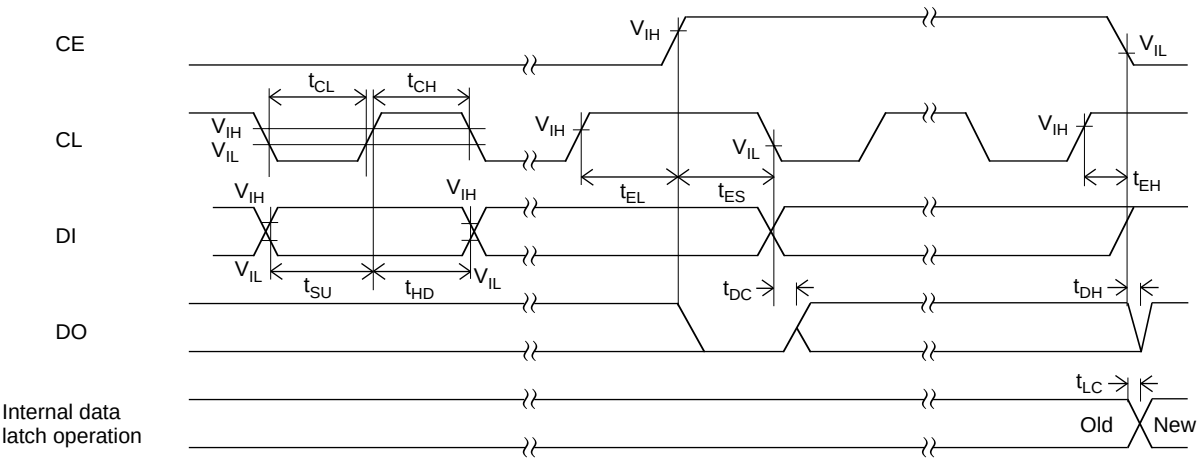


Notes: 1. The DO pin is an n-channel open drain output, and thus the data switching time will differ depending on the value of the pull-up resistor used and the printed circuit board capacitance.
2. The DO pin is normally open.

Serial data timing

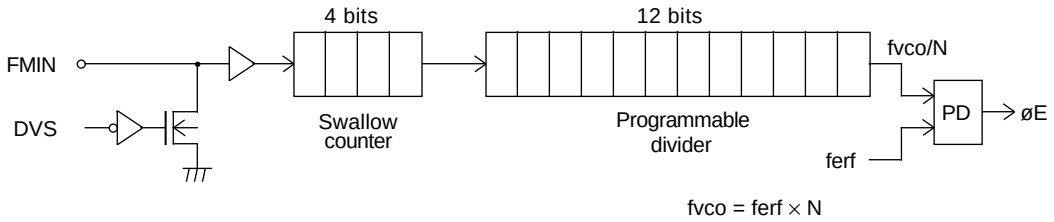


<When CL is stopped at the low level>



<When CL is stopped at the high level>

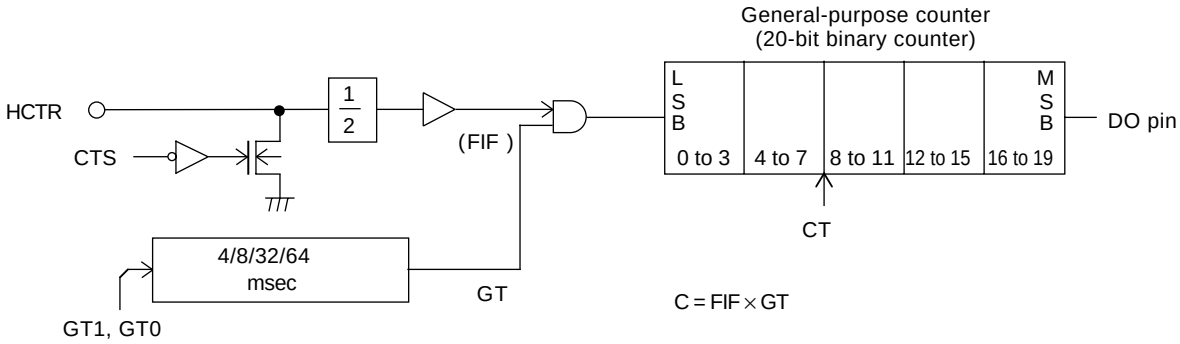
Programmable divider structure



DVS	Set divisor (N)	Input frequency range (f(MHz)) Minimum input sensitivity		FMIN
1	272 to 65535	10 ≤ f < 130 40 mVrms	130 ≤ f ≤ 180 70 mVrms	Selected
0	—	—	—	Pulled down

General-purpose counter structure

The LC72147V's general-purpose counter is a 20-bit binary counter.
The result of the count operation can be read out MSB first from the DO pin.



The measurement time when the general-purpose counter is used for frequency measurement is set to either 4, 8, 32, or 64 ms by the GT0 and GT1 bits. The frequency of the input to the HCTR pin can be measured by determining how many pulses were input to the general-purpose counter during this measurement time.

Check signal frequency

X'tal OSC	4.5 MHz	7.2 MHz	10.25 MHz	10.35 MHz	
				fref = 30, 9, 3 kHz	fref : other than 30, 9, 3 kHz
Check signal	900 kHz	900 kHz	1025 kHz	1030 kHz	1150 kHz

The CTC data switches the input sensitivity. The input sensitivity is reduced when CTC is set to 1.

CTC	HCTR: Minimum input sensitivity rating		
	0.4 ≤ f < 8	8 ≤ f < 12	12 ≤ f < 25
0 (Normal mode)	70 mVrms	70 mVrms (10 to 20 mVrms)	70 mVrms
1 (Reduced sensitivity mode)	—	100 mVrms (30 to 40 mVrms)	—

—: No sensitivity rating (not guaranteed)
( ): Rated value (reference value)

CTP data: Determines the state of the general-purpose counter input pin (HCTR) when the general-purpose counter is reset (CTE = 0).

CTP = 0: The general-purpose counter input pin is pulled down.

1: The general-purpose counter input pin is not pulled down, and the wait time is shortened by 1 to 2 ms.

IF CTP is to be set to 1, set CTP to 1 at least 4 ms before the counter is started by setting CTE to 1.

Leave CTP set to 0 if the counter will not be used.

GT1	GT0	Frequency measurement mode		
		Measurement time	Wait time	
			CTP = 0	CTP = 1
0	0	4 ms	3 to 4 ms	1 to 2 ms
0	1	8 ms		
1	0	32 ms	7 to 8 ms	
1	1	64 ms		

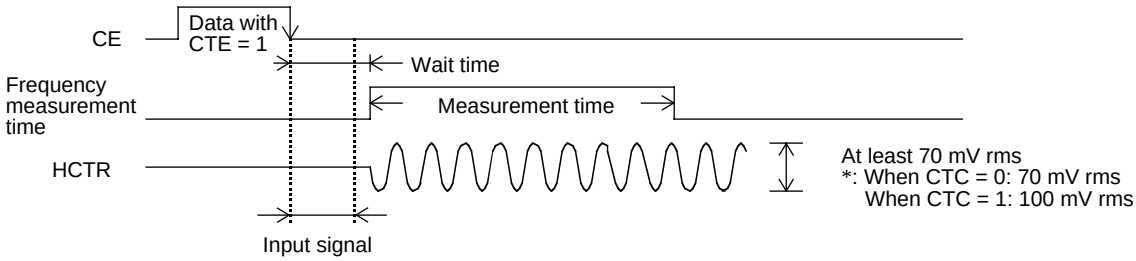
IF counter operation

Reset the general-purpose counter in advance by setting CTE to 0 before starting the counter.

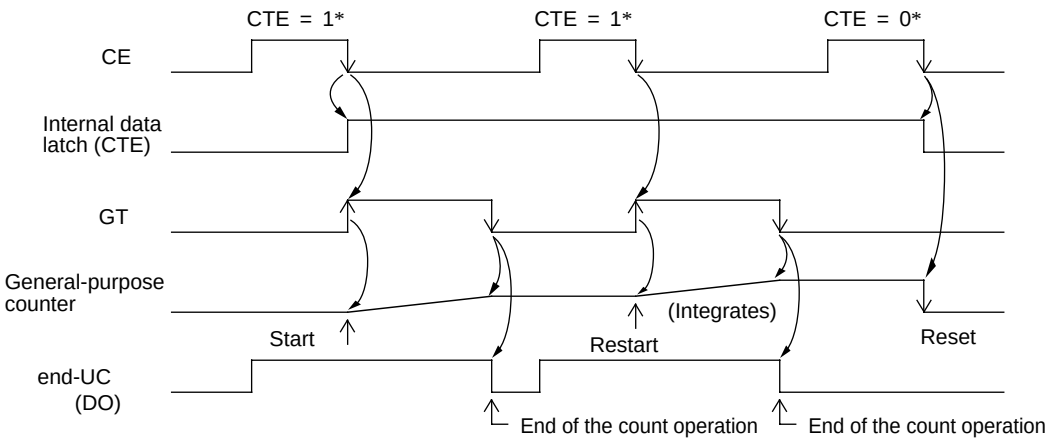
A general-purpose counter count operation is started by setting the CTE bit in the serial data to 1. The serial data takes effect internally to the LC72147V when the CE pin input level is changed from high to low. The input to the HCTR pin must be provided before the wait time has elapsed after CE was set low.

Next, the result of the general-purpose counter count after the measurement completes must be read out while CTE is still set to 1. This is because the general-purpose counter is reset when CTE is set to 0.

Note that the signal input to the HCTR pin is first divided by 2 internally to the IC and then input to the general-purpose counter. Therefore, the result of the general-purpose counter count is a value that corresponds to 1/2 of the frequency actually input to the HCTR pin.



When used as an integrating counter



*CTE: 0 → • Resets the general-purpose counter

1 → • Starts the general-purpose counter

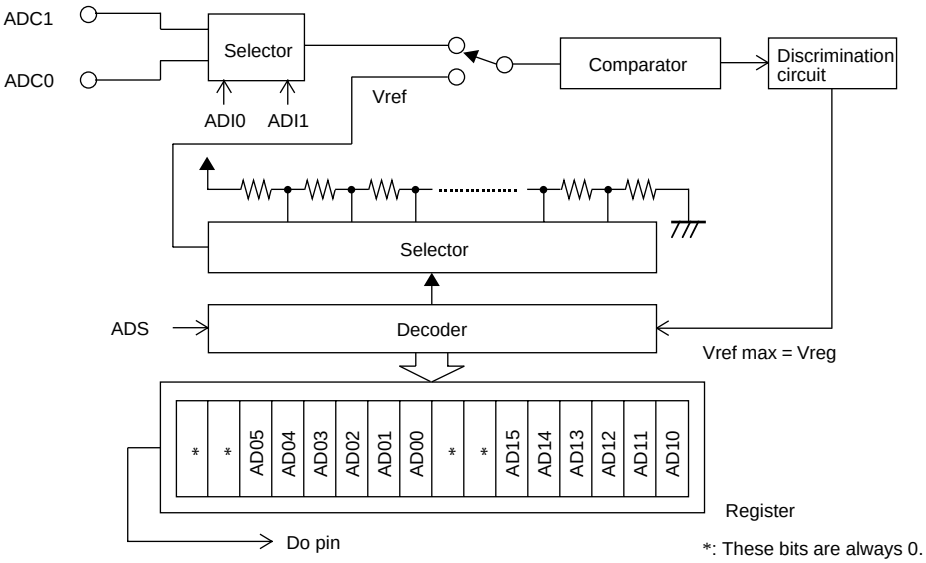
• Restarts the counter if set to 1 again.

In integrating count mode, the count value of the general-purpose counter is accumulated. Care must be taken to handle counter overflow correctly. The count value will be in the range 0_H to $FFFFF_H$.

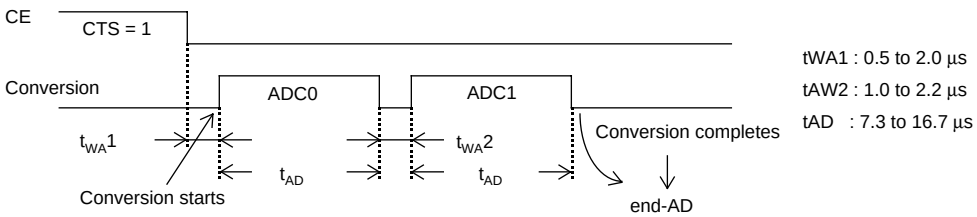
An integrating count operation is performed by sending the serial data (IN1) again with the CTE bit still set to 1. This restarts the general-purpose counter measurement operation and adds the new counts to the previous counter value.

A/D converter structure

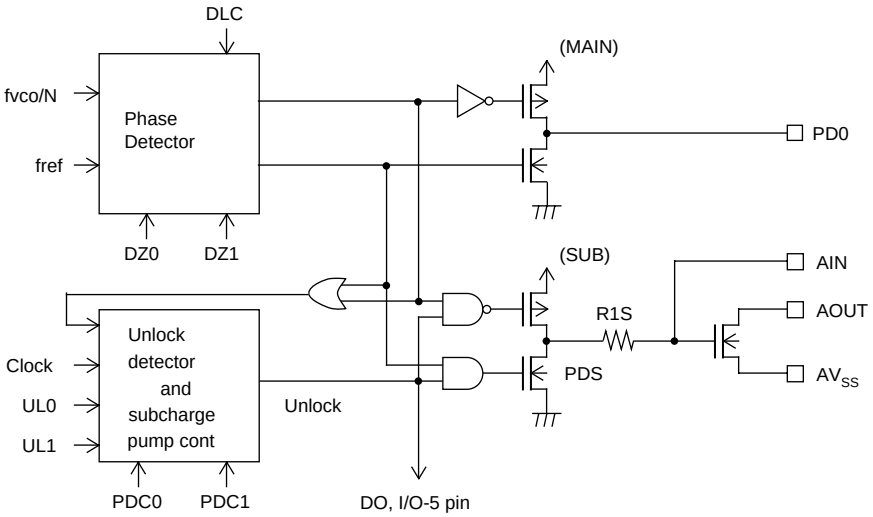
The LC72147V A/D converter is a 6-bit successive-approximation converter. It features a conversion time of about 17 µs. The full-scale voltage level is the Vreg level, which corresponds to a data value of $3F_H$.



ADI1	ADI0	Input pin
1	1	Illegal setting
1	0	ADC0
0	1	ADC1
0	0	ADC0/ADC1



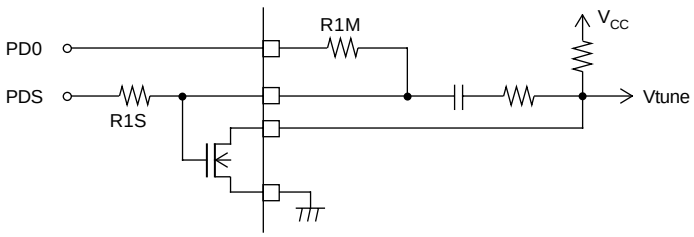
Charge pump structure



PDC1	PDC0	PDS (Sub-charge pump state)
0	*	High impedance
1	0	Charge pump operating (PLL unlocked)
1	1	Charge pump operating (normal operation)

DLC	PD1, PD0, PDS
0	Normal operation
1	Forcibly set to the low level

When the unlocked state is detected when the channel is changed, the PDS (sub-charge pump) operates, R1 goes to RIM/R1S (R1S = 100 Ω), the low-pass filter time constant is reduced, and PLL locking is accelerated.



*: The unlock state detection bit UL1 must be set to 1. The unlock detection width is set to either ±0.5 µs or ±1.0 µs and when a phase difference larger than this is detected, the unlocked state is recognized and the sub-charge pump operates. When the state approaches the locked state and the phase difference becomes less than the amount set as the unlock detection width, the sub-charge pump stops operating and the pin goes to the high-impedance state.

Other items

(1) Notes on the phase detector dead band

DZ1	DZ0	Dead band mode	Charge pump	Dead band
0	0	DZA	ON/ON	– –0 s
0	1	DZB	ON/ON	–0 s
1	0	DZC	OFF/OFF	+0 s
1	1	DZD	OFF/OFF	++0 s

When the charge pump operates in ON/ON mode, the charge pump generates correction pulses even when the PLL is locked. Here, it is easy for the loop to become unstable, and special care is required in designs that use this mode.
The following problems may occur in ON/ON mode.

- Side bands may be generated due to reference frequency leakage.
- Side bands may be generated due low-frequency leakage due to the envelope of the correction pulses.

When a dead band is present (OFF/OFF mode), the loop will be stable, but it will be harder to acquire a good C/N ratio. On the other hand, with the mode that does not have a dead band (ON/ON mode), it will be easier to acquire a high C/N ratio, but harder to acquire loop stability.
Therefore, the DZA and DZB modes, in which there is no dead band, can be effective if either a high signal-to-noise ratio of 90 to 100 dB in FM reception or an increased pilot margin in AM stereo reception is required.
Inversely, if such a high FM signal-to-noise ratio is not required for FM reception, or an adequate pilot margin can be acquired for AM stereo reception, then the DZC and DZD modes, in which a dead band is present, may be more effective.

Dead zone (dead band) definition

The phase comparator compares fp with the reference frequency (fr) as shown in figure 1. This circuit outputs a voltage V (A) that is proportional to the phase difference ø as shown in figure 2. However, due to internal delays and other factors, the actual IC is unable to compare small phase differences, and thus a dead zone (B) appears in the output. To achieve a high signal-to-noise ratio in the end product, the dead zone should be as small as possible.

However, in popularly-priced models, there are cases where a somewhat wider dead zone may be easier to work with. This is because in some situations, such as when a powerful signal is applied to the RF input, in popularly-priced models there may be RF leakage from the mixer to the VCC. When the dead zone is narrow, outputs to correct this leakage are output, that output in turn modulates the VCO, and generates a beat signal with the RF.

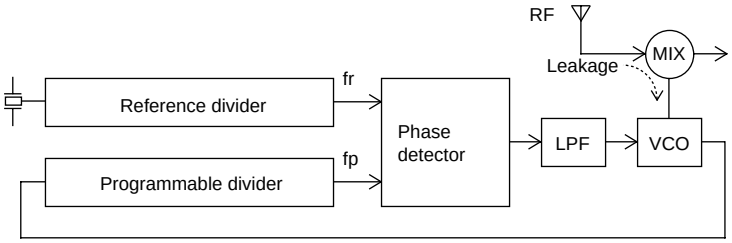


Figure 1

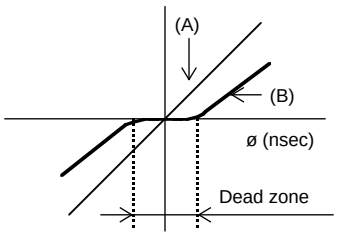


Figure 2

(2) Notes on the FMIN and HCTR pins
The coupling capacitor must be located as close as possible to these pins. A capacitance of approximately 100 pF is desirable.
In particular, if the HCTR pin capacitor is over about 1000 pF, the time required to reach the bias level may become excessive, and incorrect counting may occur due to the relationship with the wait time.

(3) Notes on the IF counting → SD must be used in conjunction with IF counting.
If the general-purpose counter is used to count the IF frequency, the application microcontroller must test the state of the IF IC SD (station detect) signal, and only if the SD signal is present, turn on the IF counter buffer output and perform an IF count operation. Methods in which auto-search operations are implemented only using the IF count may incorrectly stop at frequencies where no station is present due to leakage from the IF counter buffer.

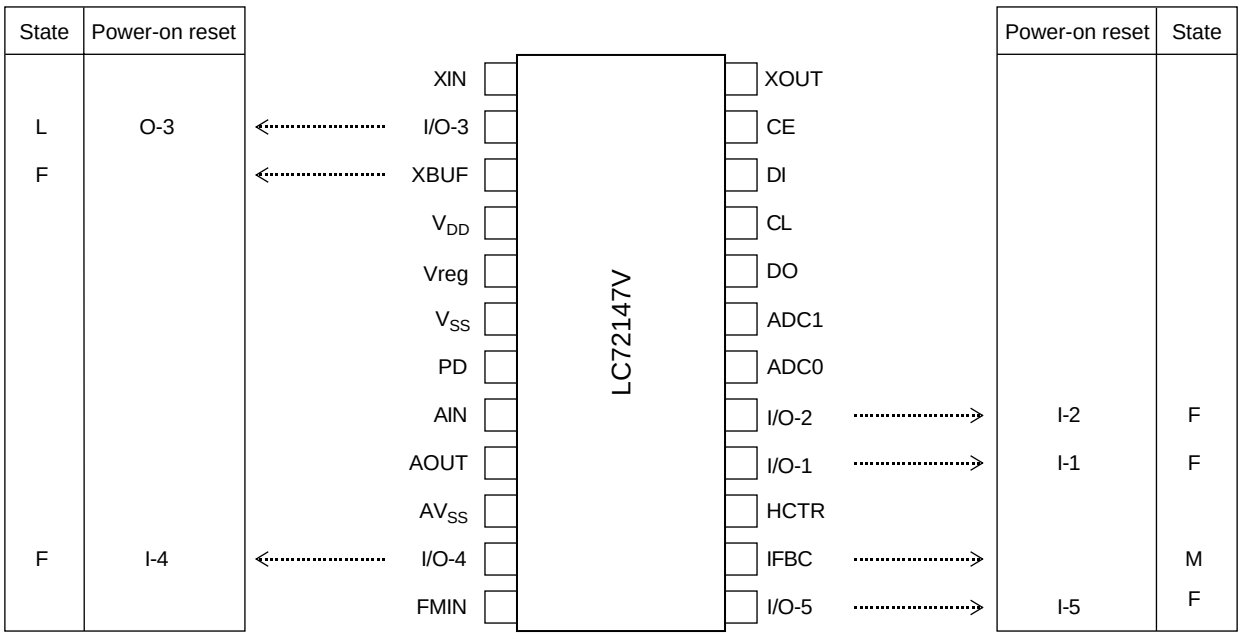
(4) Using the DO pin
At times other than data output mode, the DO pin can also be used to check for general-purpose counter count operation completion, to output the unlock state detection signal, and to check for changes in the input pins.
Note that the states of the input pins (I/O-1 and I/O-2) can be directly input to the system microcontroller through the DO pin.

(5) Power supply pins
Capacitors of over 2000 pF must be inserted between the VDD and VSS power supply pins and between Vreg and VSS to reduce noise. These capacitors must be located as close to the VDD, Vreg, and VSS pins as possible.

(6) Notes on VCO design

The VCO must be designed so that the VCO oscillation does not stop if the control voltage (Vtune) becomes 0 V. If it is possible for this oscillator to stop, use the charge pump control data (DLC) to forcible set Vtune to VCC temporarily to prevent the PLL circuit from deadlocking. (This function is called a deadlock clear circuit.)

Pin states during a power-on reset



F : Floating
L : Low
M : Medium

Sample Application Circuit