M37735S4LHP

New product

16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37735S4LHP is a microcomputer using the 7700 Family core. This microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the RAM, multiple-function timers, serial I/O, A-D converter, and so on.

Its strong points are the low power dissipation, the low supply voltage, and the small package.

FEATURES

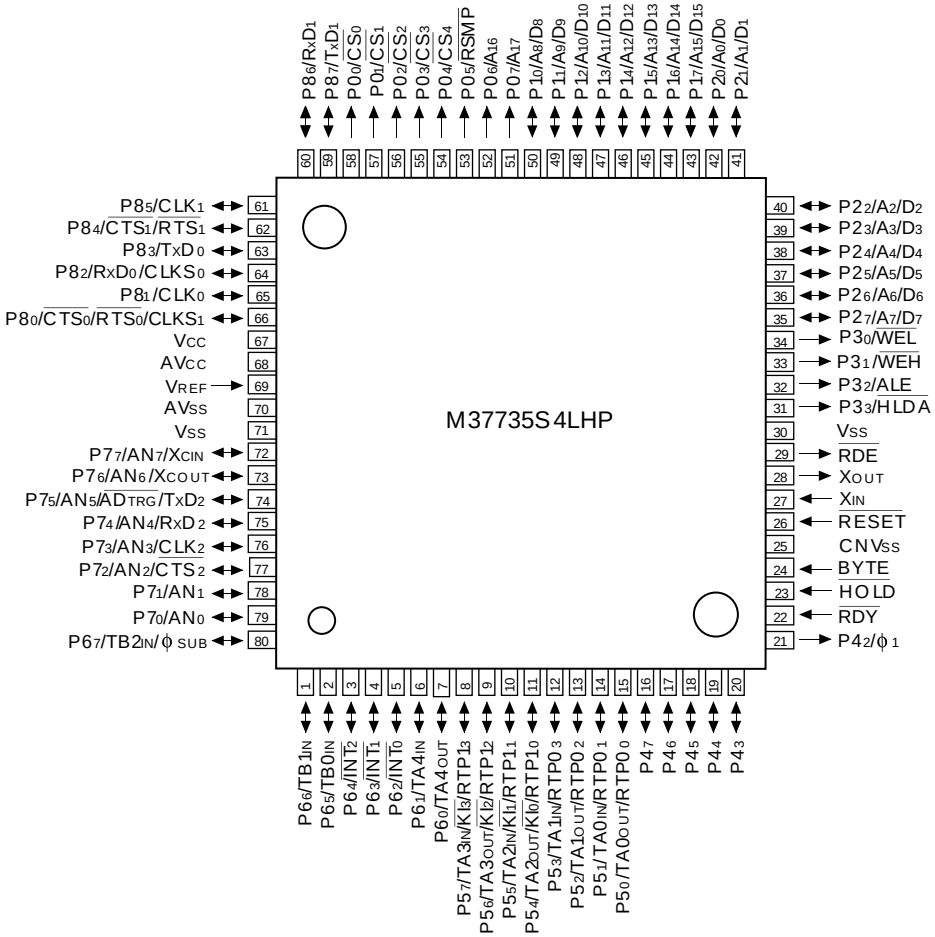
- Number of basic instructions 103
- Memory size RAM ..... 2048 bytes
- Instruction execution time
  The fastest instruction at 12 MHz frequency .....333 ns
- Single power supply ..... 2.7 – 5.5 V
- Low power dissipation (At 3 V supply voltage, 12 MHz frequency)
  ..... 10.8 mW (Typ.)
- Interrupts ..... 19 types, 7 levels
- Multiple-function 16-bit timer ..... 5 + 3
- Serial I/O (UART or clock synchronous).....3
- 10-bit A-D converter .....8-channel inputs
- 12-bit watchdog timer
- Programmable input/output
  (ports P4, P5, P6, P7, P8) 37
- Clock generating circuit ..... 2 circuits built-in
- Small package.....80-pin plastic molded fine-pitch QFP
  (80P6D-A; 0.5 mm lead pitch)

APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, and so on.

Control devices for general industrial equipment such as communication equipment, and so on.

PIN CONFIGURATION (TOP VIEW)



Outline 80P6D-A

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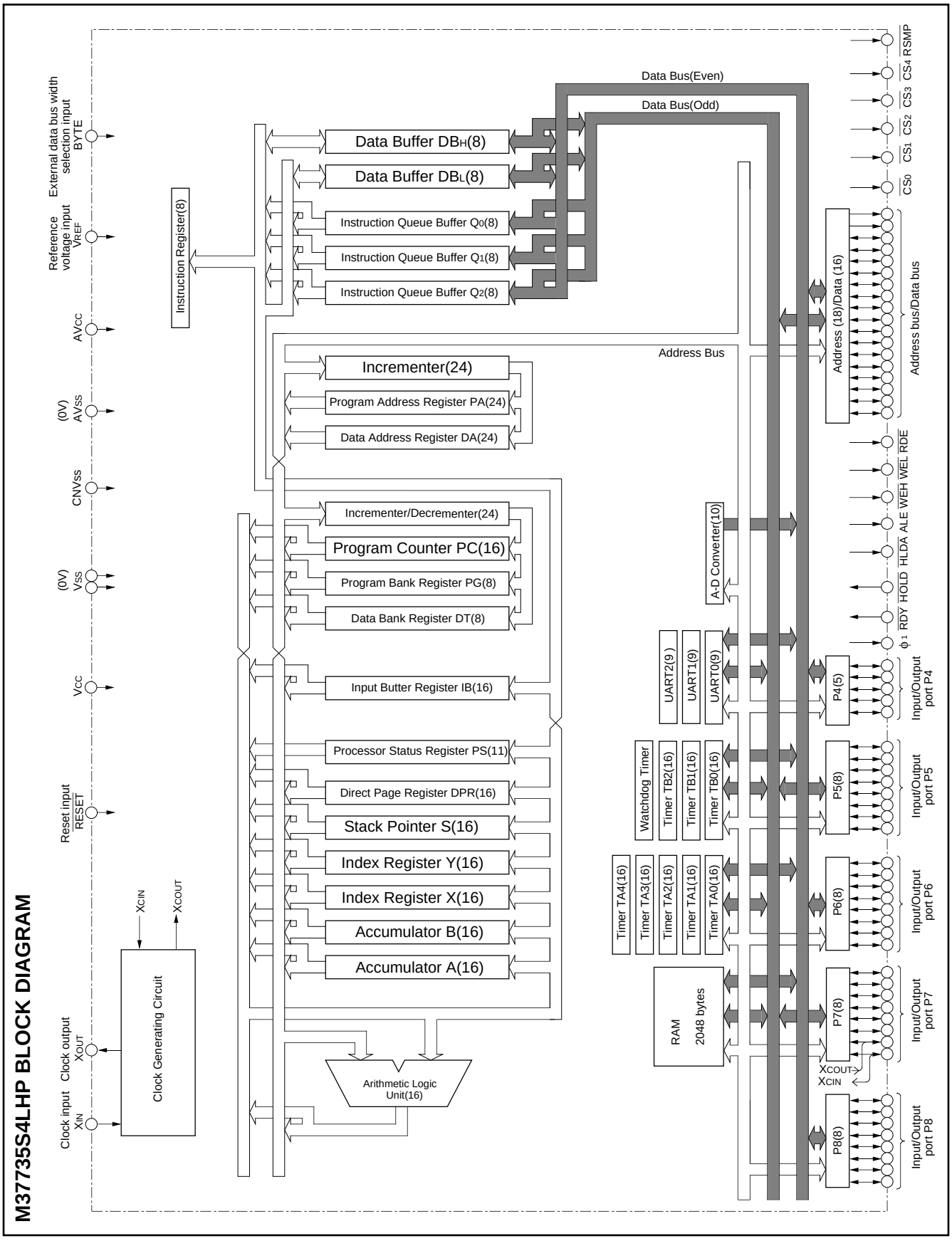
M37735S4LHP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

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FUNCTIONS OF M37735S4LHP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		333 ns (the fastest instruction at external clock 12 MHz frequency)
Memory size	RAM	2048 bytes
Input/Output ports	P5 – P8	8-bit × 4
	P4	5-bit × 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit × 5
	TB0, TB1, TB2	16-bit × 3
Serial I/O		(UART or clock synchronous serial I/O) × 3
A-D converter		10-bit × 1 (8 channels)
Watchdog timer		12-bit × 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		2.7 – 5.5 V
Power dissipation		10.8 mW (at 3 V supply voltage, external clock 12 MHz frequency)
		27 mW (at 5 V supply voltage, external clock 12 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 1 Mbytes
Operating temperature range		–40 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded fine-pitch QFP (80P6D-A; 0.5 mm lead pitch)

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	Connect to Vcc.
$\overline{RESET}$	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
X_{IN}	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin, and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{RDE}$	Read enable output	Output	When data/instruction read is performed, output level of $\overline{RDE}$ signal is "L".
BYTE	Bus width selection input	Input	This pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
$P0_0/\overline{CS_0}$ – $P0_4/\overline{CS_4}$	Chip selection output	Output	When the specified external memory area is accessed, $\overline{CS_0}$ – $\overline{CS_4}$ signals are "L".
$P0_5/\overline{RSMP}$	Ready sampling output	Output	The timing signal to be input to the $\overline{RDY}$ pin is output.
$P0_6/A_{16}$, $P0_7/A_{17}$	Address output	Output	An address (A_{16}, A_{17}) is output.
$P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$	Address output /data (high -order) I/O	I/O	When the BYTE pin is set to "L" and external data bus has a 16-bit width, high-order data (D_8 – D_{15}) is input/output or an address (A_8 – A_{15}) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address (A_8 – A_{15}) is output.
$P2_0/A_0/D_0$ – $P2_7/A_7/D_7$	Address output /data (low -order) I/O	I/O	Low-order data (D_0 – D_7) is input/output or an address (A_0 – A_7) is output.
$P3_0/\overline{WEL}$	Write enable output	Output	When the BYTE pin is "L" and writing to an even address is performed, output level of $\overline{WEL}$ signal is "L". When the BYTE pin is "H" and writing to an even address or an odd address is performed, output level of $\overline{WEL}$ signal is "L".
$P3_1/\overline{WEH}$	Write enable high output	Output	When the BYTE pin is "L" and writing to an odd address is performed, output level of $\overline{WEH}$ signal is "L". When the BYTE pin is "H", $\overline{WEH}$ signal is always "H".
$P3_2$/ALE	Address latch enable output	Output	This is used to retrieve only the address from the multiplex signal which consists of address and data.
$P3_3/\overline{HLDA}$	Hold acknow-ledge output	Output	This outputs "L" level when the microcomputer enters hold state after a hold request is accepted.
$\overline{HOLD}$	Hold request input	Input	This is an input pin for $\overline{HOLD}$ request signal. The microcomputer enters hold state while this signal is "L".
$\overline{RDY}$	Ready input	Input	This is an input pin for $\overline{RDY}$ signal. The microcomputer enters ready state while this signal is "L".
$P4_2/\phi_1$	Clock output	Output	This pin outputs the clock ϕ_1.
$P4_3$ – $P4_7$	I/O port P4	I/O	These pins become a 5-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset.
$P5_0$ – $P5_7$	I/O port P5	I/O	In addition to having the same functions as port P4, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input ($\overline{KI_0}$ – $\overline{KI_3}$).
$P6_0$ – $P6_7$	I/O port P6	I/O	In addition to having the same functions as port P4, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{INT_0}$ – $\overline{INT_2}$) and input pins for timers B0 to B2. $P6_7$ also functions as sub-clock ϕ_{SUB} output pin.
$P7_0$ – $P7_7$	I/O port P7	I/O	In addition to having the same functions as port P4, these pins function as input pins for A-D converter. $P7_2$ to $P7_5$ also function as I/O pins for UART2. Additionally, $P7_6$ and $P7_7$ have the function as the output pin (X_{COUT}) and the input pin (X_{CIN}) of the sub-clock (32 kHz) oscillation circuit, respectively. When $P7_6$ and $P7_7$ are used as the X_{COUT} and X_{CIN} pins, connect a resonator or an oscillator between the both.
$P8_0$ – $P8_7$	I/O port P8	I/O	In addition to having the same functions as port P4, these pins also function as I/O pins for UART 0 and UART 1.

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BASIC FUNCTION BLOCKS

The M37735S4LHP has the same functions as the M37735MHBXXXFP except for the following:

(1) The memory map is different.
(2) The processor mode is different.
(3) The reset circuit is different.
(4) Pulse output port mode of timer A is available.
(5) The function of ROM area modification is not available.

Refer to the section on the M37735MHBXXXFP, except for above (1)–(5).

MEMORY

The memory map is shown in Figure 1. The address space has a capacity of 16 Mbytes and is allocated to addresses from 0_{16} to $FFFFFF_{16}$. The address space is divided by 64-Kbyte unit called bank. The banks are numbered from 0_{16} to FF_{16}.

However, banks 10_{16}–FF_{16} of the M37735S4LHP cannot be accessed.

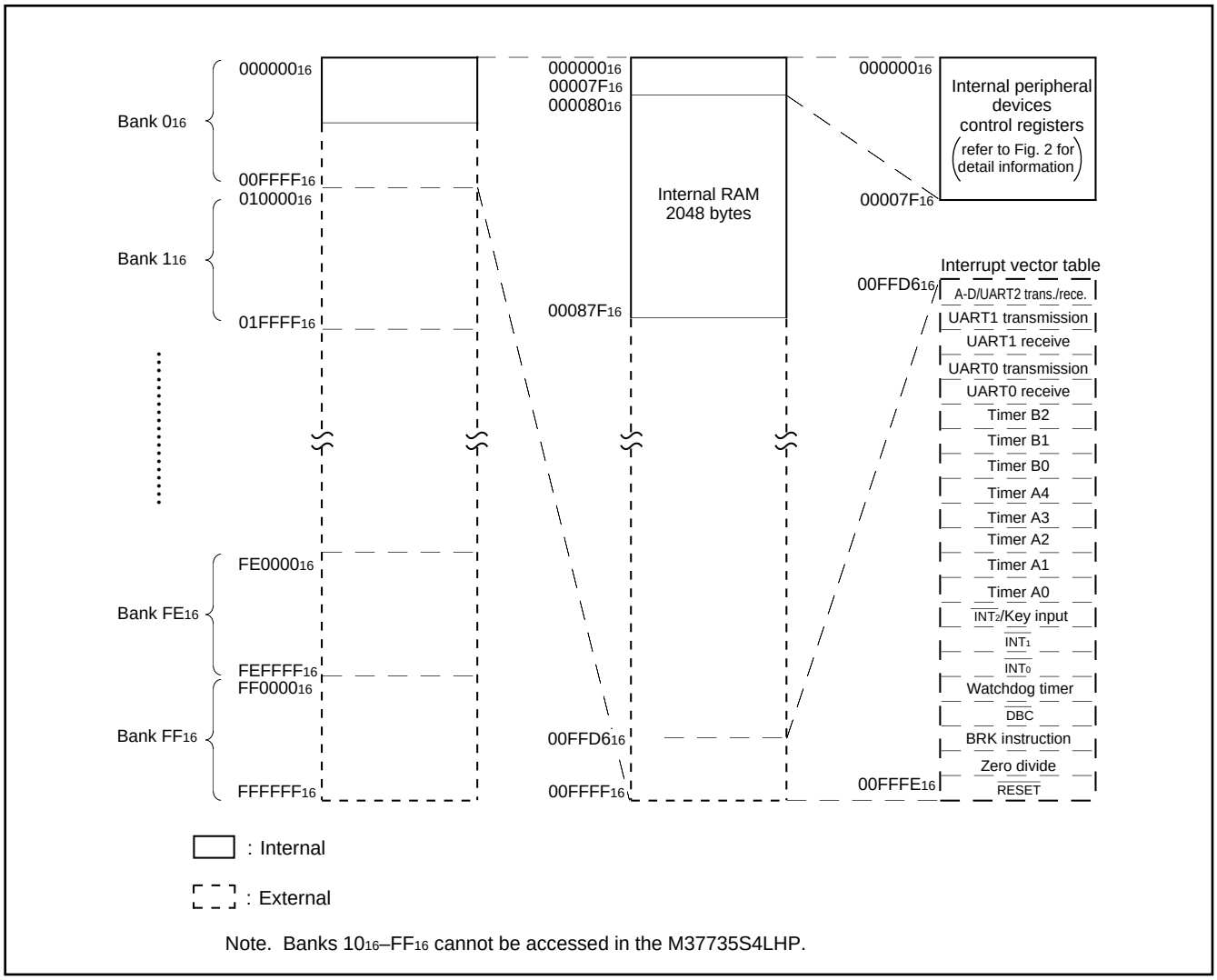
Built-in RAM and control registers for internal peripheral devices are assigned to bank 0_{16}.

Addresses $FFD6_{16}$ to $FFFF_{16}$ are the RESET and interrupt vector addresses and contain the interrupt vectors. Use ROM for memory of this address.

The 2048-byte area allocated to addresses from 80_{16} to $87F_{16}$ is the built-in RAM. In addition to storing data, the RAM is used as stack during a subroutine call or interrupts.

Peripheral devices such as I/O ports, A-D converter, serial I/O, timer, and interrupt control registers are allocated to addresses from 0_{16} to $7F_{16}$.

A 256-byte direct page area can be allocated anywhere in bank 0_{16} by using the direct page register (DPR). In the direct page addressing mode, the memory in the direct page area can be accessed with two words. Hence program steps can be reduced.



Note. Banks 10_{16}–FF_{16} cannot be accessed in the M37735S4LHP.

Fig. 1 Memory map

Address (Hexadecimal notation)	
000000	
000001	
000002	Port P0 register
000003	Port P1 register
000004	Port P0 direction register
000005	Port P1 direction register
000006	Port P2 register
000007	Port P3 register
000008	Port P2 direction register
000009	Port P3 direction register
00000A	Port P4 register
00000B	Port P5 register
00000C	Port P4 direction register
00000D	Port P5 direction register
00000E	Port P6 register
00000F	Port P7 register
000010	Port P6 direction register
000011	Port P7 direction register
000012	Port P8 register
000013	
000014	Port P8 direction register
000015	
000016	
000017	
000018	
000019	
00001A	
00001B	
00001C	Pulse output data register 1
00001D	Pulse output data register 0
00001E	A-D control register 0
00001F	A-D control register 1
000020	A-D register 0
000021	
000022	A-D register 1
000023	
000024	A-D register 2
000025	
000026	A-D register 3
000027	
000028	A-D register 4
000029	
00002A	A-D register 5
00002B	
00002C	A-D register 6
00002D	
00002E	A-D register 7
00002F	
000030	UART 0 transmit/receive mode register
000031	UART 0 baud rate register (BRG0)
000032	UART 0 transmission buffer register
000033	
000034	UART 0 transmit/receive control register 0
000035	UART 0 transmit/receive control register 1
000036	UART 0 receive buffer register
000037	
000038	UART 1 transmit/receive mode register
000039	UART 1 baud rate register (BRG1)
00003A	UART 1 transmission buffer register
00003B	
00003C	UART 1 transmit/receive control register 0
00003D	UART 1 transmit/receive control register 1
00003E	UART 1 receive buffer register
00003F	

Address (Hexadecimal notation)	
000040	Count start flag
000041	
000042	One-shot start flag
000043	
000044	Up-down flag
000045	
000046	Timer A0 register
000047	
000048	Timer A1 register
000049	
00004A	Timer A2 register
00004B	
00004C	Timer A3 register
00004D	
00004E	Timer A4 register
00004F	
000050	Timer B0 register
000051	
000052	Timer B1 register
000053	
000054	Timer B2 register
000055	
000056	Timer A0 mode register
000057	Timer A1 mode register
000058	Timer A2 mode register
000059	Timer A3 mode register
00005A	Timer A4 mode register
00005B	Timer B0 mode register
00005C	Timer B1 mode register
00005D	Timer B2 mode register
00005E	Processor mode register 0
00005F	Processor mode register 1
000060	Watchdog timer register
000061	Watchdog timer frequency selection flag
000062	Waveform output mode register
000063	Reserved area **(Note)**
000064	UART2 transmit/receive mode register
000065	UART2 baud rate register (BRG2)
000066	UART2 transmission buffer register
000067	
000068	UART2 transmit/receive control register 0
000069	UART2 transmit/receive control register 1
00006A	UART2 receive buffer register
00006B	
00006C	Oscillation circuit control register 0
00006D	Port function control register
00006E	Serial transmit control register
00006F	Oscillation circuit control register 1
000070	A-D/UART2 trans./rece. interrupt control register
000071	UART 0 transmission interrupt control register
000072	UART 0 receive interrupt control register
000073	UART 1 transmission interrupt control register
000074	UART 1 receive interrupt control register
000075	Timer A0 interrupt control register
000076	Timer A1 interrupt control register
000077	Timer A2 interrupt control register
000078	Timer A3 interrupt control register
000079	Timer A4 interrupt control register
00007A	Timer B0 interrupt control register
00007B	Timer B1 interrupt control register
00007C	Timer B2 interrupt control register
00007D	$\overline{INT_0}$ interrupt control register
00007E	$\overline{INT_1}$ interrupt control register
00007F	$\overline{INT_2}$/Key input interrupt control register

Note. Writing to reserved area is disabled.

Fig. 2 Location of internal peripheral devices and interrupt control registers

Pulse output port mode

The pulse motor drive waveform can be output by using plural internal timer A.

Figure 3 shows a block diagram for pulse output port mode. In the pulse output port mode, two pairs of four-bit pulse output ports are used. Whether using pulse output port or not can be selected by waveform output selection bit (bit 0, bit 1) of waveform output mode register (62_{16} address) shown in Figure 4. When bit 0 of waveform output selection bit is set to "1", $RTP1_0$, $RTP1_1$, $RTP1_2$, and $RTP1_3$ are used as pulse output ports, and when bit 1 of waveform output selection bit is set to "1", $RTP0_0$, $RTP0_1$, $RTP0_2$, and $RTP0_3$ are used as pulse output ports. When bits 1 and 0 of waveform output selection bit are set to"1", $RTP1_0$, $RTP1_1$, $RTP1_2$, and $RTP1_3$, and $RTP0_0$, $RTP0_1$, $RTP0_2$, and $RTP0_3$ are used as pulse output ports. The ports not used as pulse output ports can be used as normal parallel ports, timer input/output or key input interruput input.

In the pulse output port mode, set timers A0 and A2 to timer mode as timers A0 and A2 are used. Figure 5 shows the bit configuration of timer A0, A2 mode registers in pulse output port mode.

Data can be set in each bit of the pulse output data register corresponding to four ports selected as pulse output ports. Figure 6 shows the bit configuration of the pulse output data register. The contents of the pulse output data register 1 (low-order four bits of $1C_{16}$ address) corresponding to $RTP1_0$, $RTP1_1$, $RTP1_2$, and $RTP1_3$ is output to the ports each time the counter of timer A2 becomes 0000_{16}. The contents of the pulse output data register 0 (low-order four bits of $1D_{16}$ address) corresponding to $RTP0_0$, $RTP0_1$, $RTP0_2$, and $RTP0_3$ is output to the ports each time the counter of timer A0 becomes 0000_{16}.

Figure 7 shows example of waveforms in pulse output port mode.

When "0" is written to a specified bit of the pulse output data register, "L" level is output to the corresponding pulse output port when the counter of corresponding timer becomes 0000_{16}, and when "1" is written, "H" level is output to the pulse output port.

Pulse width modulation can be applied to each pulse output port. Since pulse width modulation involves the use of timers A1 and A3, activate these timers in pulse width modulation mode.

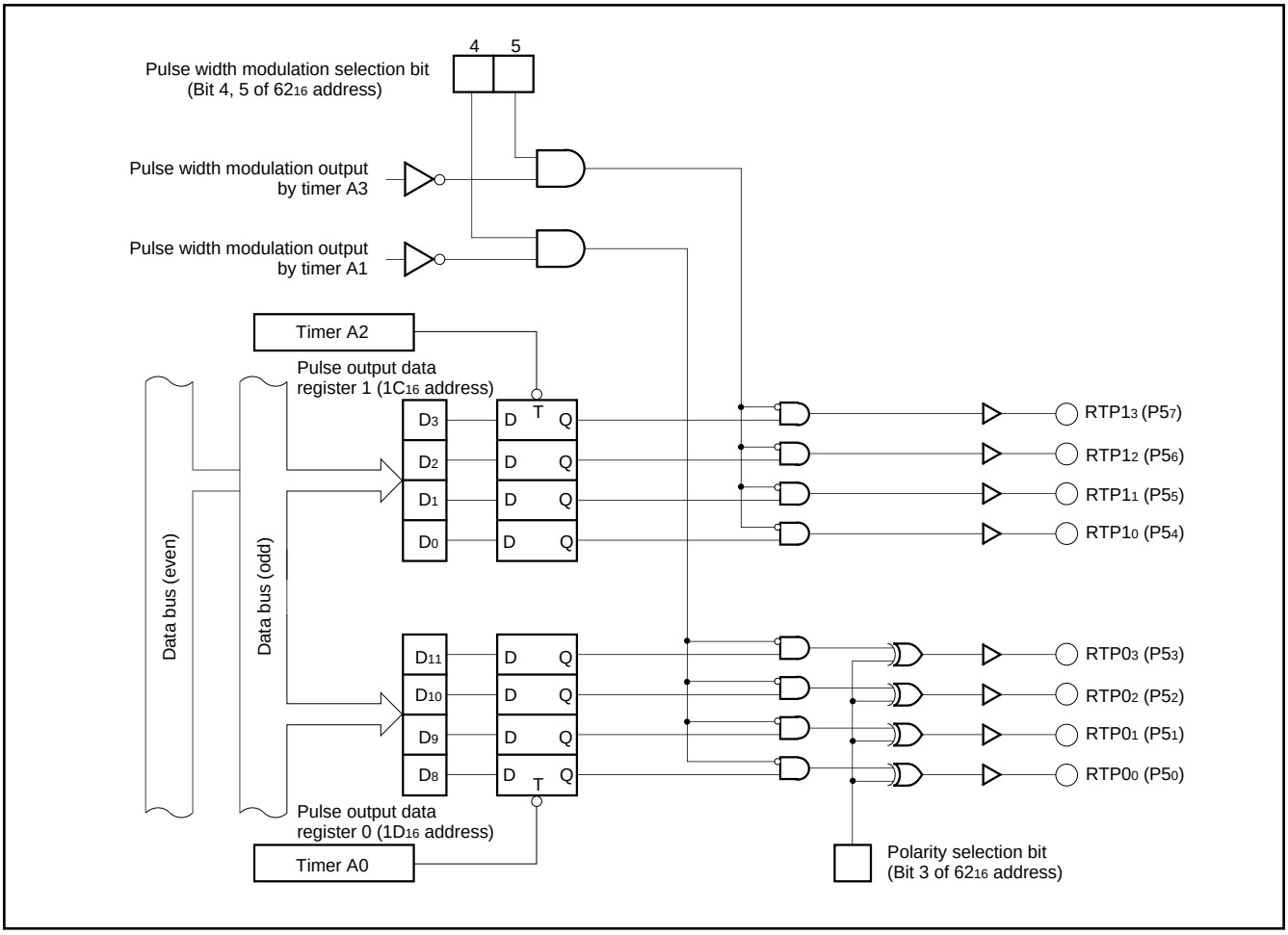


Fig. 3 Block diagram for pulse output port mode

RTP1$_0$, RTP1$_1$, RTP1$_2$, and RTP1$_3$ are applied pulse width modulation by timer A3 by setting the pulse width modulation selection bit by timer A3 (bit 5) of the waveform output mode register to "1".
RTP0$_0$, RTP0$_1$, RTP0$_2$, and RTP0$_3$ are applied pulse width modulation by timer A1 by setting the pulse width modulation selection bit by timer A1 (bit 4) of the waveform output mode register to "1".
The contents of the pulse output data register 0 can be reversed and output to pulse output ports RTP0$_0$, RTP0$_1$, RTP0$_2$, and RTP0$_3$ by the polarity selection bit (bit 3) of the waveform output mode register. When the polarity selection bit is "0", the contents of the pulse output data register 0 is output unchangeably, and when "1", the contents of the pulse output data register 0 is reversed and output. When pulse width modulation is applied, likewise the polarity reverse to pulse width modulation can be selected by the polarity selection bit.

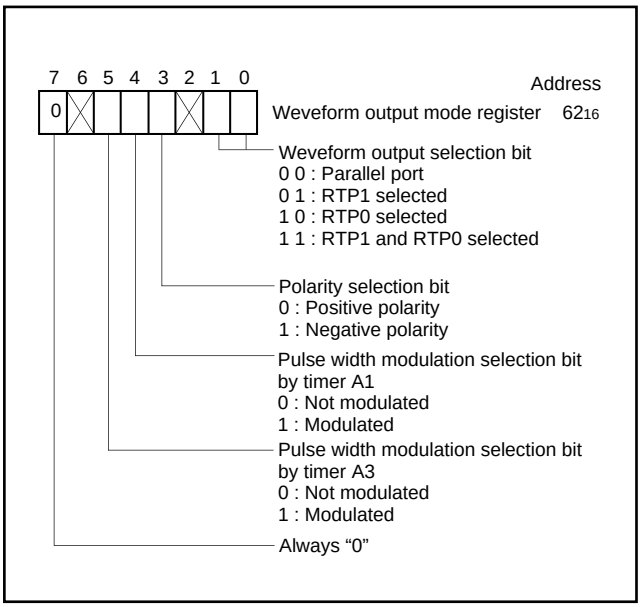


Fig. 4 Waveform output mode register bit configuration

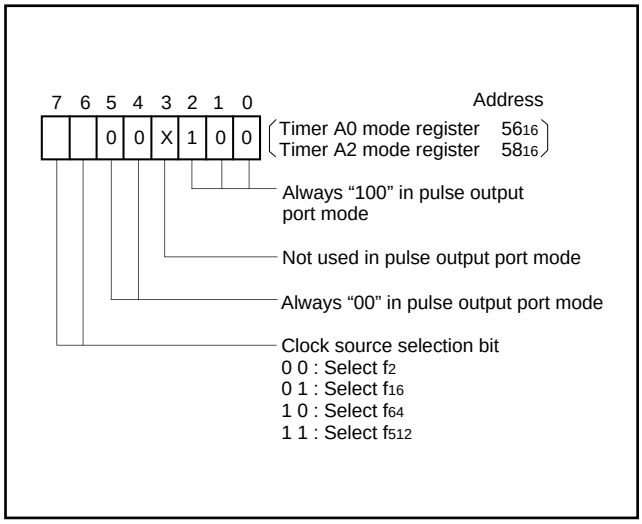


Fig. 5 Timer A0, A2 mode register bit configuration in pulse output port mode

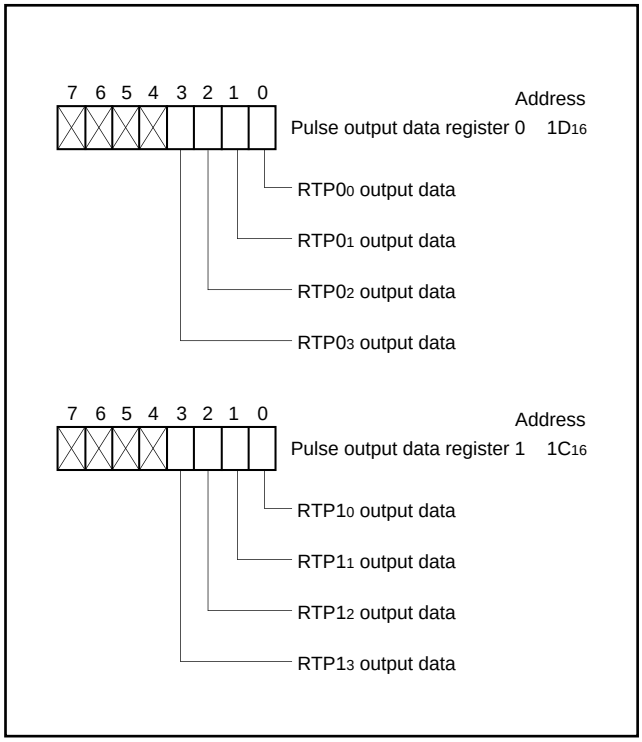


Fig. 6 Pulse output data register bit configuration

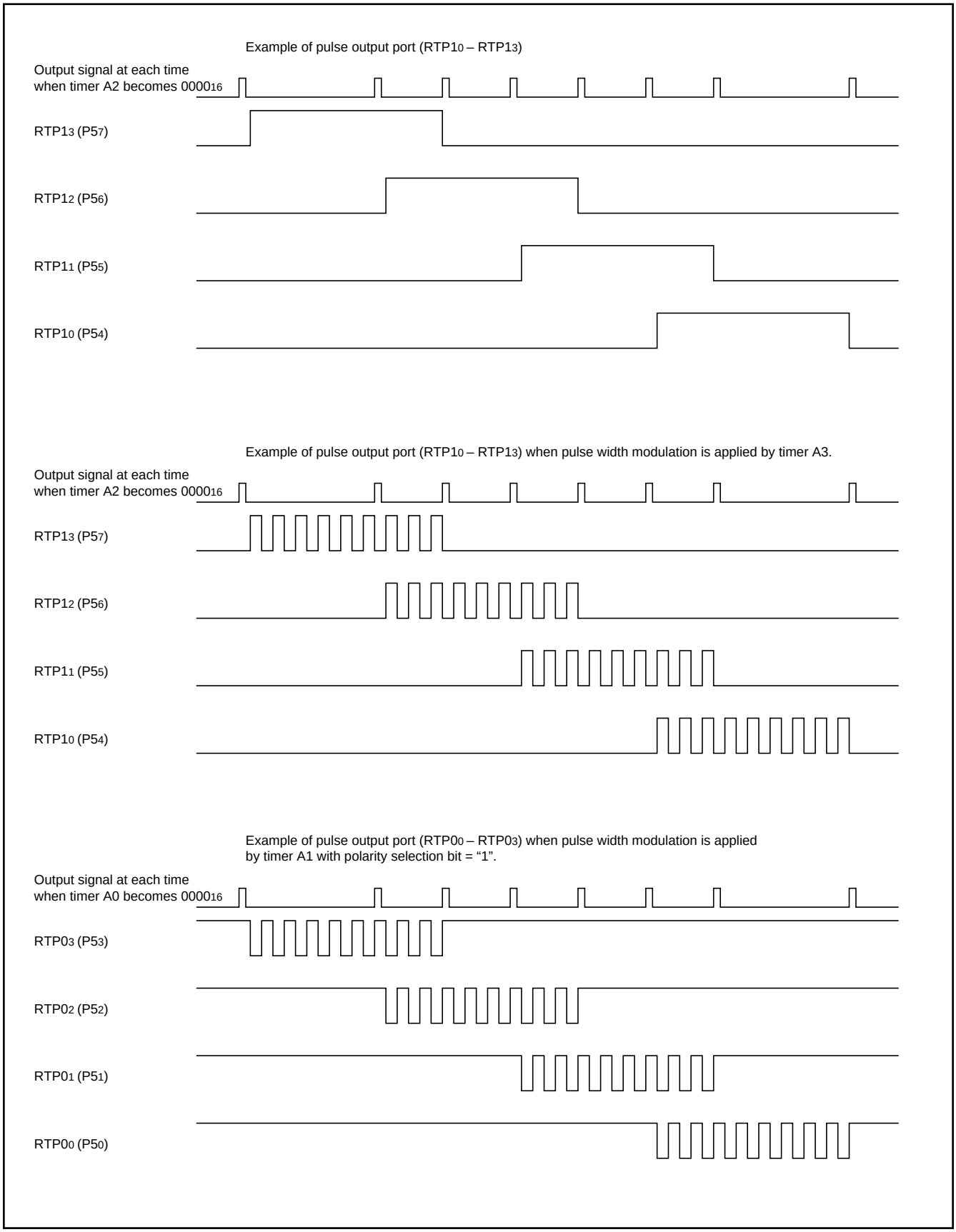


Fig. 7 Example of waveforms in pulse output port mode

PROCESSOR MODE

Only the microprocessor mode can be selected.

Figure 9 shows the functions of pins $P0_0/\overline{CS_0}$ – $P4_7$ in the microprocessor mode.

Figure 10 shows external memory area for the microprocessor mode. Access to the external memory is affected by the BYTE pin, the wait bit (bit 2 of the processor mode register 0 at address $5E_{16}$), and the wait selection bit (bit 0 of the processor mode register 1 at address $5F_{16}$) .

• BYTE pin

When accessing the external memory, the level of the BYTE pin is used to determine whether to use the data bus as 8-bit width or 16-bit width.

The data bus has a width of 8 bits when level of the BYTE pin is “H”, and pins $P2_0/A_0/D_0$ — $P2_7/A_7/D_7$ are the data I/O pins.

The data bus has a width of 16 bits when the level of the BYTE pin is “L”, and pins $P2_0/A_0/D_0$ — $P2_7/A_7/D_7$ and pins $P1_0/A_8/D_8$ — $P1_7/A_{15}/D_{15}$ are the data I/O pins.

When accessing the internal memory, the data bus always has a width of 16 bits regardless of the BYTE pin level.

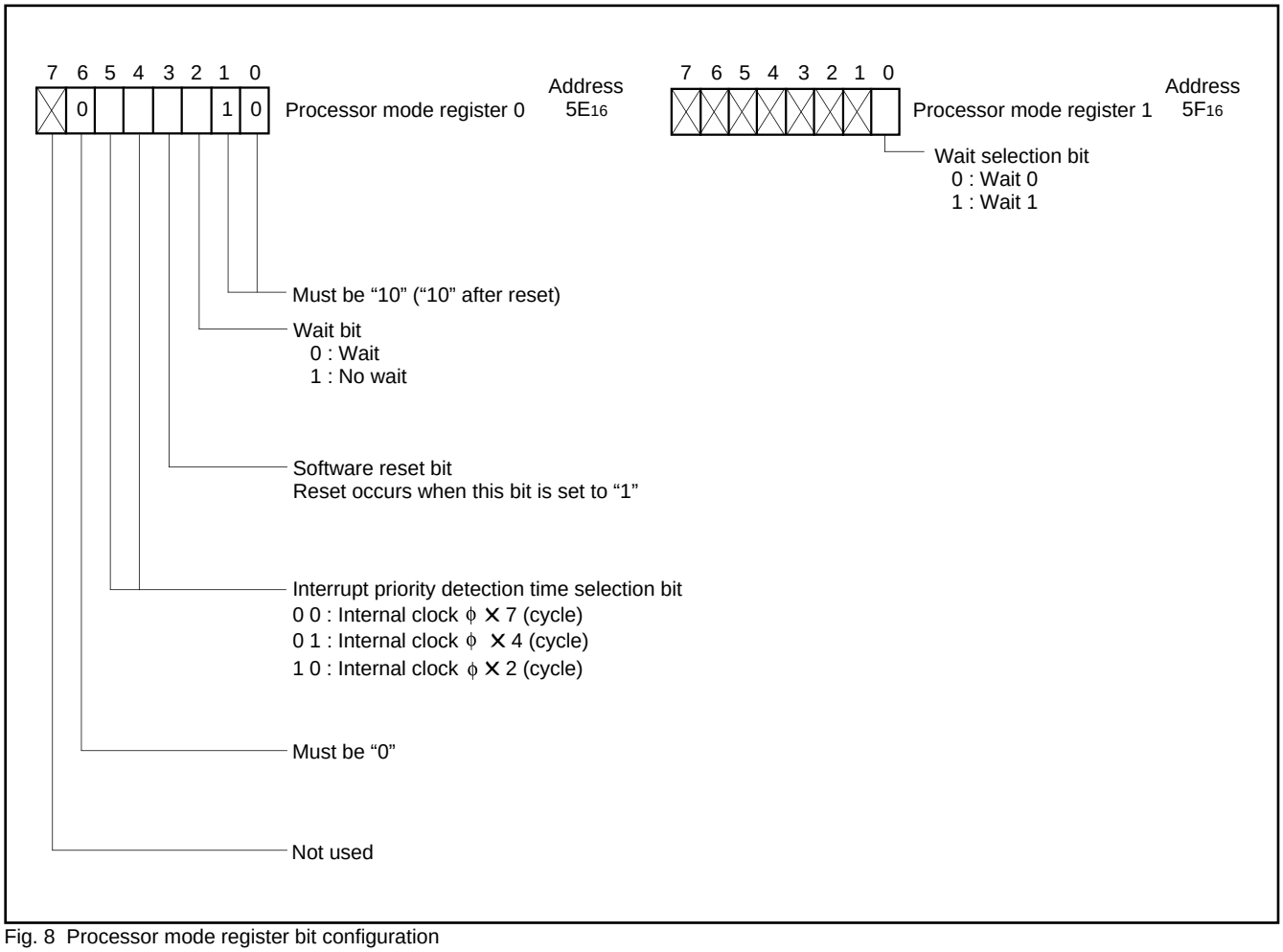


Fig. 8 Processor mode register bit configuration

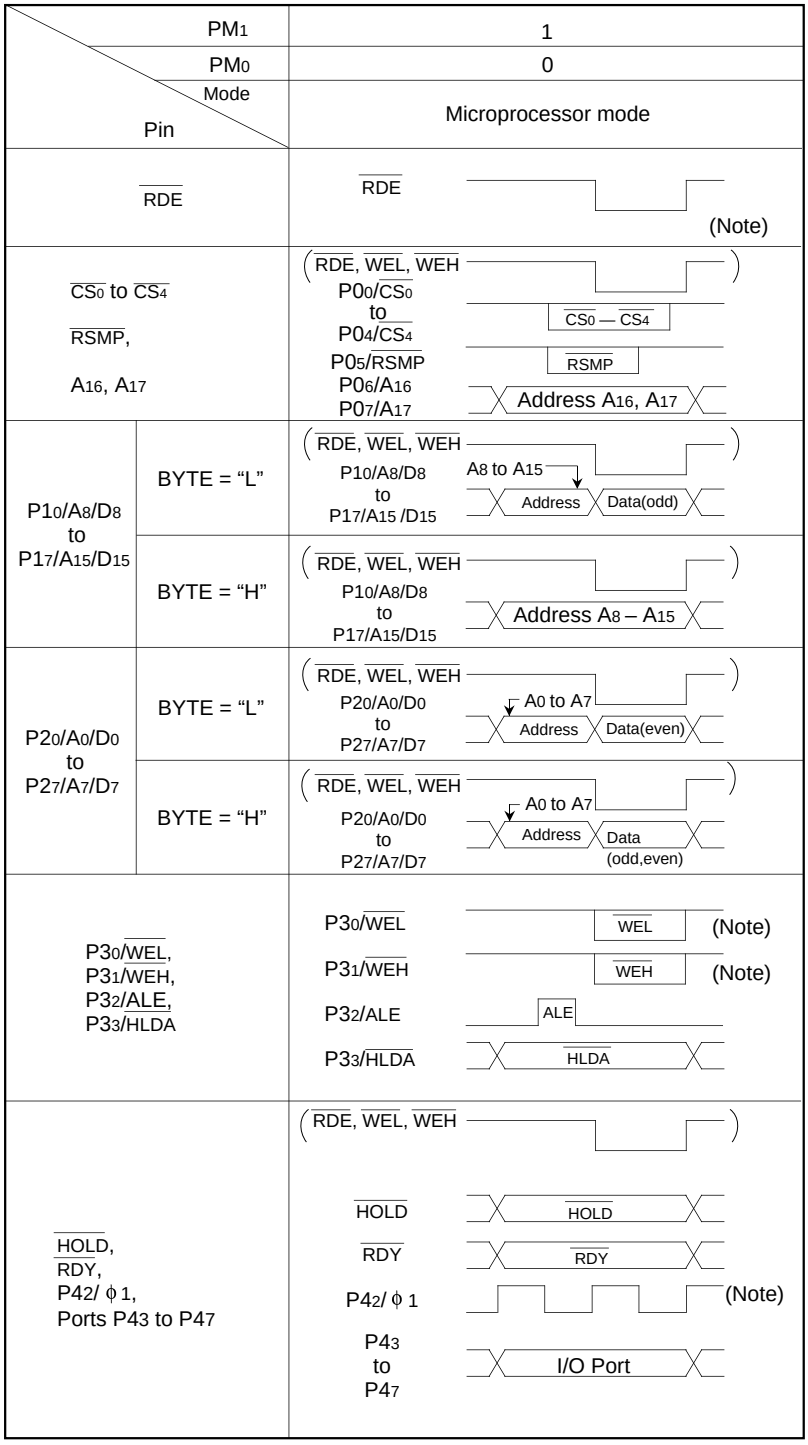


Fig. 9 Functions of pins P00/CS0 to P47 in microprocessor mode

Note. The signal output disable selection bit (bit 6 of the oscillation circuit control register 0) can stop the φ1 output in the microprocessor mode. In this mode, signals RDE, WEL, WEH can also be fixed to "H" when the internal memory area is accessed.

• Wait bit

As shown in Figure 11, when the external memory area is accessed with the wait bit (bit 2 of the processor mode register 0 at address $5E_{16}$) cleared to “0”, the access time can be extended compared with no wait (the wait bit is “1”).
The access time is extended in two ways and this is selected with the wait selection bit (bit 0 of the processor mode register 1 at address $5F_{16}$).
When this bit is “1”, the access time is 1.5 times compared to that for no wait. When this bit is “0”, the access time is twice compared to that for no wait.
At reset, the wait bit and the wait selection bit are “0”.
Access to internal memory area is always performed in the no wait mode regardless of the wait bit.
The processor modes are described below.

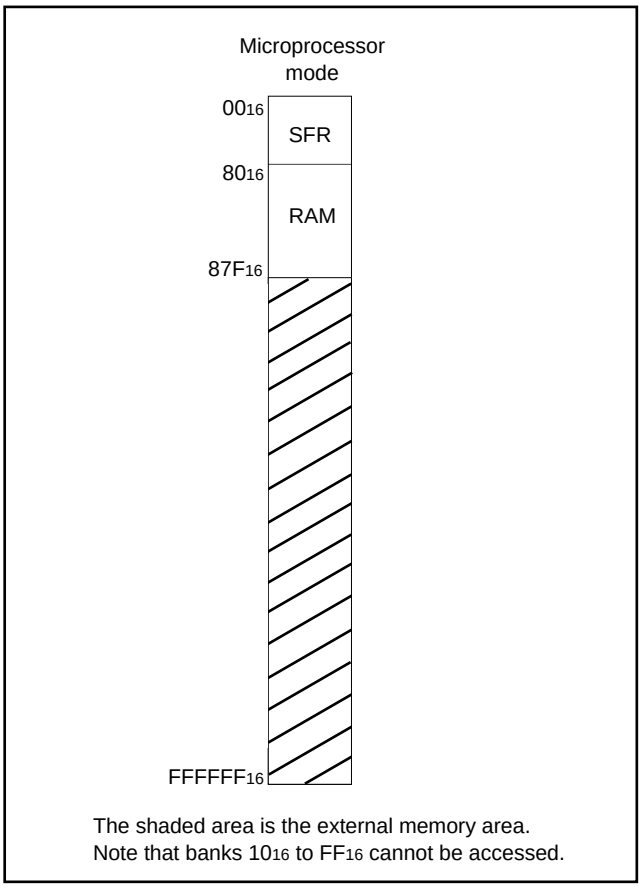


Fig. 10 External memory area for microprocessor mode

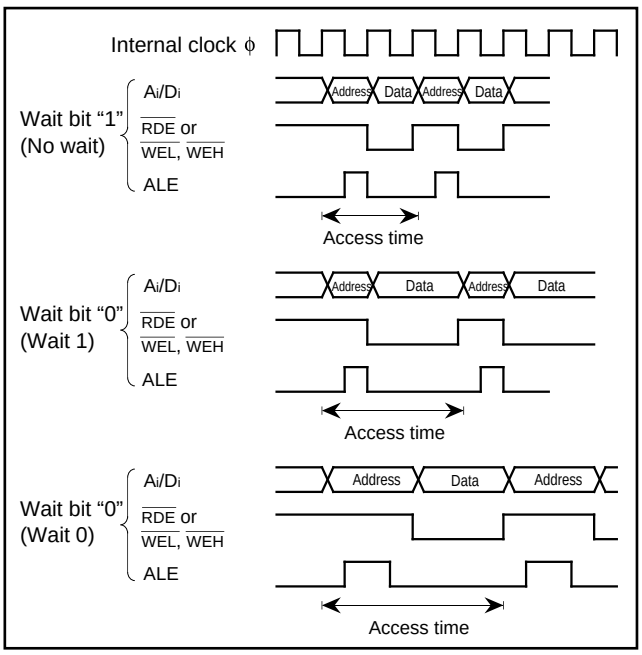


Fig. 11 Relationship between wait bit, wait selection bit, and access time

(1) Microprocessor mode [10]

The microcomputer enters the microprocessor mode after connecting the CNVss pin to Vcc and starting from reset.
Pin $\overline{RDE}$ is the output pin for the read enable signal ($\overline{RDE}$).
$\overline{RDE}$ is “L” during the data read term in the read cycle. When the internal memory area is read, $\overline{RDE}$ can be fixed to “H” by setting the signal output disable selection bit (bit 6 of the oscillation circuit control register 0) to “1”.

$\overline{CS_0}$ to $\overline{CS_4}$ are the chip select signals and are "L" when the address shown in Table 2 is accessed. $\overline{RSMP}$ is the ready-sampling signal which is output for the $\overline{RDY}$ input described later when the external memory area is accessed. By inputting logical AND of $\overline{RSMP}$ and $\overline{CS_n}$ (n = 0 to 4) to the $\overline{RDY}$ pin, read/write term for any address areas can be extended by 1 cycle of clock ϕ_1. In addition, the read/write term can also be extended by 2 cycles of clock ϕ_1 if the above function and wait 0/1 function specified with the wait bit are used together.

Pins $P1_0/A_8/D_8$ — $P1_7/A_{15}/D_{15}$ have two functions depending on the level of the BYTE pin.

When the BYTE pin level is "L", pins $P1_0/A_8/D_8$ — $P1_7/A_{15}/D_{15}$ function as address (A_8 to A_{15}) output pins while $\overline{RDE}$ or $\overline{WEL}$, $\overline{WEH}$ are "H" and as odd address data I/O pins while these signals are "L". However, if an internal memory is read, external data is ignored while $\overline{RDE}$ is "L".

When the BYTE pin level is "H", pins $P1_0/A_8/D_8$ — $P1_7/A_{15}/D_{15}$ function as address (A_8 to A_{15}) output pins.

Pins $P2_0/A_0/D_0$ — $P2_7/A_7/D_7$ have two functions depending on the level of the BYTE pin.

When the BYTE pin level is "L", pins $P2_0/A_0/D_0$ — $P2_7/A_7/D_7$ function as address (A_0 to A_7) output pins while $\overline{RDE}$ or $\overline{WEL}$, $\overline{WEH}$ are "H" and as even address data I/O pins while these signals are "L". However, if an internal memory is read, external data is ignored while $\overline{RDE}$ is "L".

When the BYTE pin level is "H", pins $P2_0/A_0/D_0$ — $P2_7/A_7/D_7$ function as address (A_0 to A_7) output pins while $\overline{RDE}$ or $\overline{WEL}$, $\overline{WEH}$ are "H" and as even and odd address data I/O pins while these signals are "L". However, if an internal memory is read, external data is ignored while $\overline{RDE}$ is "L".

$\overline{WEL}$, $\overline{WEH}$ are the write-enable low signal and the write-enable high signal, respectively. These signals are "L" during the data write term of the write cycle, but their operations differ depending on the BYTE pin level.

In the case the BYTE pin level is "L", $\overline{WEL}$ is "L" when writing to an even address, $\overline{WEH}$ is "L" when writing to an odd address, and both $\overline{WEL}$ and $\overline{WEH}$ are "L" when writing to even and odd addresses.

In the case the BYTE pin level is "H", regardless of address, only $\overline{WEL}$ is "L", and $\overline{WEH}$ retains "H". $\overline{WEL}$ and $\overline{WEH}$ can also be fixed to "H" when the internal memory is accessed, same as $\overline{RDE}$, by writing "1" to the signal output disable selection bit.

ALE is an address latch enable signal used to latch the address signal from a multiplexed signal of address and data. The latch is transparent while ALE is "H" to let the address signal pass through and held while ALE is "L".

$\overline{HLDA}$ is a hold acknowledge signal and is used to notify externally when the microcomputer receives $\overline{HOLD}$ input and enters into hold state.

$\overline{HOLD}$ is a hold request signal. It is an input signal used to put the microcomputer in hold state. $\overline{HOLD}$ input is accepted when the internal clock ϕ falls from "H" level to "L" level while the bus is not used.

Pins $P0_0/\overline{CS_0}$ — $P3_1/\overline{WEH}$ and $\overline{RDE}$ are floating while the microcomputer stays in hold state. After $\overline{HLDA}$ signal changes to "L" level and one cycle of internal clock ϕ passed, these ports become floating. After $\overline{HLDA}$ signal changes to "H" level and one cycle of internal clock ϕ passed, these ports are released from floating state.

$\overline{RDY}$ is a ready signal. If this signal goes "L", the internal clock ϕ stops at "L". $\overline{RDY}$ is used when slow external memory is attached.

$P4_2/\phi_1$ pin is an output pin for clock ϕ_1. The ϕ_1 output is independent of $\overline{RDY}$ and does not stop even when internal clock ϕ stops because of "L" input to the $\overline{RDY}$ pin.

As shown in Table 3, ϕ_1 output can be stopped with the signal output disable selection bit = "1". In this case, write "1" to the port $P4_2$ direction register.
Table 1 shows the relationship between the CNVss pin input level and the processor mode.

Table 1. Relationship between CNVss pin input levels and processor mode

CNVss	Mode	Description
Vcc	• Microprocessor	Microprocessor mode upon starting after reset.

Table 2. Relationship between access addresses and chip-select signals $\overline{CS_0}$ to $\overline{CS_4}$

Chip-select signal	Area	Access address
		Microprocessor mode
$\overline{CS_0}$	The first half of bank 00_{16} except internal memory area	$00\ 0880_{16}$ to $00\ 7FFF_{16}$
$\overline{CS_1}$	The latter half of bank 00_{16} except internal memory area and banks 01_{16} to 03_{16}.	$00\ 8000_{16}$ to $03\ FFFF_{16}$
$\overline{CS_2}$	Banks 04_{16} to 07_{16}	$04\ 0000_{16}$ to $07\ FFFF_{16}$
$\overline{CS_3}$	Banks 08_{16} to $0B_{16}$	$08\ 0000_{16}$ to $0B\ FFFF_{16}$
$\overline{CS_4}$	Banks $0C_{16}$ to $0F_{16}$	$0C\ 0000_{16}$ to $0F\ FFFF_{16}$

Table 3. Function of signal output disable selection bit CM_6 (bit 6 of oscillation circuit control register 0)

Processor mode	Pin	Function	
		CM_6 = "0"	CM_6 = "1"
Microprocessor mode	$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$	$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$ are output when the internal/external memory area is accessed.	$\overline{RDE}$, $\overline{WEL}$, $\overline{WEH}$ are output only when the external memory area is accessed.
	$\overline{RDE}$	After WIT/STP instruction is executed, "H" is output.	"L" is output after WIT/STP instruction is executed ∗ Standby state selection bit (bit 0 of port function control register) must be set to "1".
	ϕ_1	Clock ϕ_1 is output independent of ϕ_1 output selection bit.	"H" or "L" is output. (Contents of $P4_2$ port latch is output.) ∗ Port $P4_2$ direction register must be set to "1".

Note. Functions shown in Table 3 cannot be emulated with a debugger. For the oscillation circuit control register 0 and port function control register, refer to Figures 64 and 11 in data sheet "M37735MHBXXXFP", respectively.

RESET CIRCUIT

The microcomputer is released from the reset state when the $\overline{\text{RESET}}$ pin is returned to "H" level after holding it at "L" level with the power source voltage at 2.7 to 5.5 V. Program execution starts at the address formed by setting address A_{23} – A_{16} to 00_{16}, A_{15} – A_8 to the contents of address $FFFF_{16}$, and A_7 – A_0 to the contents of address $FFFE_{16}$.
Figure 13 shows an example of a reset circuit. If the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. If a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.
Figure 12 shows the status of the internal registers during reset.

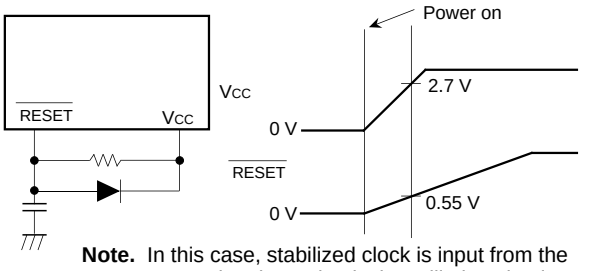
	Address	
Port P0 direction register	(04_{16})•••	00_{16}
Port P1 direction register	(05_{16})•••	00_{16}
Port P2 direction register	(08_{16})•••	00_{16}
Port P3 direction register	(09_{16})•••	X X X X 0 0 0 0
Port P4 direction register	($0C_{16}$)•••	00_{16}
Port P5 direction register	($0D_{16}$)•••	00_{16}
Port P6 direction register	(10_{16})•••	00_{16}
Port P7 direction register	(11_{16})•••	00_{16}
Port P8 direction register	(14_{16})•••	00_{16}
A-D control register 0	($1E_{16}$)•••	0 0 0 0 0 ? ? ?
A-D control register 1	($1F_{16}$)•••	X X 0 0 0 X 1 1
UART 0 transmit/receive mode register	(30_{16})•••	00_{16}
UART 1 transmit/receive mode register	(38_{16})•••	00_{16}
UART 0 transmit/receive control register 0	(34_{16})•••	0 0 0 0 1 0 0 0
UART 1 transmit/receive control register 0	($3C_{16}$)•••	0 0 0 0 1 0 0 0
UART 0 transmit/receive control register 1	(35_{16})•••	0 0 0 0 0 0 1 0
UART 1 transmit/receive control register 1	($3D_{16}$)•••	0 0 0 0 0 0 1 0
Count start flag	(40_{16})•••	00_{16}
One- shot start flag	(42_{16})•••	X X X 0 0 0 0 0
Up-down flag	(44_{16})•••	00_{16}
Timer A0 mode register	(56_{16})•••	00_{16}
Timer A1 mode register	(57_{16})•••	00_{16}
Timer A2 mode register	(58_{16})•••	00_{16}
Timer A3 mode register	(59_{16})•••	00_{16}
Timer A4 mode register	($5A_{16}$)•••	00_{16}
Timer B0 mode register	($5B_{16}$)•••	0 0 1 0 0 0 0 0
Timer B1 mode register	($5C_{16}$)•••	0 0 1 X 0 0 0 0
Timer B2 mode register	($5D_{16}$)•••	0 0 1 X 0 0 0 0
Processor mode register 0	($5E_{16}$)•••	00_{16}
Processor mode register 1	($5F_{16}$)•••	X X X X X X X 0
Watchdog timer register	(60_{16})•••	FFF_{16}

	Address	
Watchdog timer frequency selection flag	(61_{16})•••	X X X X X X X 0
Waveform output mode register	(62_{16})•••	0 X 0 0 0 X 0 0
UART2 transmit/receive mode register	(64_{16})•••	X 0 0 0 0 0 0 0
UART2 transmit/receive control register 0	(68_{16})•••	X X X X 1 0 0 0
UART2 transmit/receive control register 1	(69_{16})•••	0 0 0 0 0 0 1 0
Oscillation circuit control register 0	($6C_{16}$)•••	X 0 0 0 0 0 X 1
Port function control register	($6D_{16}$)•••	00_{16}
Serial transmit control register	($6E_{16}$)•••	X X 0 0 X X X X
Oscillation circuit control register 1	($6F_{16}$)•••	0 X X 0 0 0 0 0
A-D/UART2 trans./rece. interrupt control register	(70_{16})•••	X X X X 0 0 0 0
UART 0 transmission interrupt control register	(71_{16})•••	X X X X 0 0 0 0
UART 0 receive interruupt control register	(72_{16})•••	X X X X 0 0 0 0
UART 1 transmission interrupt control register	(73_{16})•••	X X X X 0 0 0 0
UART 1 receive interruupt control register	(74_{16})•••	X X X X 0 0 0 0
Timer A0 interrupt control register	(75_{16})•••	X X X X 0 0 0 0
Timer A1 interrupt control register	(76_{16})•••	X X X X 0 0 0 0
Timer A2 interrupt control register	(77_{16})•••	X X X X 0 0 0 0
Timer A3 interrupt control register	(78_{16})•••	X X X X 0 0 0 0
Timer A4 interrupt control register	(79_{16})•••	X X X X 0 0 0 0
Timer B0 interrupt control register	($7A_{16}$)•••	X X X X 0 0 0 0
Timer B1 interrupt control register	($7B_{16}$)•••	X X X X 0 0 0 0
Timer B2 interrupt control register	($7C_{16}$)•••	X X X X 0 0 0 0
$\overline{\text{INT}_0}$ interrupt control register	($7D_{16}$)•••	X X 0 0 0 0 0 0
$\overline{\text{INT}_1}$ interrupt control register	($7E_{16}$)•••	X X 0 0 0 0 0 0
$\overline{\text{INT}_2}$/key input interrupt control register	($7F_{16}$)•••	X X 0 0 0 0 0 0
Processor status register (PS)		0 0 0 ? ? 0 0 0 1 ? ?
Program bank register (PG)		00_{16}
Program counter (PC_H)		Content of $FFFF_{16}$
Program counter (PC_L)		Content of $FFFE_{16}$
Direct page register (DPR)		0000_{16}
Data bank register (DT)		00_{16}

Contents of other registers and RAM are undefined during reset. Initialize them by software.

Fig. 12 Microcomputer internal status during reset

New product



Note. In this case, stabilized clock is input from the external to the main-clock oscillation circuit. Perform careful evaluation at the system design level before using.

Fig. 13 Example of a reset circuit

ADDRESSING MODES

The M37735S4LHP has 28 powerful addressing modes.Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37735S4LHP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Power source voltage		–0.3 to +7	V
AVcc	Analog power source voltage		–0.3 to +7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		–0.3 to +12	V
V_I	Input voltage $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$, $P4_3$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, V_{REF}, X_{IN}, $\overline{HOLD}$, $\overline{RDY}$		–0.3 to Vcc + 0.3	V
V_O	Output voltage $P0_0/\overline{CS_0}$ – $P0_7/A_{17}$, $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$, $P3_0/\overline{WEL}$ – $P3_3/\overline{HLDA}$, $P4_2/\phi_1$, $P4_3$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{OUT}, $\overline{RDE}$		–0.3 to Vcc + 0.3	V
P_d	Power dissipation	Ta = 25 °C	200	mW
T_{opr}	Operating temperature		–40 to +85	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (Vcc = 2.7 – 5.5 V, Ta = –40 to +85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
Vcc	Power source voltage	f(X_{IN}) : Operating	2.7		5.5	V
		f(X_{IN}) : Stopped, f(X_{CIN}) = 32.768 kHz	2.7		5.5	
AVcc	Analog power source voltage			Vcc		V
Vss	Power source voltage			0		V
AVss	Analog power source voltage			0		V
V_{IH}	High-level input voltage $\overline{HOLD}$, $\overline{RDY}$, $P4_3$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} (Note 3)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$		0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage $\overline{HOLD}$, $\overline{RDY}$, $P4_3$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$, X_{IN}, $\overline{RESET}$, CNVss, BYTE, X_{CIN} (Note 3)		0		0.2Vcc	V
V_{IL}	Low-level input voltage $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$		0		0.16Vcc	V
$I_{OH(peak)}$	High-level peak output current $P0_0/\overline{CS_0}$ – $P0_7/A_{17}$, $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$, $P3_0/\overline{WEL}$ – $P3_3/\overline{HLDA}$, $P4_2/\phi_1$, $P4_3$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				–10	mA
$I_{OH(avg)}$	High-level average output current $P0_0/\overline{CS_0}$ – $P0_7/A_{17}$, $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$, $P3_0/\overline{WEL}$ – $P3_3/\overline{HLDA}$, $P4_2/\phi_1$, $P4_3$ – $P4_7$, $P5_0$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				–5	mA
$I_{OL(peak)}$	Low-level peak output current $P0_0/\overline{CS_0}$ – $P0_7/A_{17}$, $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$, $P3_0/\overline{WEL}$ – $P3_3/\overline{HLDA}$, $P4_2/\phi_1$, $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				10	mA
$I_{OL(peak)}$	Low-level peak output current $P4_4$ – $P4_7$, $P5_0$ – $P5_3$				16	mA
$I_{OL(avg)}$	Low-level average output current $P0_0/\overline{CS_0}$ – $P0_7/A_{17}$, $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$, $P3_0/\overline{WEL}$ – $P3_3/\overline{HLDA}$, $P4_2/\phi_1$, $P4_3$, $P5_4$ – $P5_7$, $P6_0$ – $P6_7$, $P7_0$ – $P7_7$, $P8_0$ – $P8_7$				5	mA
$I_{OL(avg)}$	Low-level average output current $P4_4$ – $P4_7$, $P5_0$ – $P5_3$				12	mA
f(X_{IN})	Main-clock oscillation frequency (Note 4)				12	MHz
f(X_{CIN})	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

2. The sum of $I_{OL(peak)}$ for ports $P0_0/\overline{CS_0}$ – $P0_7/A_{17}$, $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$, $P3_0/\overline{WEL}$ – $P3_3/\overline{HLDA}$ and P8 must be 80 mA or less, the sum of $I_{OH(peak)}$ for ports $P0_0/\overline{CS_0}$ – $P0_7/A_{17}$, $P1_0/A_8/D_8$ – $P1_7/A_{15}/D_{15}$, $P2_0/A_0/D_0$ – $P2_7/A_7/D_7$, $P3_0/\overline{WEL}$ – $P3_3/\overline{HLDA}$ and P8 must be 80 mA or less, the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80 mA or less.

3. Limits V_{IH} and V_{IL} for X_{CIN} are applied when the sub clock external input selection bit = "1".

4. The maximum value of f(X_{IN}) = 6 MHz when the main clock division selection bit = "1".

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –40 to +85 °C, f(XIN) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
VOH	High-level output voltage P00/CS0 – P07/A17, P10/A8/D8 – P17/A15/D15, P20/A0/D0 – P27/A7/D7, P33/HLDA, P42/ φ 1, P43 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87	VCC = 5 V, IOH = –10 mA	3			V
		VCC = 3 V, IOH = –1 mA	2.5			
VOH	High-level output voltage P00/CS0 – P07/A17, P10/A8/D8 – P17/A15/D15, P20/A0/D0 – P27/A7/D7, P33/HLDA, P42/ φ 1	VCC = 5 V, IOH = –400 μA	4.7			V
VOH	High-level output voltage P30/WEL, P31/WEH, P32/ALE	VCC = 5 V, IOH = –10 mA	3.1			V
		VCC = 5 V, IOH = –400 μA	4.8			
		VCC = 3 V, IOH = –1 mA	2.6			
VOH	High-level output voltage RDE	VCC = 5 V, IOH = –10 mA	3.4			V
		VCC = 5 V, IOH = –400 μA	4.8			
		VCC = 3 V, IOH = –1 mA	2.6			
VOL	Low-level output voltage P00/CS0 – P07/A17, P10/A8/D8 – P17/A15/D15, P20/A0/D0 – P27/A7/D7, P33/HLDA, P42/ φ 1, P43, P54 – P57, P60 – P67, P70 – P77, P80 – P87	VCC = 5 V, IOL = 10 mA			2	V
		VCC = 3 V, IOL = 1 mA			0.5	
VOL	Low-level output voltage P44 – P47, P50 – P53	VCC = 5 V, IOL = 16 mA			1.8	V
		VCC = 3 V, IOL = 10 mA			1.5	
VOL	Low-level output voltage P00/CS0 – P07/A17, P10/A8/D8 – P17/A15/D15, P20/A0/D0 – P27/A7/D7, P33/HLDA, P42/ φ 1	VCC = 5 V, IOL = 2 mA			0.45	V
VOL	Low-level output voltage P30/WEL, P31/WEH, P32/ALE	VCC = 5 V, IOL = 10 mA			1.9	V
		VCC = 5 V, IOL = 2 mA			0.43	
		VCC = 3 V, IOL = 1 mA			0.4	
VOL	Low-level output voltage RDE	VCC = 5 V, IOL = 10 mA			1.6	V
		VCC = 5 V, IOL = 2 mA			0.4	
		VCC = 3 V, IOL = 1 mA			0.4	
VT+ – VT–	Hysteresis HOLD, RDY, TA0IN – TA4IN, TB0IN – TB2IN, INT0 – INT2, ADTRG, CTS0, CTS1, CTS2, CLK0, CLK1, CLK2, KI0 – KI3	VCC = 5 V	0.4		1	V
		VCC = 3 V	0.1		0.7	
VT+ – VT–	Hysteresis RESET	VCC = 5 V	0.2		0.5	V
		VCC = 3 V	0.1		0.4	
VT+ – VT–	Hysteresis XIN	VCC = 5 V	0.1		0.4	V
		VCC = 3 V	0.06		0.26	
VT+ – VT–	Hysteresis XCIN (When external clock is input)	VCC = 5 V	0.1		0.4	V
		VCC = 3 V	0.06		0.26	
IIH	High-level input current P10/A8/D8 – P17/A15/D15, P20/A0/D0 – P27/A7/D7, P43 – P47, P50 – P57, P60 – P67, P70 – P77, P80 – P87, XIN, RESET, CNVss, BYTE	VCC = 5 V, VI = 5 V			5	μA
		VCC = 3 V, VI = 3 V			4	
IIL	Low-level input current P10/A8/D8 – P17/A15/D15, P20/A0/D0 – P27/A7/D7, P43 – P47, P50 – P53, P60, P61, P65 – P67, P70 – P77, P80 – P87, XIN, RESET, CNVss, BYTE	VCC = 5 V, VI = 0 V			–5	μA
		VCC = 3 V, VI = 0 V			–4	
IIL	Low-level input current P54 – P57, P62 – P64	VI = 0 V, without a pull-up transistor, VCC = 5 V			–5	μA
		VI = 0 V, without a pull-up transistor, VCC = 3 V			–4	
		VI = 0 V, with a pull-up transistor, VCC = 5 V	–0.25	–0.5	–1.0	mA
		VI = 0 V, with a pull-up transistor, VCC = 3 V	–0.08	–0.18	–0.35	
VRAM	RAM hold voltage	When clock is stopped.	2			V

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –40 to +85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	When external bus is in use, output pins are open, and other pins are V_{SS}.	V_{CC} = 5 V, $f(X_{IN})$ = 12 MHz (square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating (Note 1)		5.4	10.8	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), ($f(f_2)$ = 6 MHz), $f(X_{CIN})$ = 32.768 kHz, in operating (Note 1)		3.6	7.2	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), ($f(f_2)$ = 0.75 MHz), $f(X_{CIN})$: Stopped, in operating		0.5	1.0	mA
			V_{CC} = 3 V, $f(X_{IN})$ = 12 MHz (square waveform), $f(X_{CIN})$ = 32.768 kHz, when a WIT instruction is executed (Note 2)		6	12	µ A
			V_{CC} = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$ = 32.768 kHz, in operating (Note 3)		40	80	µ A
			V_{CC} = 3 V, $f(X_{IN})$: Stopped, $f(X_{CIN})$ = 32.768 kHz, when a WIT instruction is executed (Note 4)		3	6	µ A
			Ta = 25 °C, when clock is stopped			1	µ A
			Ta = 85 °C, when clock is stopped			20	µ A

Notes 1. This applies when the main clock external input selection bit = “1”, the main clock division selection bit = “0”, and the signal output stop bit = “1”.
2. This applies when the main clock external input selection bit = “1” and the system clock stop bit at wait state = “1”.
3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.
4. This applies when the X_{COUT} drivability selection bit = “0” and the system clock stop bit at wait state = “1”.

A–D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5 V, V_{SS} = AV_{SS} = 0 V, Ta = –40 to +85 °C, $f(X_{IN})$ = 12 MHz, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}			10	Bits
—	Absolute accuracy	V_{REF} = V_{CC}			± 3	LSB
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}	10		25	kΩ
t_{CONV}	Conversion time		19.6			µ s
V_{REF}	Reference voltage		2.7		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

Note. This applies when the main clock division selection bit = “0” and $f(f_2)$ = 6 MHz.

TIMING REQUIREMENTS (V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note 1))

Notes 1. This applies when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 1)	83		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 2)	33		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 2)	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Notes 1. When the main clock division selection bit = "1", the minimum value of t_c = 166 ns.

2. When the main clock division selection bit = "1", values of $t_{w(H)}$ / t_c and $t_{w(L)}$ / t_c must be set to values from 0.45 through 0.55.

Microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P4D–RDE)}$	Port P4 input setup time	200		ns
$t_{su(P5D–RDE)}$	Port P5 input setup time	200		ns
$t_{su(P6D–RDE)}$	Port P6 input setup time	200		ns
$t_{su(P7D–RDE)}$	Port P7 input setup time	200		ns
$t_{su(P8D–RDE)}$	Port P8 input setup time	200		ns
$t_{h(RDE–P4D)}$	Port P4 input hold time	0		ns
$t_{h(RDE–P5D)}$	Port P5 input hold time	0		ns
$t_{h(RDE–P6D)}$	Port P6 input hold time	0		ns
$t_{h(RDE–P7D)}$	Port P7 input hold time	0		ns
$t_{h(RDE–P8D)}$	Port P8 input hold time	0		ns
$t_{su(D–RDE)}$	Data input setup time	80		ns
$t_{su(RDY–\phi 1)}$	$\overline{RDY}$ input setup time	80		ns
$t_{su(HOLD–\phi 1)}$	$\overline{HOLD}$ input setup time	80		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns
$t_{h(\phi 1–RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi 1–HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time	250		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	125		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time (Note)	666		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width (Note)	333		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} input cycle time (Note)	333		ns
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	166		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	166		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS".

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} input high-level pulse width	166		ns
$t_{w(TAL)}$	TAi_{IN} input low-level pulse width	166		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} input cycle time	3333		ns
$t_{w(UPH)}$	TAi_{OUT} input high-level pulse width	1666		ns
$t_{w(UPL)}$	TAi_{OUT} input low-level pulse width	1666		ns
$t_{su(UP-TIN)}$	TAi_{OUT} input setup time	666		ns
$t_{h(TIN-UP)}$	TAi_{OUT} input hold time	666		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAj_{IN} input cycle time	2000		ns
$t_{su(TAjIN-TAjOUT)}$	TAj_{IN} input setup time	500		ns
$t_{su(TAjOUT-TAjIN)}$	TAj_{OUT} input setup time	500		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (one edge count)	250		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (one edge count)	125		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (one edge count)	125		ns
$t_{c(TB)}$	TBi_{IN} input cycle time (both edges count)	500		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (both edges count)	250		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (Note)	666		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (Note)	333		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to “DATA FORMULAS”.

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} input cycle time (Note)	666		ns
$t_{w(TBH)}$	TBi_{IN} input high-level pulse width (Note)	333		ns
$t_{w(TBL)}$	TBi_{IN} input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to “DATA FORMULAS”.

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (minimum allowable trigger)	1333		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low-level pulse width	166		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLK_i input cycle time	333		ns
$t_{w(CKH)}$	CLK_i input high-level pulse width	166		ns
$t_{w(CKL)}$	CLK_i input low-level pulse width	166		ns
$t_{d(C-Q)}$	TxD_i output delay time		100	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	65		ns
$t_{h(C-D)}$	RxD_i input hold time	75		ns

External interrupt $\overline{INT_i}$ input, key input interrupt $\overline{KI_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns
$t_{w(KIL)}$	$\overline{KI_i}$ input low-level pulse width	250		ns

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	$\frac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width	$\frac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. f(f_2) represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37735MHBXXXFP”.

SWITCHING CHARACTERISTICS

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85°C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note))

Microprocessor mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(WE-P4Q)}$	Port P4 data output delay time	Fig. 14		300	ns
$t_{d(WE-P5Q)}$	Port P5 data output delay time			300	ns
$t_{d(WE-P6Q)}$	Port P6 data output delay time			300	ns
$t_{d(WE-P7Q)}$	Port P7 data output delay time			300	ns
$t_{d(WE-P8Q)}$	Port P8 data output delay time			300	ns

Note. This applies when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

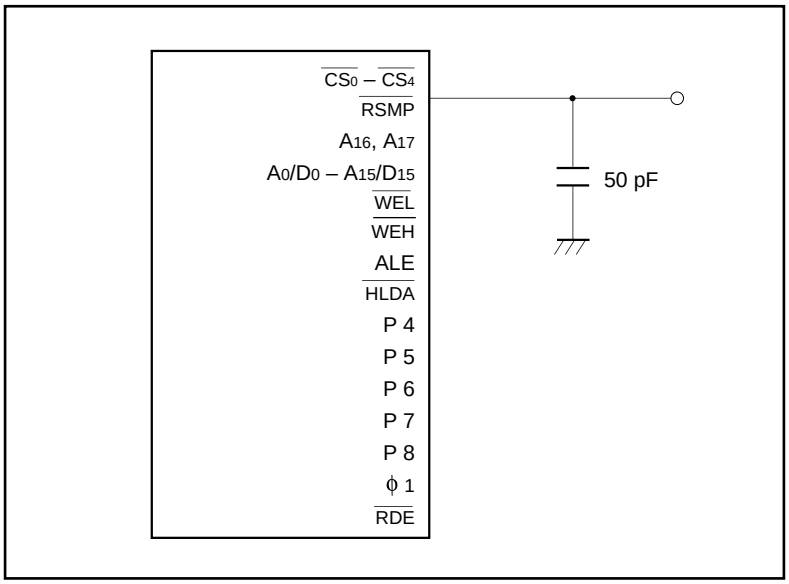


Fig. 14 Measuring circuit for each pin

Microprocessor mode

(V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note 1))

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits Min.	Limits Max.	Unit
$t_{d(CS–WE)}$ $t_{d(CS–RDE)}$	Chip-select output delay time	No wait Wait 1	Fig. 14	20		ns
		Wait 0		182		ns
$t_{h(WE–CS)}$ $t_{h(RDE–CS)}$	Chip-select hold time			4		ns
$t_{d(An–WE)}$ $t_{d(An–RDE)}$	Address output delay time	No wait Wait 1		20		ns
		Wait 0		182		ns
$t_{d(A–WE)}$ $t_{d(A–RDE)}$	Address output delay time	No wait Wait 1		20		ns
		Wait 0		162		ns
$t_{h(WE–An)}$ $t_{h(RDE–An)}$	Address hold time			40		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1		40		ns
		Wait 0		123		ns
$t_{su(A–ALE)}$	Address output setup time	No wait Wait 1		10		ns
		Wait 0		93		ns
$t_{h(ALE–A)}$	Address hold time	No wait Wait 1		9		ns
		Wait 0		40		ns
$t_{d(ALE–WE)}$ $t_{d(ALE–RDE)}$	ALE output delay time	No wait Wait 1		4		ns
		Wait 0		40		ns
$t_{d(WE–DQ)}$	Data output delay time				90	ns
$t_{h(WE–DQ)}$	Data hold time			40		ns
$t_{w(WE)}$	$\overline{WEL}$/$\overline{WEH}$ pulse width	No wait		131		ns
		Wait 1 Wait 0		298		ns
$t_{pxz(RDE–DZ)}$	Floating start delay time				10	ns
$t_{pzx(RDE–DZ)}$	Floating release delay time			53		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait		128		ns
		Wait 1 Wait 0		295		ns
$t_{d(RSMP–WE)}$ $t_{d(RSMP–RDE)}$	$\overline{RSMP}$ output delay time			25		ns
$t_{h(\phi 1–RSMP)}$	$\overline{RSMP}$ hold time			0		ns
$t_{d(WE–\phi 1)}$ $t_{d(RDE–\phi 1)}$	ϕ_1 output delay time			0	30	ns
$t_{d(\phi 1–HLDA)}$	$\overline{HLDA}$ output delay time				120	ns

Notes 1. This applies when the main clock division selection bit = “0” and f(f_2) = 6 MHz.

2. No wait : Wait bit = “1”.
Wait 1 : The external memory area is accessed with wait bit = “0” and wait selection bit = “1”.
Wait 0 : The external memory area is accessed with wait bit = “0” and wait selection bit = “0”.

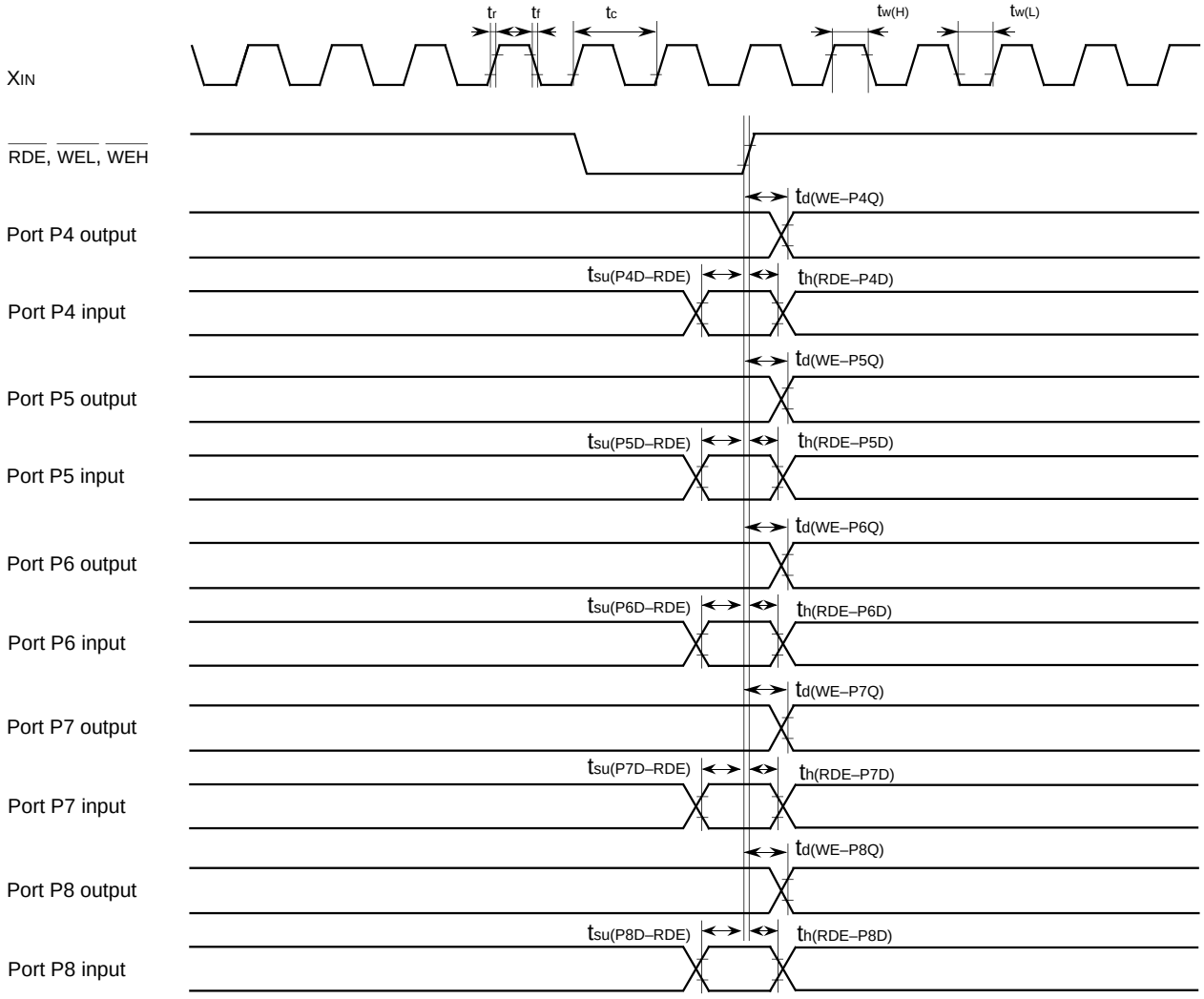
Bus timing data formulas (V_{CC} = 2.7 – 5.5V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz (Max.), unless otherwise noted (Note1))

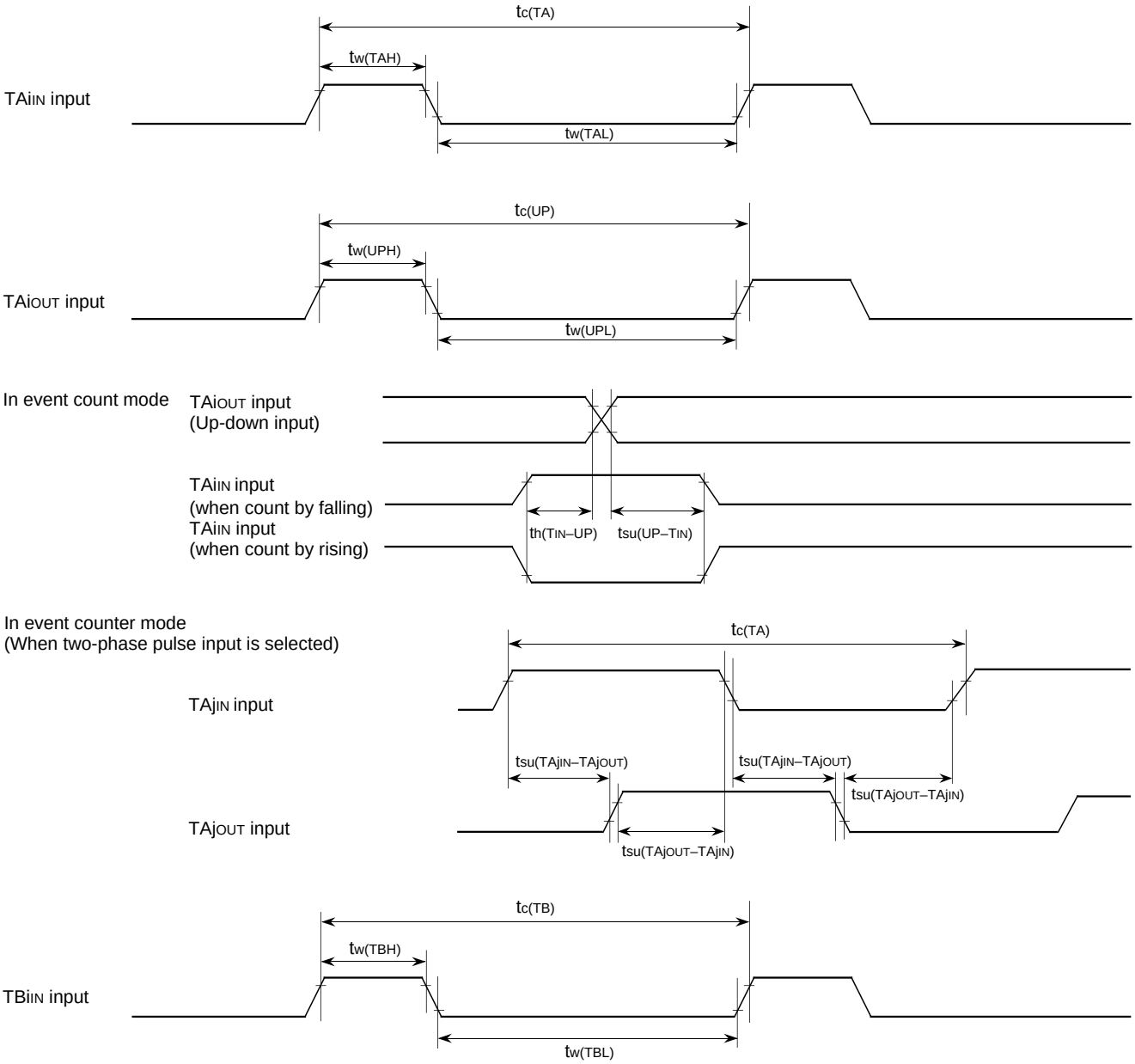
Symbol	Parameter	Wait mode	Limits Min.	Limits Max.	Unit
$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$	Chip-select output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$	Chip-select hold time		4		ns
$t_{d(An-WE)}$ $t_{d(An-RDE)}$	Address output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{d(A-WE)}$ $t_{d(A-RDE)}$	Address output delay time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\frac{3 \times 10^9}{2 \cdot f(f_2)} - 88$		ns
$t_{h(WE-An)}$ $t_{h(RDE-An)}$	Address hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{su(A-ALE)}$	Address output setup time	No wait Wait 1	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
		Wait 0	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
$t_{h(ALE-A)}$	Address hold time	No wait Wait 1	9		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{d(ALE-WE)}$ $t_{d(ALE-RDE)}$	ALE output delay time	No wait Wait 1	4		ns
		Wait 0	$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{d(WE-DQ)}$	Data output delay time			90	ns
$t_{h(WE-DQ)}$	Data hold time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{w(WE)}$	$\overline{WEL}$/$\overline{WEH}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1 Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
$t_{pxz(RDE-DZ)}$	Floating start delay time			10	ns
$t_{pzx(RDE-DZ)}$	Floating release delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait	$\frac{2 \times 10^9}{2 \cdot f(f_2)} - 38$		ns
		Wait 1 Wait 0	$\frac{4 \times 10^9}{2 \cdot f(f_2)} - 38$		ns
$t_{d(RSMP-WE)}$ $t_{d(RSMP-RDE)}$	$\overline{RSMP}$ output delay time		$\frac{1 \times 10^9}{2 \cdot f(f_2)} - 58$		ns
$t_{h(\phi 1-RSMP)}$	$\overline{RSMP}$ hold time		0		ns
$t_{d(WE-\phi 1)}$ $t_{d(RDE-\phi 1)}$	ϕ 1 output delay time		0	30	ns

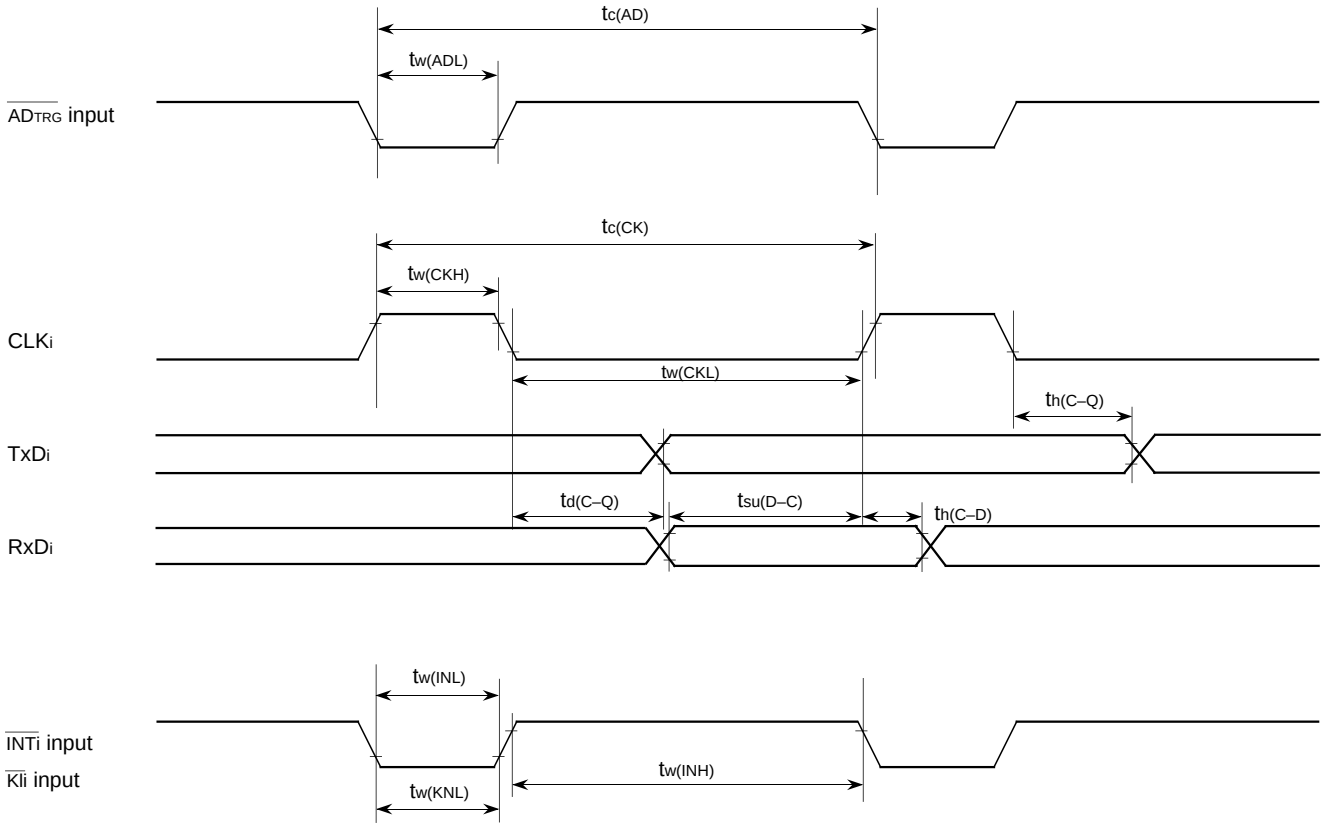
Notes 1. This applies when the main clock division selection bit = “0”.

2. f(f_2) represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet “M37735MHBXXXFP”.

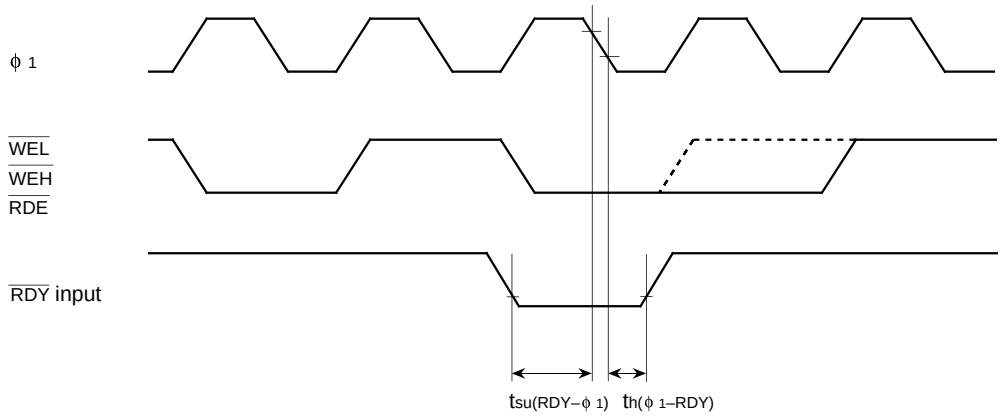
TIMING DIAGRAM



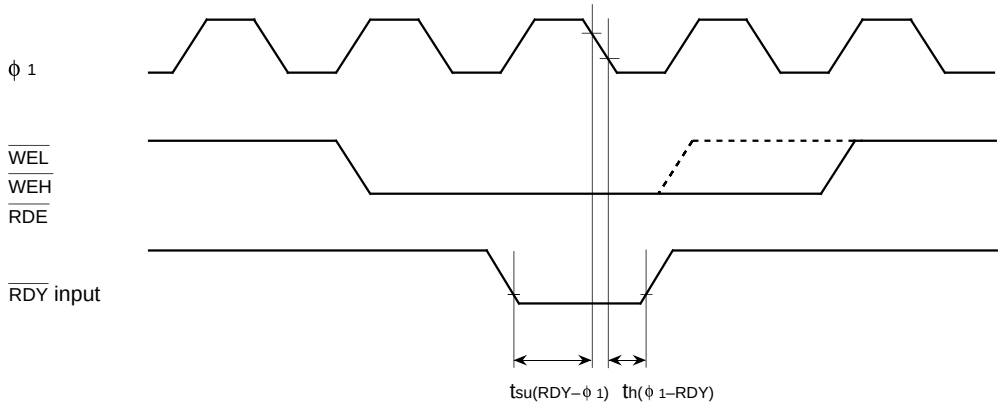

tc(TA)
tw(TAH)
TAiIN input
tw(TAL)
tc(UP)
tw(UPH)
TAiOUT input
tw(UPL)
In event count mode
TAiOUT input
(Up-down input)
TAiIN input
(when count by falling)
TAiIN input
(when count by rising)
th(TIN–UP)
tsu(UP–TIN)
In event counter mode
(When two-phase pulse input is selected)
tc(TA)
TAjIN input
tsu(TAjIN–TAjOUT)
tsu(TAjIN–TAjOUT)
tsu(TAjOUT–TAjIN)
TAjOUT input
tsu(TAjOUT–TAjIN)
tc(TB)
tw(TBH)
TBiIN input
tw(TBL)


tc(AD)
tw(ADL)
ADTRG input
tc(CK)
tw(CKH)
CLKi
tw(CKL)
th(C–Q)
TxDi
td(C–Q)
tsu(D–C)
th(C–D)
RxDi
tw(INL)
INTi input
tw(INH)
Kli input
tw(KNL)

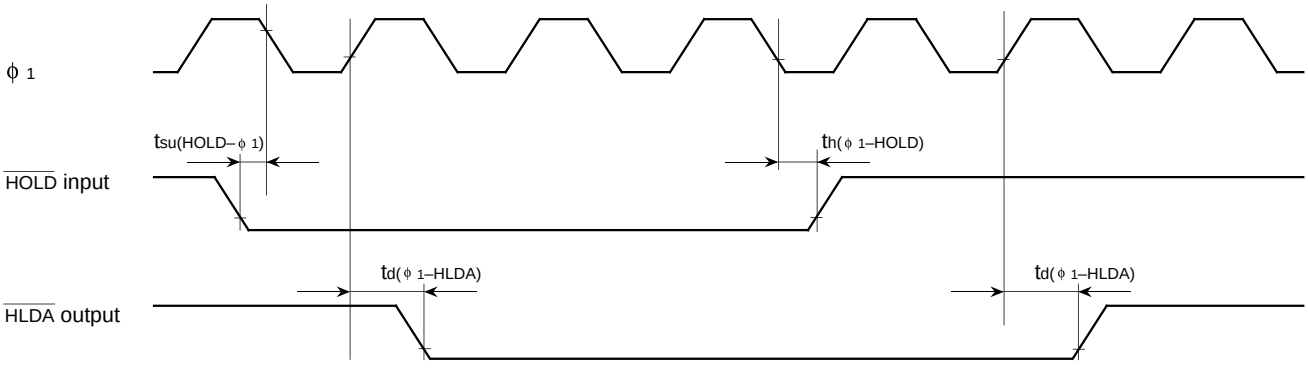
Microprocessor mode
(When wait bit = “1”)



(When wait bit = “0”)

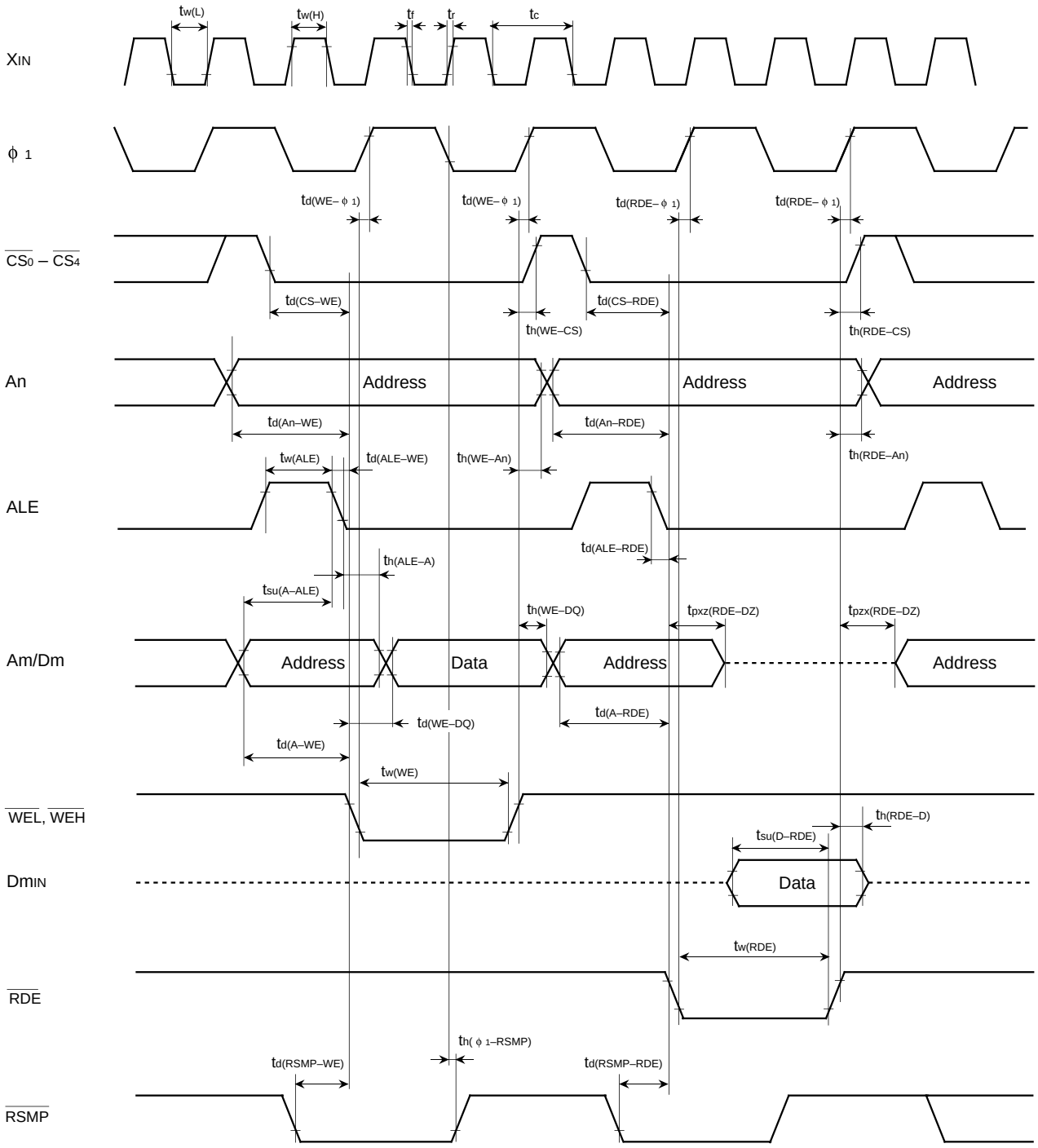


(When wait bit = “1” or “0” in common)



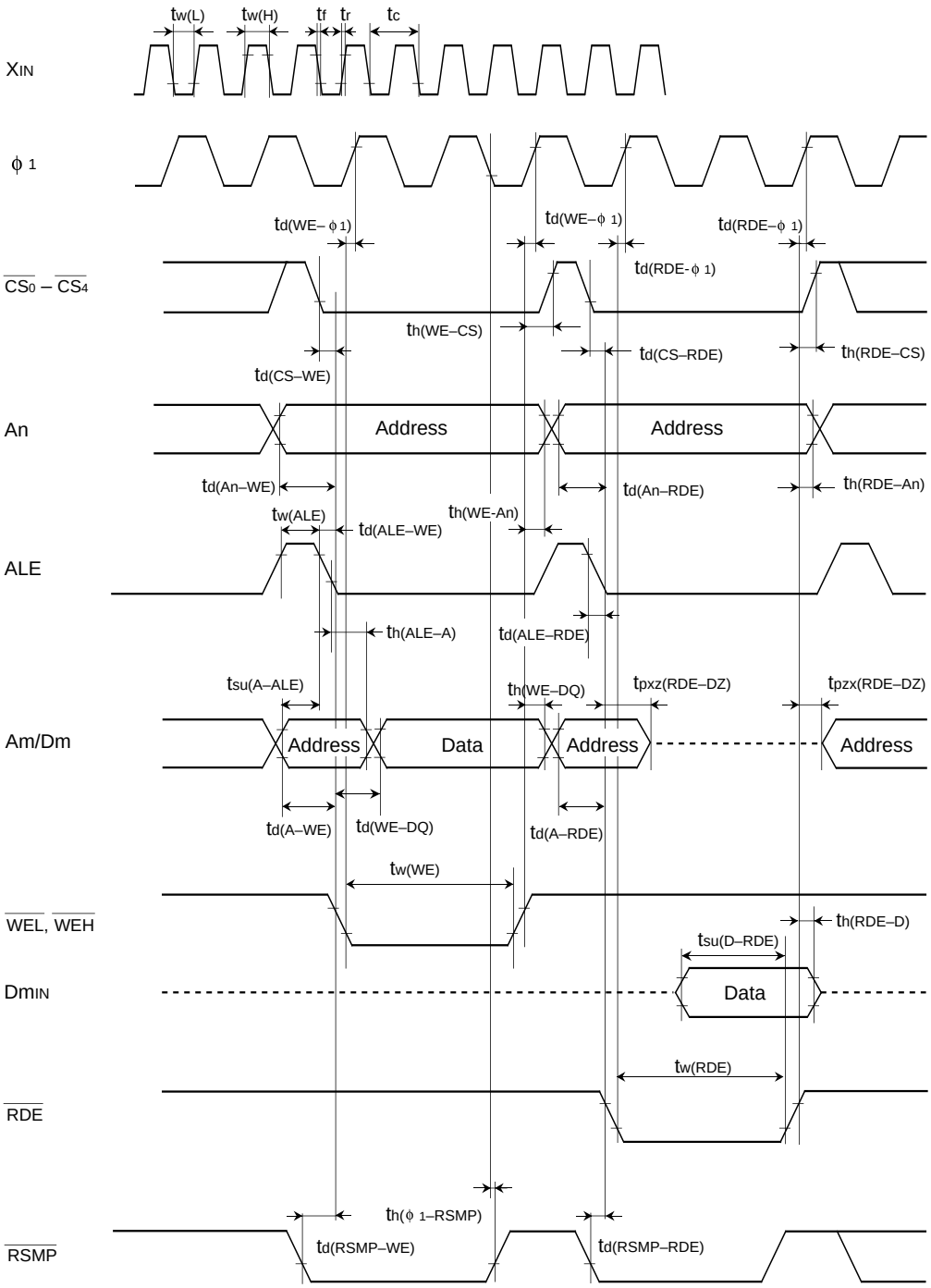
Test conditions
- V_{CC} = 2.7 – 5.5 V
- Input timing voltage : V_{IL} = 0.2V_{CC}, V_{IH} = 0.8V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

Microprocessor mode
(No wait : When wait bit = “1”)



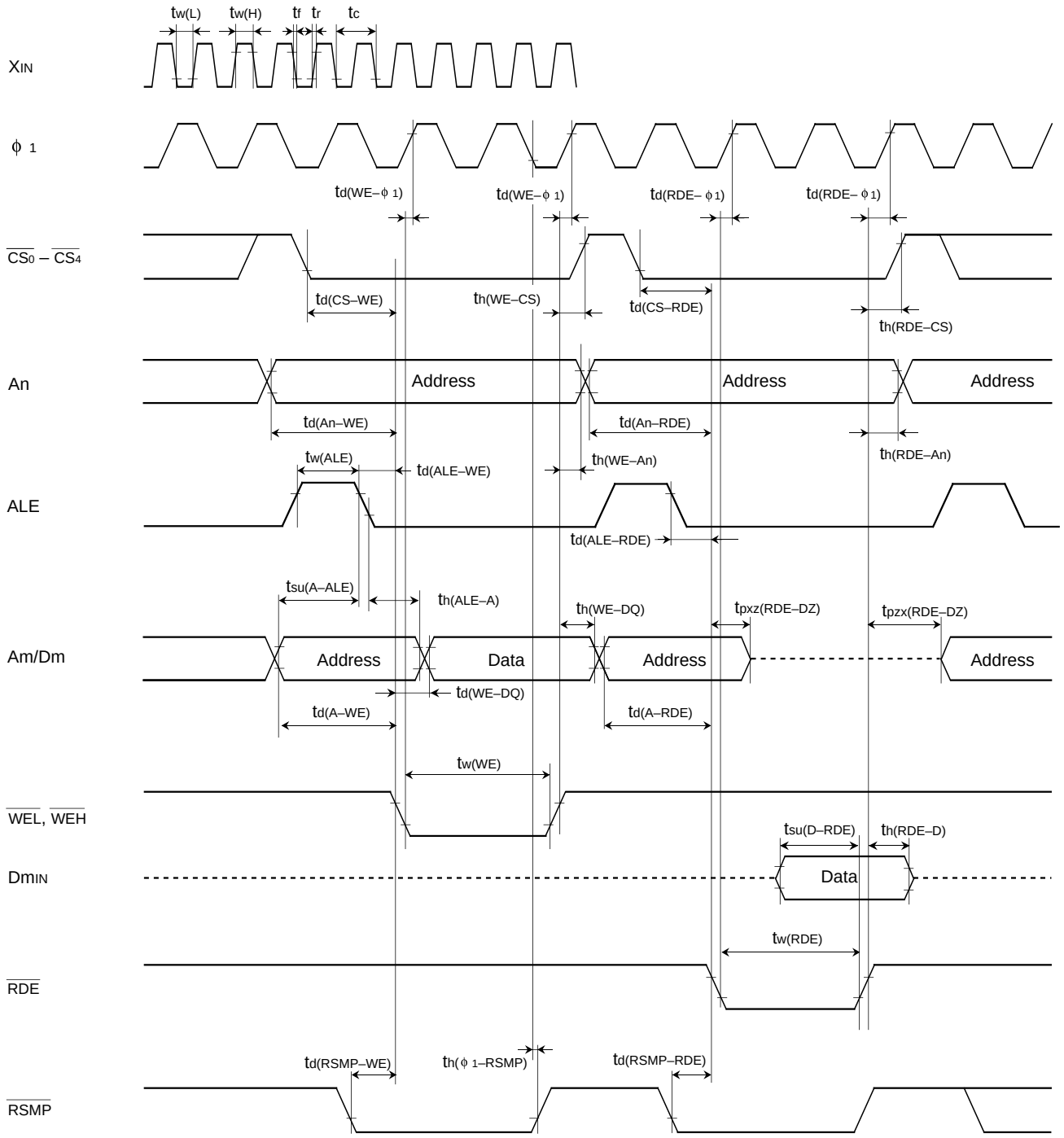
Test conditions
• Vcc = 2.7 – 5.5 V
• Output timing voltage : VOL = 0.8 V, VOL = 2.0 V
• Data input DmIN : VIL = 0.16 Vcc, VIH = 0.5 Vcc

Microprocessor mode
(Wait 1 : The external area is accessed when wait bit = “0” and wait selection bit = “1”.)



Test conditions
• Vcc = 2.7 – 5.5 V
• Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
• Data input DmIN : VIL = 0.16 Vcc, VIH = 0.5 Vcc

Microprocessor mode
(Wait 0 : The external memory area is accessed when wait bit = “0” and wait selection bit = “0”.)



Test conditions
• Vcc = 2.7 – 5.5 V
• Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
• Data input DmIN : VIL = 0.16 Vcc, VIH = 0.5 Vcc

New product

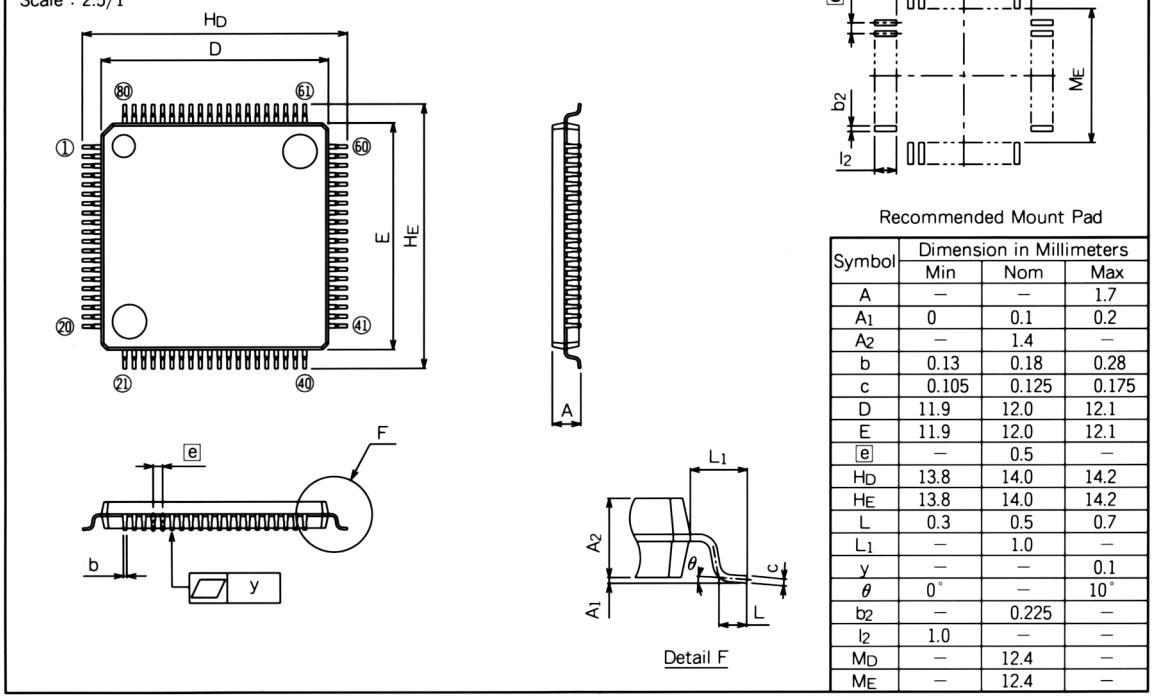
PACKAGE OUTLINE

80P6D−A

Plastic 80pin 12×12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.50	—	0.44	Alloy 42

Scale : 2.5/1



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	—	0.5	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	—	1.0	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.225	—
l_2	1.0	—	—
M_D	—	12.4	—
M_E	—	12.4	—

MEMO

M37735S4LHP

New product

16-BIT CMOS MICROCOMPUTER

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