TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

32,768-WORD BY 8-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V328BJ/BFT is a 262,144-bit high-speed static random access memory (SRAM) organized as 32,768 words by 8 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed and low-voltage operation, it operates from a single 3.3 V power supply. There are two control inputs. Chip enable ($\overline{CE}$) can be used to place the device in a low-power mode, and output enable ($\overline{OE}$) provides fast memory access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55V328BJ/BFT is available in plastic 28-pin SOJ (300 mil width) and TSOP packages for high density surface assembly.

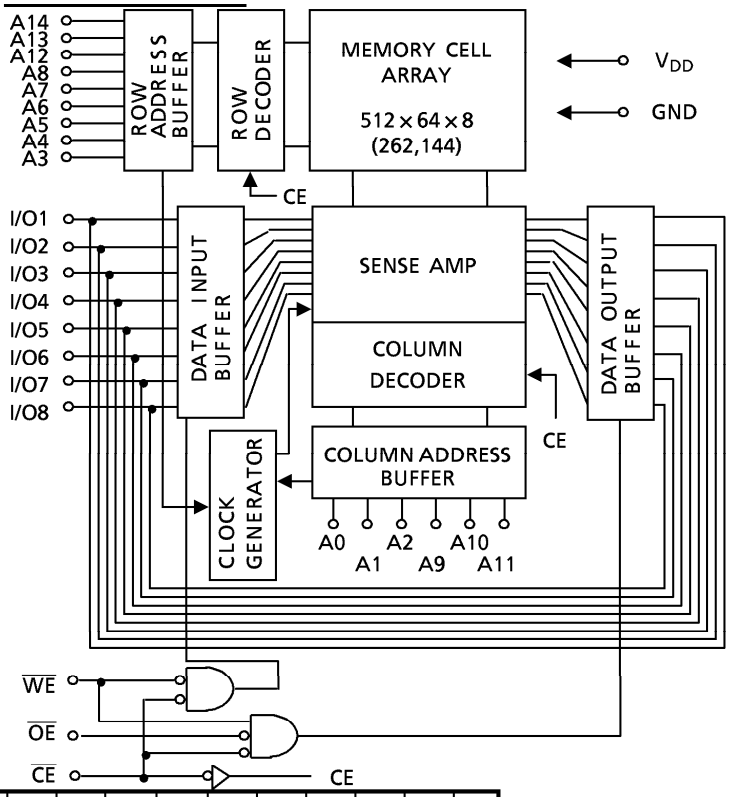
FEATURES

- Fast access time (the following are maximum values)
  TC55V328BJ/BFT-12: 12 ns
  TC55V328BJ/BFT-15: 15 ns
- Low-power dissipation
  (the following are maximum values)
  Operating: 120 mA (12 ns type)
  Operating: 100 mA (15 ns type)
  Standby : 300 μA (all devices)
- Single power supply voltage:
  TC55V328BJ/BFT-12 : 3.3V + 0.3V or -0.2V
  TC55V328BJ/BFT-15 : 3.3V $\pm$ 0.3V
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using $\overline{OE}$
- Packages:
  SOJ28-P-300-1.27A (BJ) (Weight: 0.83 g typ)
  TSOP I 28-P-0.55 (BFT) (Weight: 0.22 g typ)

PIN ASSIGNMENT

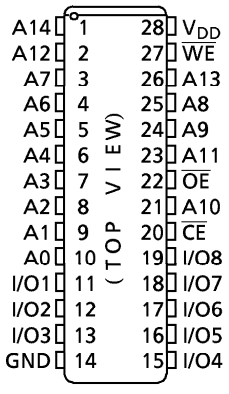
A0 to A14	Address Inputs
I/O1 to I/O8	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+ 3.3V)
GND	Ground

BLOCK DIAGRAM



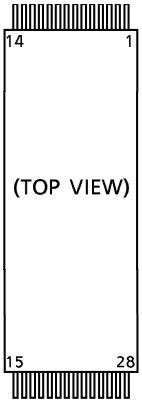
PIN CONNECTION

TC55V328BJ



(SOJ)

TC55V328BFT



(TSOP)

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Pin Name	$\overline{OE}$	A_{11}	A_9	A_8	A_{13}	$\overline{WE}$	V_{DD}	A_{14}	A_{12}	A_7	A_6	A_5	A_4	A_3
Pin No.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Pin Name	A_2	A_1	A_0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A_{10}

961001EBA1

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	– 0.5 to 4.6	V
V_{IN}	Input Voltage	– 0.5* to 4.6	V
$V_{I/O}$	Input/Output Voltage	– 0.5* to V_{DD} + 0.5**	V
P_D	Power Dissipation	0.5	W
T_{solder}	Soldering Temperature (10 s)	260	°C
T_{strg}	Storage Temperature	– 65 to 150	°C
T_{opr}	Operating Temperature	– 10 to 85	°C

*: – 1.5V with a pulse width of 20% of t_{RC} (4ns max.)
**: V_{DD} + 1.5V with a pulse width of 20% of t_{RC} (4ns max.)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	-12	3.1	3.3	3.6	V
		-15	3.0	3.3	3.6	
V_{IH}	Input High Voltage		2.0	–	V_{DD} + 0.3**	V
V_{IL}	Input Low Voltage		– 0.3*	–	0.8	V

* : – 1.0V with a pulse width of 20% of t_{RC} (4ns max.)
** : V_{DD} + 1.0V with a pulse width of 20% of t_{RC} (4ns max.)

DC CHARACTERISTICS (Ta = 0° to 70°C, -12: V_{DD} = 3.3V + 0.3V or -0.2V, -15: V_{DD} = 3.3V ± 0.3V)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}		–	–	± 1	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0 V to V_{DD}		–	–	± 1	μA
V_{OH}	Output High Voltage	I_{OH} = – 2 mA		2.4	–	–	V
		I_{OH} = – 100 μA		V_{DD} – 0.2	–	–	
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		–	–	0.4	
		I_{OL} = 100 μA		–	–	0.2	
I_{DDO}	Operating Current	tcycle = Minimum Cycle, $\overline{CE}$ = V_{IL}	– 12	–	–	120	mA
		Other Inputs = V_{IH} or V_{IL}, Iout = 0 mA	– 15	–	–	100	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} Other Inputs = V_{IH} or V_{IL}, tcycle = Minimum Cycle		–	–	20	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} – 0.2 V Other Inputs = V_{DD} – 0.2 V or 0.2 V		–	–	300	μA

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1 to I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	×	L	Input	I_{DDO}
Outputs Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	×	×	High Impedance	I_{DDS}

×: Don't care

AC CHARACTERISTICS (Ta = 0° to 70°C, -12: V_{DD} = 3.3V + 0.3V or -0.2V, -15: V_{DD} = 3.3V ± 0.3V)

READ CYCLE

SYMBOL	PARAMETER	TC55 V328BJ/BFT-12		TC55 V328BJ/BFT-15		UNIT
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	12	–	15	–	ns
t_{ACC}	Address Access Time	–	12	–	15	
t_{CO}	Chip Enable Access Time	–	12	–	15	
t_{OE}	Output Enable Access Time	–	6	–	7	
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	
t_{COE}	Output Enable Time from Chip Enable	3	–	3	–	
t_{COD}	Output Disable Time from Chip Enable	–	7	–	8	
t_{OEE}	Output Enable Time from Output Enable	1	–	1	–	
t_{ODO}	Output Disable Time from Output Enable	–	7	–	8	

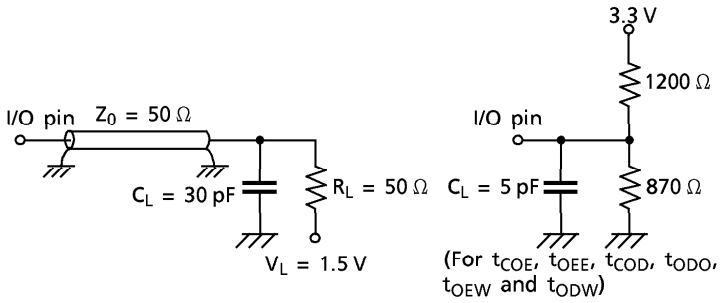
WRITE CYCLE

SYMBOL	PARAMETER	TC55 V328BJ/BFT-12		TC55 V328BJ/BFT-15		UNIT
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	12	–	15	–	ns
t_{WP}	Write Pulse Width	8	–	10	–	
t_{AW}	Address Valid to End of Write	10	–	10	–	
t_{CW}	Chip Enable to End of Write	10	–	11	–	
t_{AS}	Address Setup Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{DS}	Data Setup Time	7	–	8	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	7	–	8	

AC TEST CONDITIONS

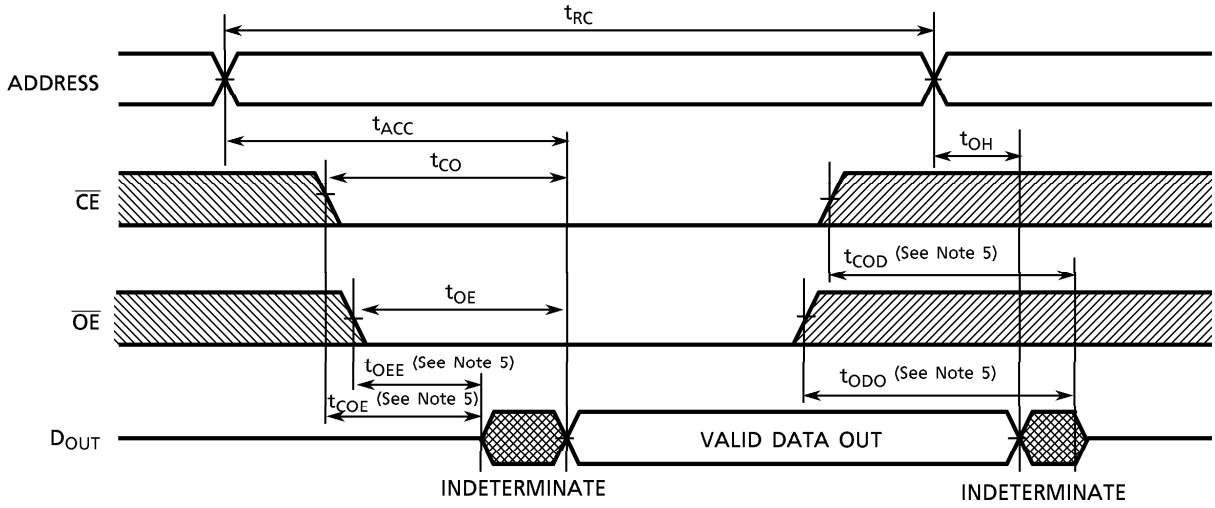
Input Pulse Levels	3.0 V, 0.0 V
Input Pulse Rise and Fall Time	3 ns
Input Timing Measurement Reference Levels	1.5 V
Output Timing Measurement Reference Levels	1.5 V
Output Load	Fig. 1

FIG. 1

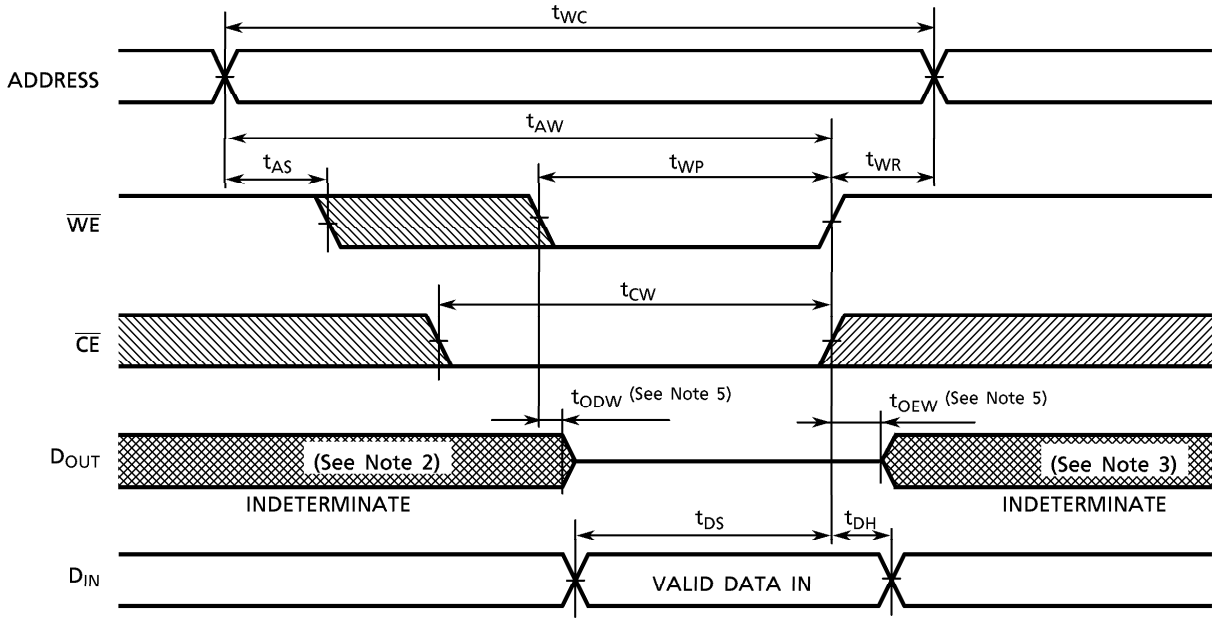


TIMING DIAGRAMS

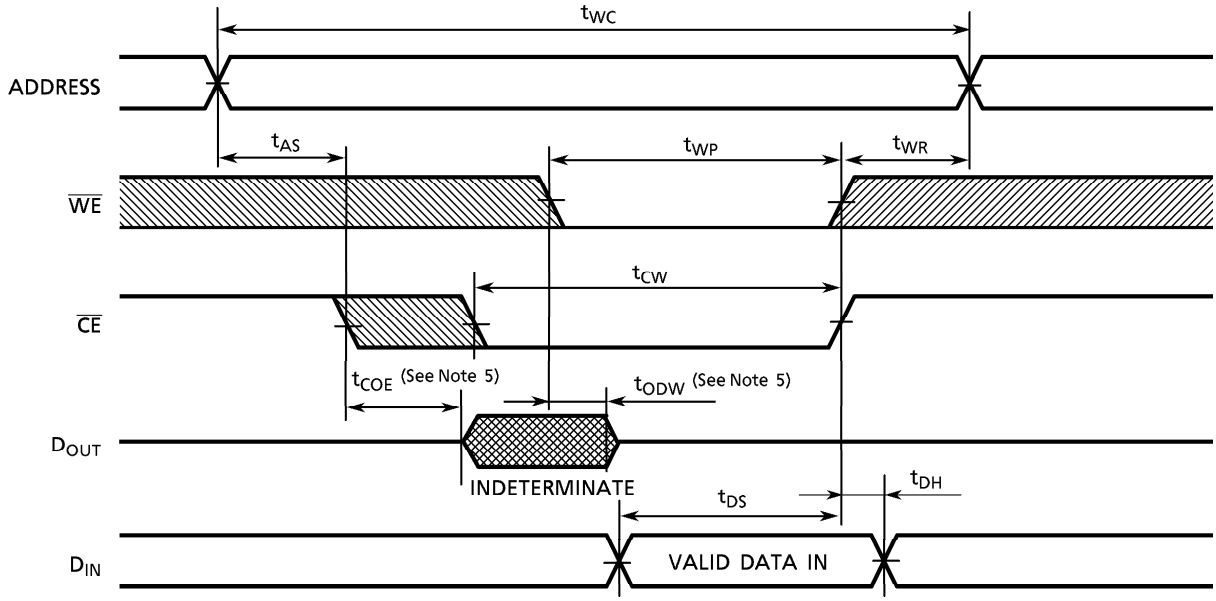
READ CYCLE (See Note 1)



WRITE CYCLE ($\overline{WE}$ CONTROLLED 1) (See Note 4)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 4)



Note: (1) $\overline{WE}$ remains HIGH for the read cycle.

(2) If $\overline{CE}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

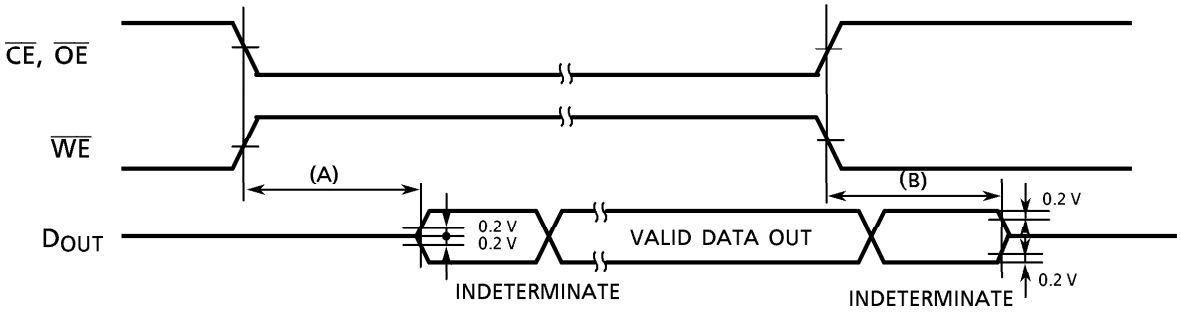
(3) If $\overline{CE}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

(4) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(5) The parameters are specified below measured using the load shown in Fig. 1.

(A) t_{COE}, t_{OEE}, t_{OEW} ····· Output Enable Time

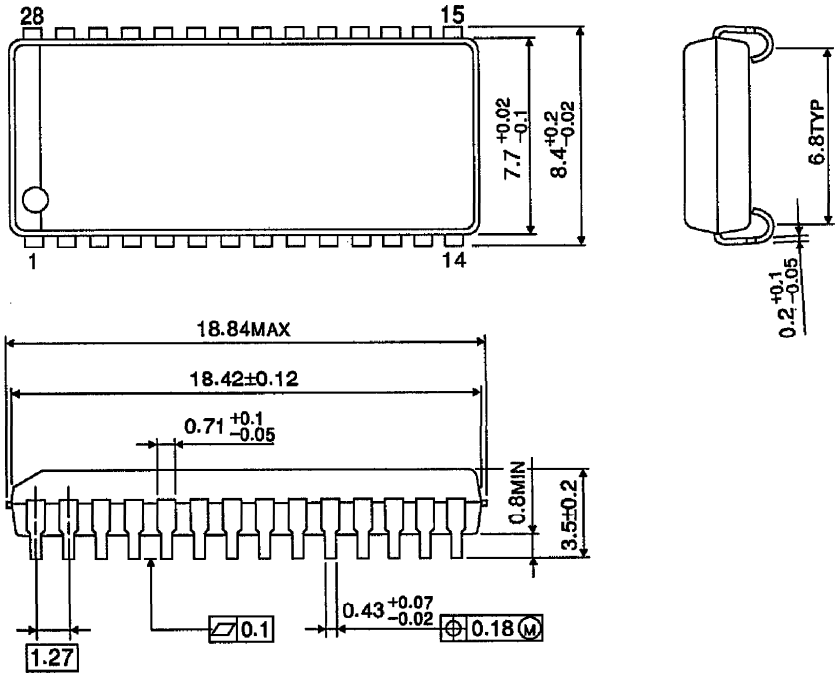
(B) t_{COD}, t_{ODO}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic SOJ (SOJ28-P-300-1.27A)

Unit in mm

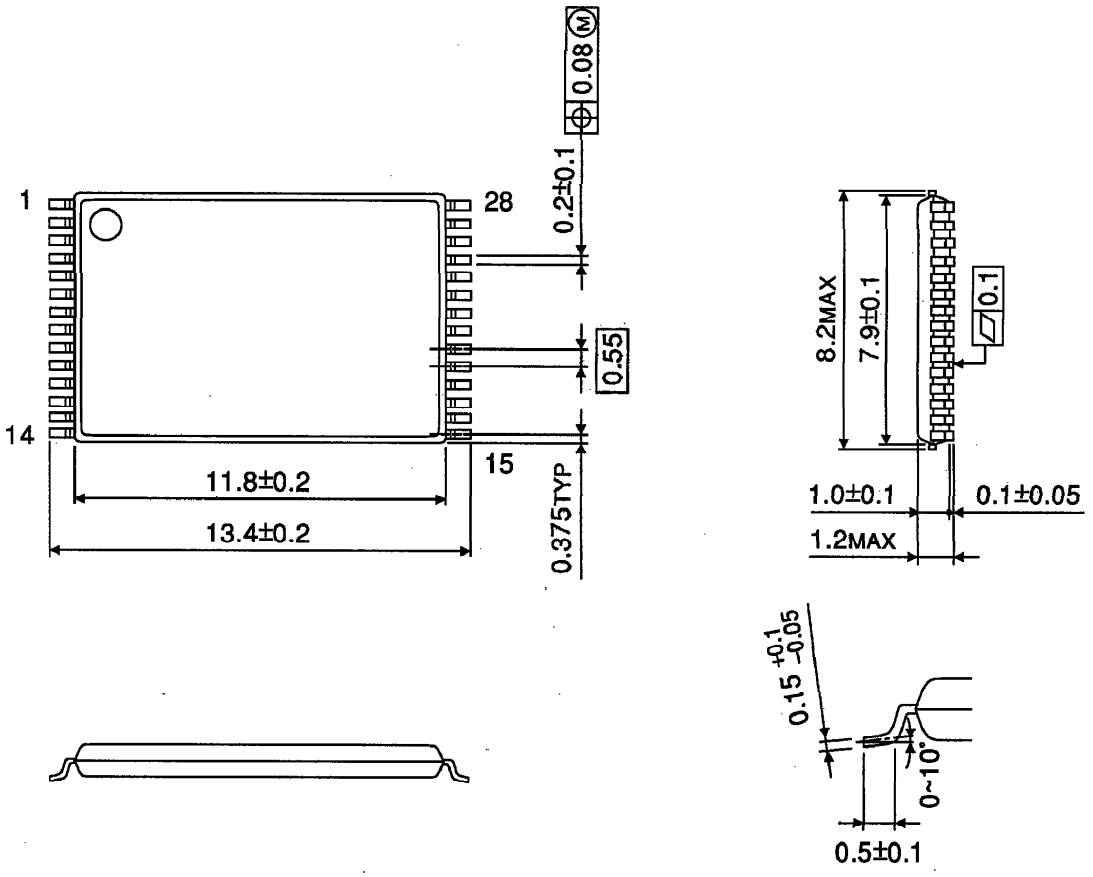


Weight : 0.83g (Typ.)

OUTLINE DRAWINGS

Plastic TSOP (TSOP I 28-P-0.55)

Unit in mm



Weight : 0.22g (Typ.)