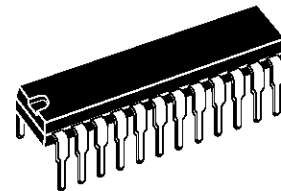


BUS-CONTROLLED AUDIO MATRIX

- 6 STEREO INPUTS
- 3 STEREO OUTPUTS
- GAIN CONTROL 0dB/MUTE FOR EACH OUTPUT
- CASCADABLE (2 DIFFERENT ADDRESSES)
- SERIAL BUS CONTROLLED
- VERY LOW NOISE
- VERY LOW DISTORSION
- FULLY ESD PROTECTED

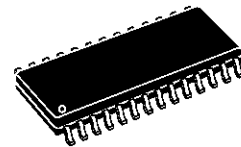
DESCRIPTION

The TEA6422 switches 6 stereo audio inputs on 3 stereo outputs.
All the switching possibilities are changed through the I²C BUS.



SHRINK 24
(Plastic Package)

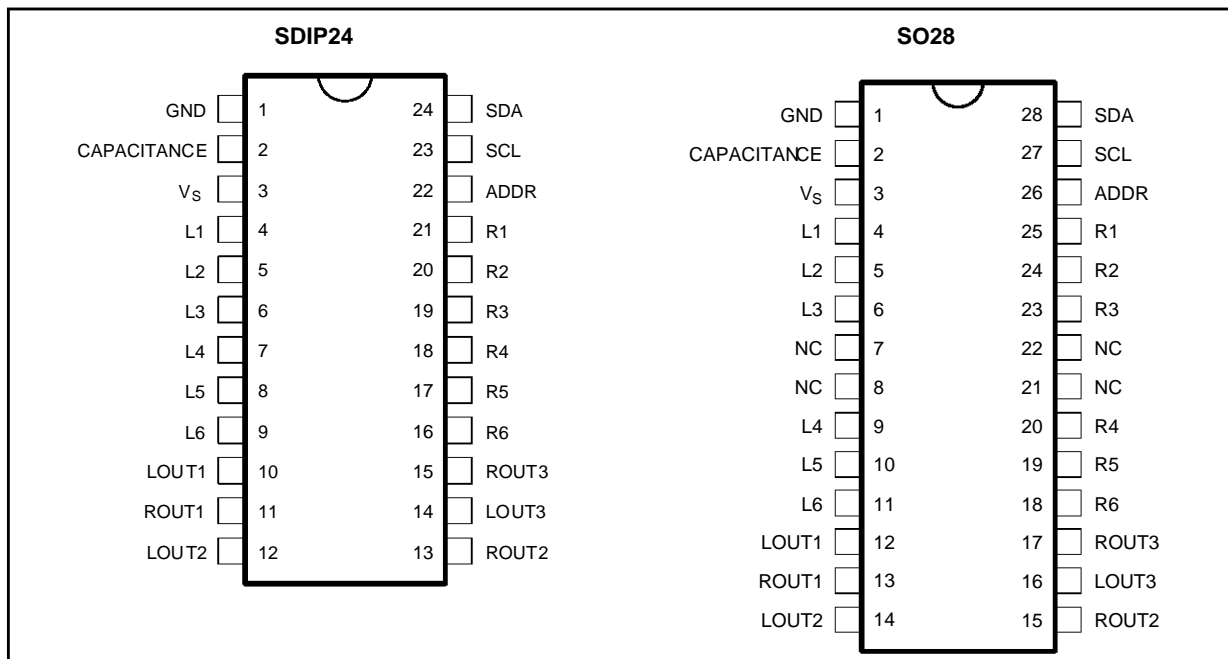
ORDER CODE : TEA6422



SO28
(Plastic Micropackage)

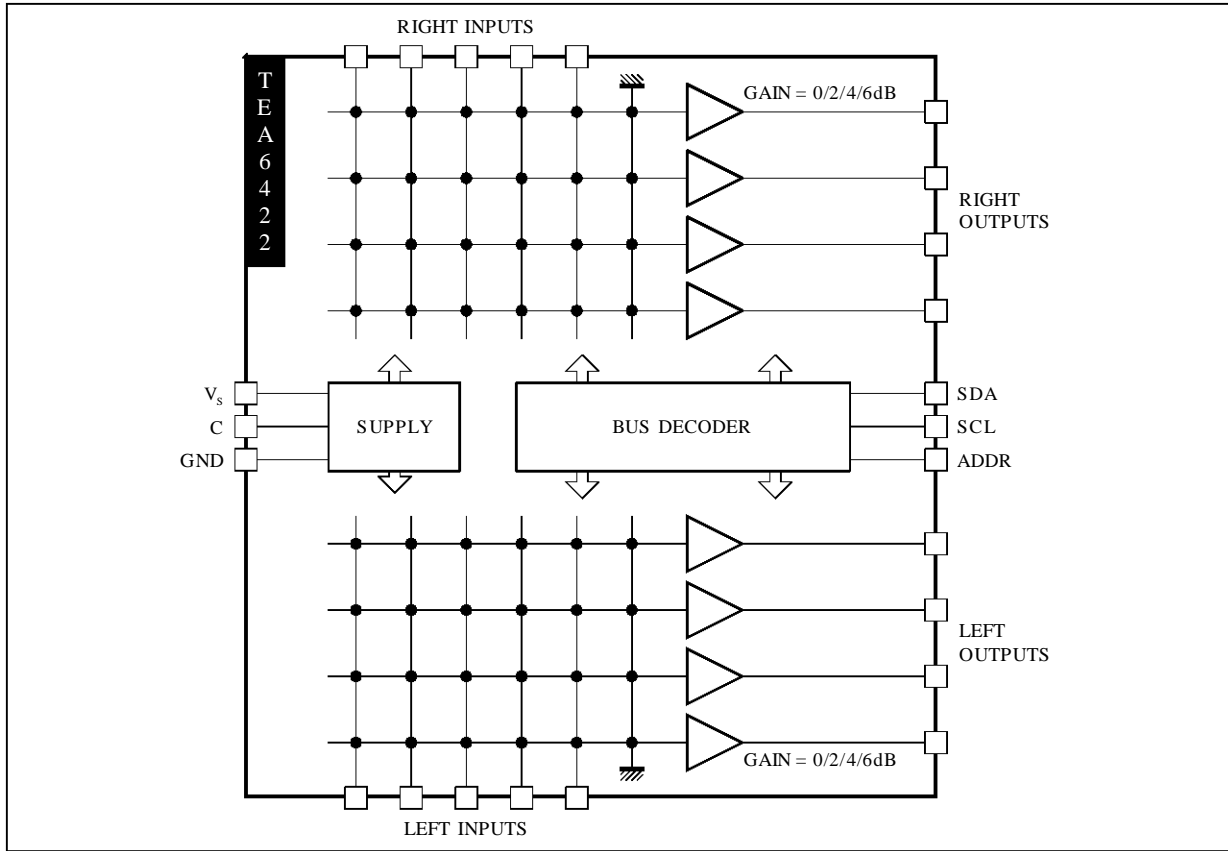
ORDER CODE : TEA6422D

PIN CONNECTIONS



6422-01.EPS / 6422-02.EPS

BLOCK DIAGRAM



6422-03.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	12	V
T _{oper}	Operating Temperature	0, + 70	°C
T _{stg}	Storage Temperature	- 20, + 150	°C

6422-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th(j-a)}	Junction - ambient Thermal Resistance	SDIP24	75
		SO28	75

6422-02.TBL

ELECTRICAL CHARACTERISTICS

$T_A = 25^{\circ}\text{C}$, $V_S = 9\text{V}$, $R_L = 10\text{k}\Omega$, $R_G = 600\Omega$, $f = 1\text{kHz}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

SUPPLY

V_S	Supply Voltage		8	9	10.2	V
I_S	Supply Current			3	8	mA
SVR	Ripple Rejection	$V_{IN} = 500\text{mV}_{\text{RMS}}$, $f = 1\text{kHz}$	70	80		dB

MATRIX

V_{IN}	Input DC Level			4.5		V
R_I	Input Resistance		30	50	100	$\text{k}\Omega$
C_S	Channel Separation	$V_{IN} = 2\text{V}_{\text{RMS}}$, $f = 1\text{kHz}$	80	90		dB

OUTPUT BUFFER

V_{OUT}	Output DC Level		4.2	4.5	4.8	V
R_{OUT}	Output Resistance			50	100	Ω
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		μV
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1\text{V}_{\text{RMS}}$		110		dB
G	Gain		-1	0	+ 1	dB
d	Distortion	$V_{IN} = V_{OUT} = 1\text{V}_{\text{RMS}}$		0.01	0.05	%
V_{CL}	Clipping Level	$d = 0.3\%$	2	2.5		V_{RMS}
R_L	Output Load Resistance		2			$\text{k}\Omega$

6422-03.TBL

I²C BUS CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
SCL					
V _{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V _{IH}	High Level Input Voltage		3.0	V _{CC} + 0.5	V
I _{LI}	Input Leakage Current	V _I = 0 to V _{CC}	- 10	+ 10	μA
f _{SCL}	Clock Frequency		0	100	kHz
t _R	Input Rise Time	1.5V to 3V		1000	ns
t _F	Input Fall Time	1.5V to 3V		300	ns
C _I	Input Capacitance			10	pF

SDA

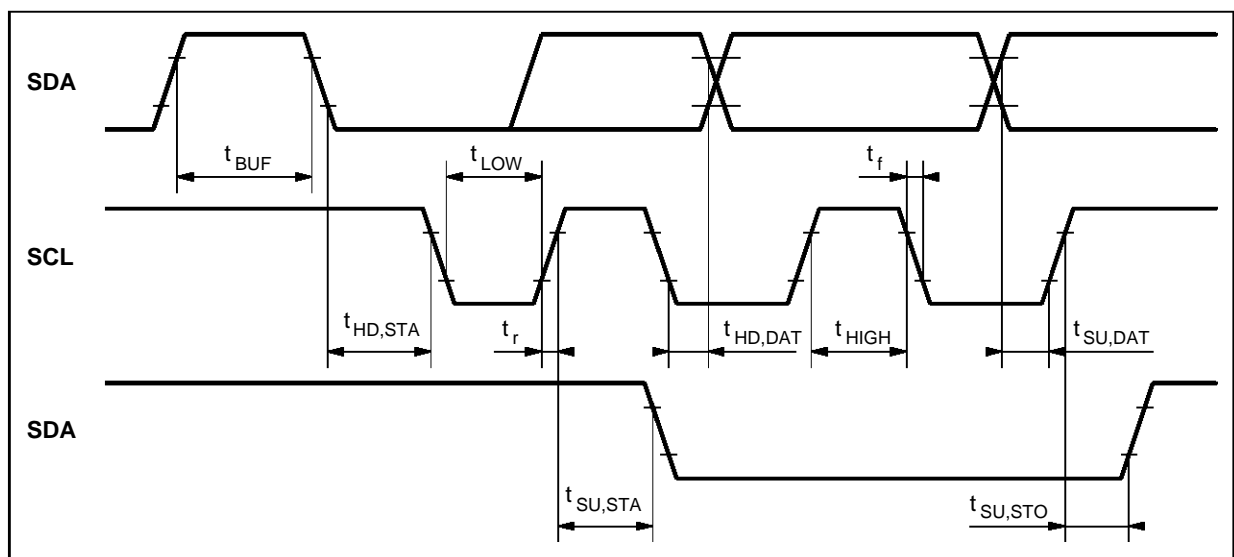
V _{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V _{IH}	High Level Input Voltage		3.0	V _{CC} + 0.5	V
I _{LI}	Input Leakage Current	V _I = 0 to V _{CC}	- 10	+ 10	μA
C _I	Input Capacitance			10	pF
t _R	Input Rise Time	1.5V to 3V		1000	ns
t _F	Input Fall Time	1.5V to 3V		300	ns
V _{OL}	Low Level Output Voltage	I _{OL} = 3mA		0.4	V
t _F	Output Fall Time	3V to 1.5V		250	ns
C _L	Load Capacitance			400	pF

TIMING

t _{LOW}	Clock Low Period		4.7		μs
t _{HIGH}	Clock High Period		4.0		μs
t _{SU, DAT}	Data Set-up Time		250		ns
t _{HD, DAT}	Data Hold Time		0	340	ns
t _{SU, STO}	Set-up Time from Clock High to Stop		4.0		μs
t _{BUF}	Start Set-up Time following a Stop		4.7		μs
t _{HD, STA}	Start Hold Time		4.0		μs
t _{SU, STA}	Start Set-up Time following Clock Low-to High Transition		4.7		μs

6422-04.TBL

Figure 1 : I²C Bus Timing



6422-04.LFS

POWER ON RESET

After power-on reset all outputs are in mute mode

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset	Start of Reset	Incr. V_{CC}	4.5		2.5	V
	End of Reset	Decr. V_{CC}			4.2	V
		Incr. V_{CC}				V

6422-05.TBL

SOFTWARE SPECIFICATION**1. Chip address**

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

2. Data bytes

Output select

X	0 0 1	0 1 0	X	X	l_2	l_1	l_0	Output 1 Output 2 Output 3

Input select

X	Q_1	Q_0	X	X	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1 0	Input 1 Input 2 Input 3 Input 4 Input 5 Input 6 Mute

6422-06.TBL

X = don't care - MSB is transmitted first

Example : 0 10 XX 10Q connects outputs 3 with input 5.

Figure 2 : Distorsion Level versus Input Voltage

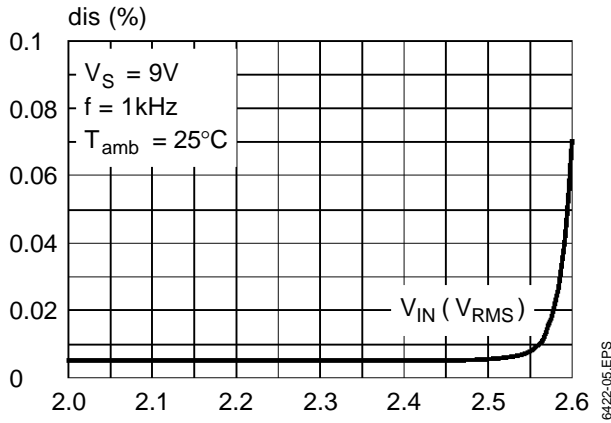


Figure 3 : Clipping Level versus Supply Voltage

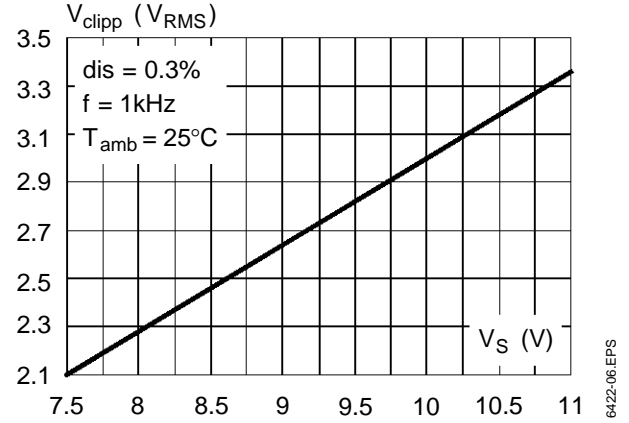
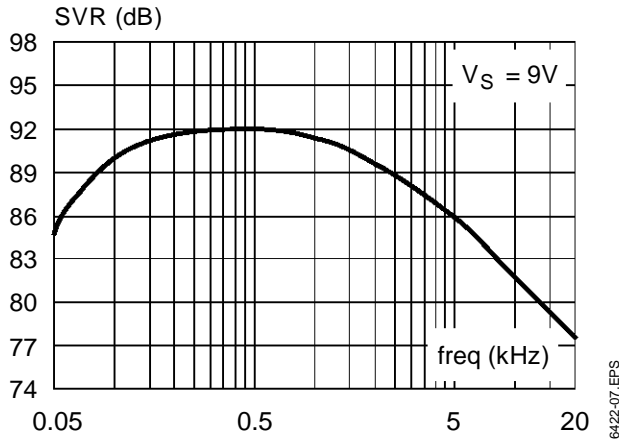
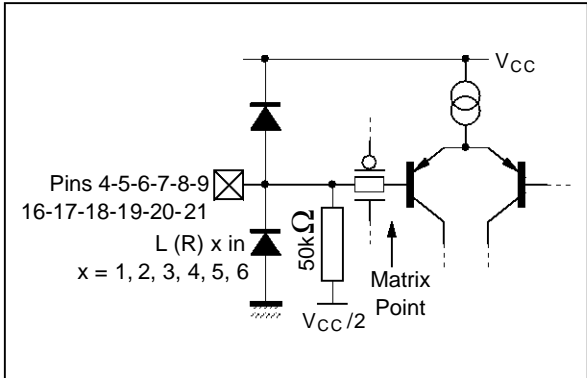


Figure 4 : Supply Voltage Rejection versus frequency ($V_{IN} = 500mV_{RMS}$)



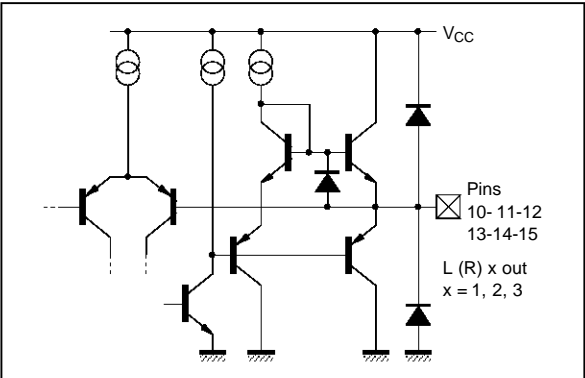
PIN CONFIGURATIONS (SDIP24 Package)

Figure 5 : Audio IN



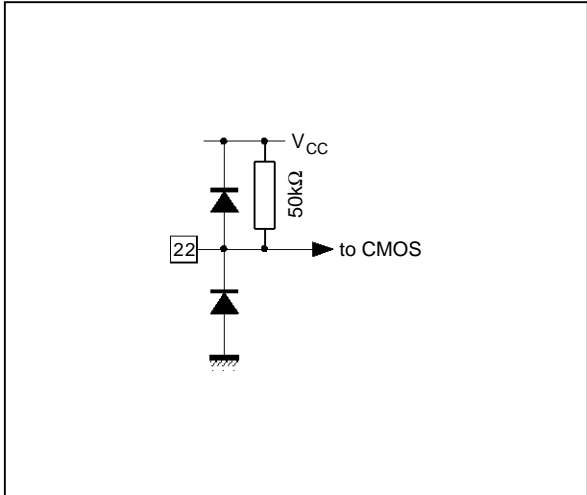
6422-08.EPS

Figure 6 : Audio OUT



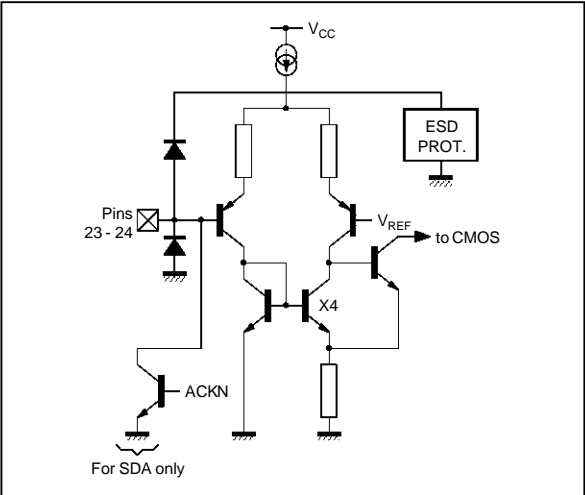
6422-09.EPS

Figure 7 : ADDR



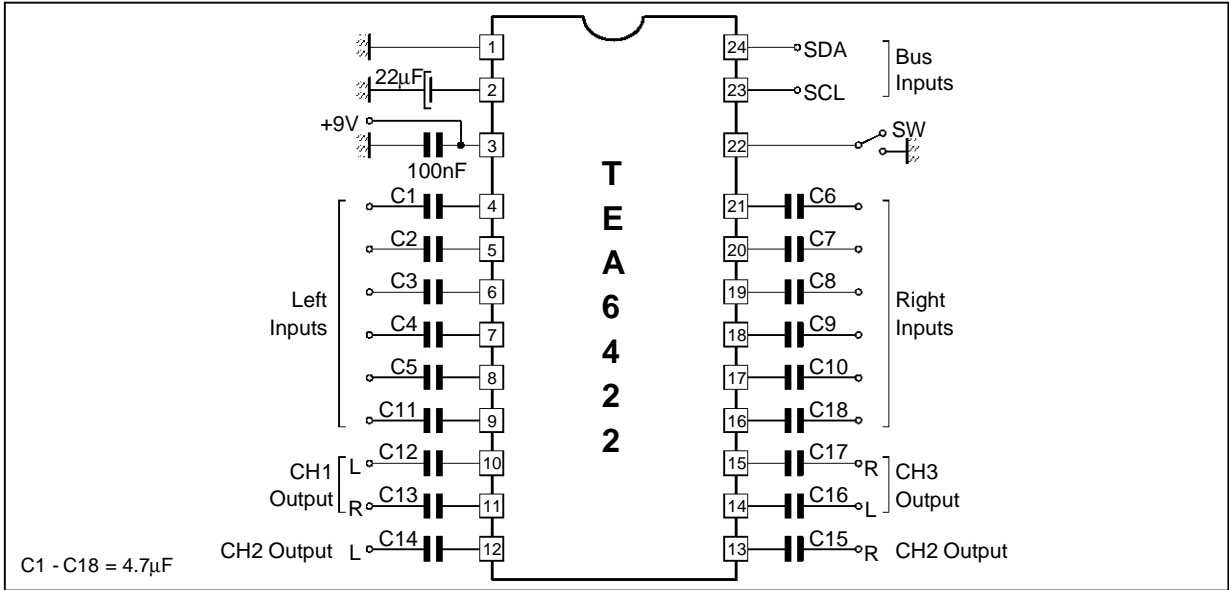
6422-10.EPS

Figure 8 : Bus Inputs (SDA, SCL)



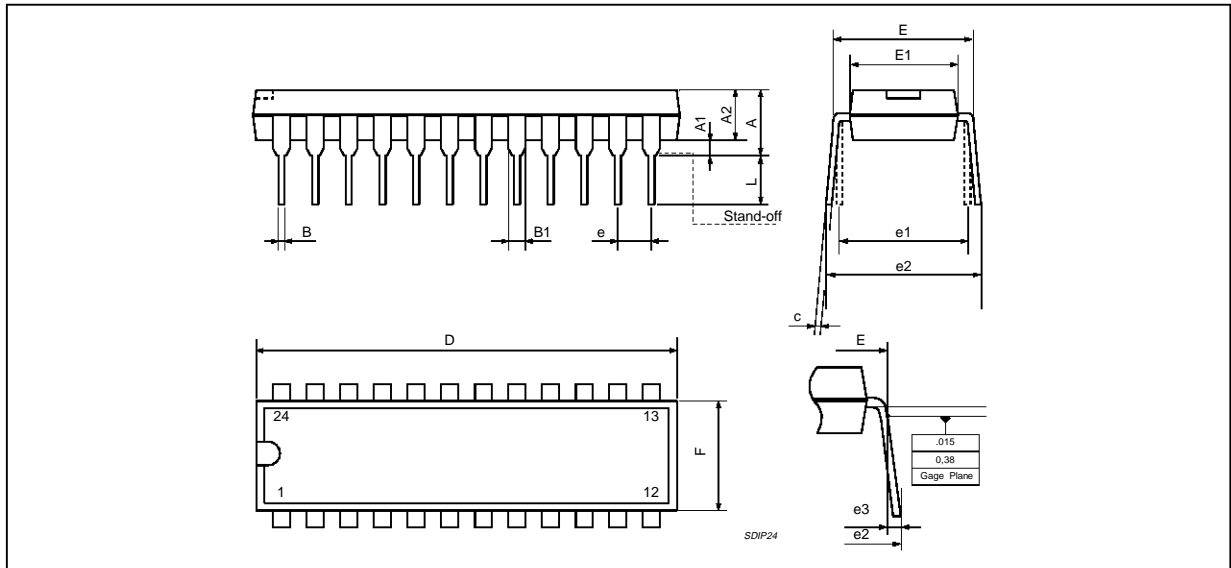
6422-11.EPS

TYPICAL APPLICATION (SDIP24 Package)



6422-12.EPS

PACKAGE MECHANICAL DATA
24 PINS - PLASTIC SHRINK



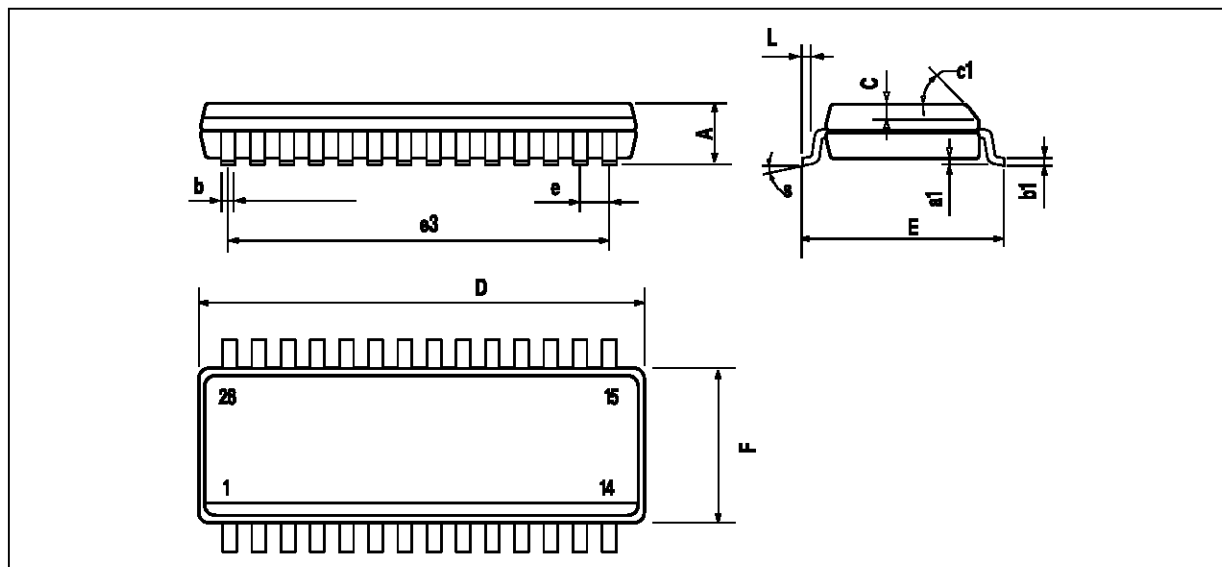
PMSDIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.30	4.57	0.120	0.130	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
C	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	22.61	22.86	23.11	0.890	0.90	0.910
E	7.62		8.64	0.30		0.340
E1	6.10	6.40	6.86	0.240	0.252	0.270
e		1.778			0.070	
e1		7.62			0.30	
e2			10.92			0.430
e3			1.52			0.060
L	2.54	3.30	3.81	0.10	0.130	0.150

SDIP24.TBL

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO28-EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (Typ.)					
D	17.7		18.1	0.697		0.713
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		16.51			0.65	
F	7.4		7.6	0.291		0.299
L	0.4		1.27	0.016		0.050
S	8° (Max.)					

SO28-TBL

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