NEC

MOS INTEGRATED CIRCUIT

μPD784035Y,784036Y,784037Y,784038Y

16-/8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD784038Y is based on the μPD784038 with an I²C bus control function added, and is ideal for audio-visual applications.

One-time PROM and EPROM versions, such as the μPD78P4038Y, that can operate in the same voltage range as mask ROM versions, and various development tools are provided.

The functions are explained in detail in the following User's Manual. Be sure to read this manual when designing your system.

μPD784038, 784038Y Subseries User's Manual - Hardware: U11316E
78K/IV Series User's Manual - Instruction: U10905E

FEATURES

- 78K/IV Series
- Pin-compatible with μPD78234 Subseries, μPD784026 Subseries, and μPD784038 Subseries
- Higher internal memory capacity than μPD78234 Subseries and μPD784026 Subseries
- Minimum instruction execution time: 125 ns (@ 32-MHz operation)
- I/O ports: 64
- Serial interface: 3 channels
  UART/IOE (3-wire serial I/O): 2 channels
  CSI (3-wire serial I/O, 2-wire serial I/O, I²C bus): 1 channel
- Timer/counter 16-bit timer/counter × 3 units 16-bit timer × 1 unit
- PWM output: 2 outputs
- Standby function
  HALT/STOP/IDLE mode
- Clock division function
- Watchdog timer: 1 channel
- Clock output function
  Selectable from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, and $f_{CLK}/16$
- A/D converter: 8-bit resolution × 8 channels
- D/A converter: 8-bit resolution × 2 channels
- Supply voltage: V_{DD} = 2.7 to 5.5 V

APPLICATION FIELDS

Cellular phones, cordless phones, audio-visual systems, etc.

Unless contextually excluded, references in this document to the μPD784038Y mean μPD784035Y, μPD784036Y, and μPD784037Y.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

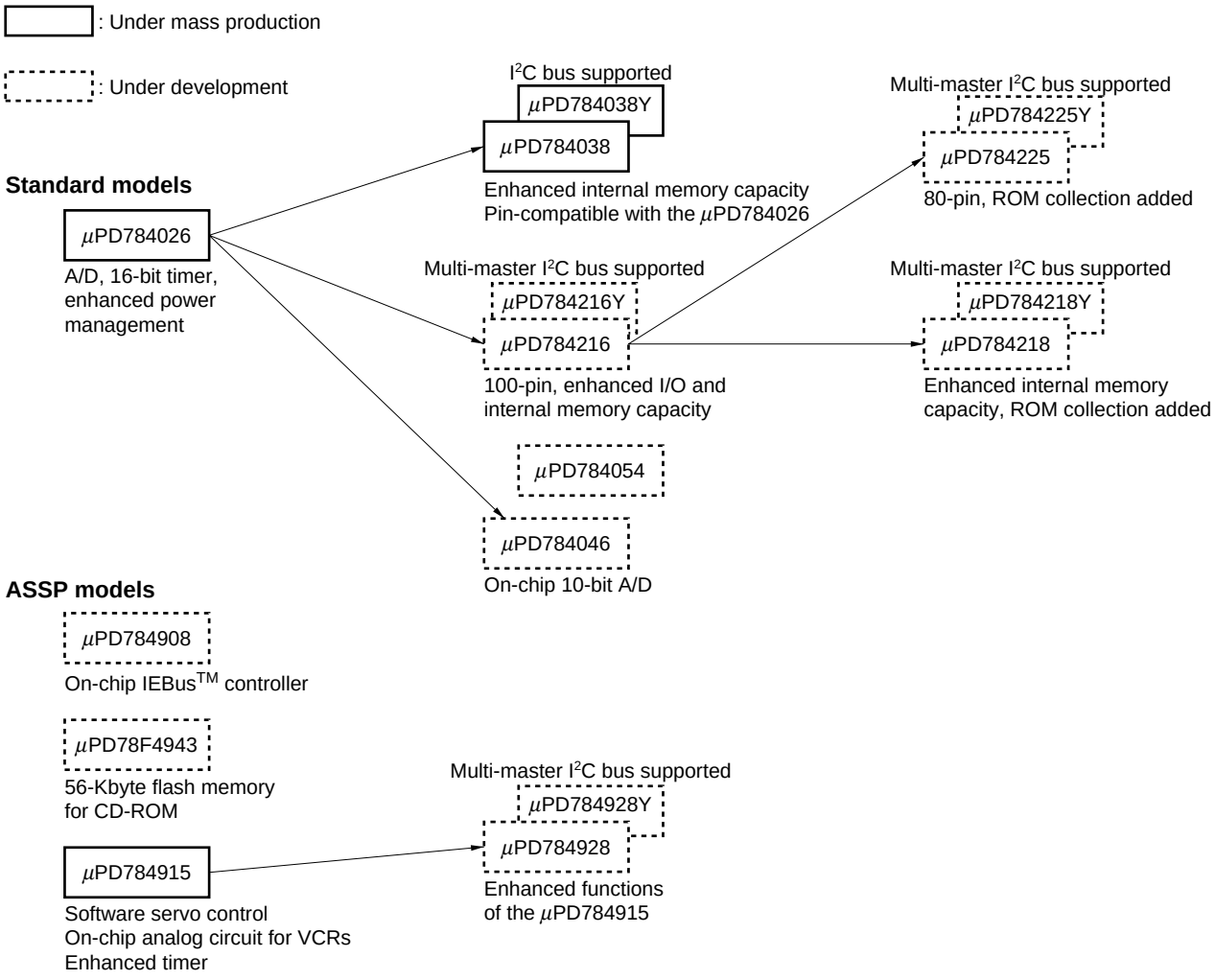
ORDERING INFORMATION

	Part Number	Package	Internal ROM (Bytes)	Internal RAM (Bytes)
	μPD784035YGC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)	48 K	2048
★	μPD784035YGC-×××-8BT	80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)	48 K	2048
	μPD784035YGK-×××-BE9[Note]	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	48 K	2048
	μPD784036YGC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)	64 K	2048
★	μPD784036YGC-×××-8BT	80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)	64 K	2048
	μPD784036YGK-×××-BE9[Note]	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	64 K	2048
	μPD784037YGC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)	96 K	3584
★	μPD784037YGC-×××-8BT	80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)	96 K	3584
	μPD784037YGK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	96 K	3584
	μPD784038YGC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)	128 K	4352
★	μPD784038YGC-×××-8BT	80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)	128 K	4352
	μPD784038YGK-×××-BE9	80-pin plastic TQFP (fine pitch) (12 × 12 mm)	128 K	4352

Note Under development

Remark ××× indicates the ROM code suffix.

★ 78K/IV Series Product Development



FUNCTIONS

Item \ Part Number		μPD784035Y	μPD784036Y	μPD784037Y	μPD784038Y
Number of basic instructions (mnemonics)		113			
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)			
Minimum instruction execution time		125 ns/250 ns/500 ns/1000 ns (@ 32-MHz operation)			
Internal memory	ROM	48 KBytes	64 KBytes	96 KBytes	128 KBytes
	RAM	2048 Bytes		3584 Bytes	4352 Bytes
Memory space		1 MByte with program and data spaces combined			
I/O port	Total	64			
	Input	8			
	I/O	56			
Pins with ancillary function[Note]	Pins with pull-up resistor	54			
	LEDs direct drive output	24			
	Transistor direct drive	8			
Real-time output port		4 bits × 2 or 8 bits × 1			
Timer/counter		Timer/counter 0: (16 bits) Timer register × 1, Capture register × 1, Compare register × 2 — Pulse output: • Toggle output • PWM/PPG output • One-shot pulse output			
		Timer/counter 1: (8/16 bits) Timer register × 1, Capture register × 1, Capture/compare register × 1, Compare register × 1 — Pulse output: • Real-time output (4 bits × 2)			
		Timer/counter 2: (8/16 bits) Timer register × 1, Capture register × 1, Capture/compare register × 1, Compare register × 1 — Pulse output: • Toggle output • PWM/PPG output			
		Timer 3: (8/16 bits) Timer register × 1, Compare register × 1			
PWM output		12-bit resolution × 2 channels			
Serial interface		UART/IOE (3-wire serial I/O) : 2 channels (on-chip baud rate generator) CSI (3-wire serial I/O, 2-wire serial I/O, I^2C bus) : 1 channel			
A/D converter		8-bit resolution × 8 channels			
D/A converter		8-bit resolution × 2 channels			
Clock output		Selectable from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, $f_{CLK}/16$ (can also be used as 1-bit output port)			
Watchdog timer		1 channel			
Standby		HALT/STOP/IDLE mode			
Interrupt	Hardware source	24 (internal: 17, external: 7 (variable sampling clock input: 1))			
★	Software source	BRK instruction, BRKCS instruction, operand error			
	Non-maskable	Internal: 1, external: 1			
	Maskable	Internal: 16, external: 6			
		• 4 programmable priority levels • 3 processing styles: vectored interrupt/macro service/context switching			
Supply voltage		V_{DD} = 2.7 to 5.5 V			
★ Package		80-pin plastic QFP (14 × 14 mm, 2.7-mm thick) 80-pin plastic QFP (14 × 14 mm, 1.4-mm thick) 80-pin plastic TQFP (fine pitch) (12 × 12 mm)			

Note The pins with ancillary function are included in the I/O pins.

CONTENTS

1. DIFFERENCES AMONG MODELS IN μPD784038Y SUBSERIES

The only difference among the μPD784035Y, 784036Y, 784037Y, and 784038Y lies in the internal memory capacity.

The μPD78P4038Y is provided with a 128-KB one-time PROM or EPROM instead of the mask ROM of the above models. These differences are summarized in Table 1-1.

★ **Table 1-1. Differences among Models in μPD784038Y Subseries**

Part Number / Item	μPD784031Y	μPD784035Y	μPD784036Y	μPD784037Y	μPD784038Y	μPD78P4038Y
Internal ROM	Not available	48 KBytes (mask ROM)	64 KBytes (mask ROM)	96 KBytes (mask ROM)	128 KBytes (mask ROM)	128 KBytes (one-time PROM or EPROM)
Internal RAM	2048 Bytes			3584 Bytes	4352 Bytes	
Package	80-pin plastic QFP (14 × 14 mm, 2.7-mm thick) 80-pin plastic QFP (14 × 14 mm, 1.4-mm thick) 80-pin plastic TQFP (fine pitch) (12 × 12 mm)					80-pin ceramic WQFN (14 × 14 mm)

2. MAJOR DIFFERENCES FROM μPD784026 SUBSERIES AND μPD78234 SUBSERIES

Item \ Series Name		μPD784038Y Subseries μPD784038 Subseries	μPD784026 Subseries	μPD78234 Subseries
Number of basic instructions (mnemonics)		113		65
Minimum instruction execution time		125 ns (@ 32-MHz operation)	160 ns (@ 25-MHz operation)	333 ns (@ 12-MHz operation)
Memory space (program/data)		1 MByte combined		64 KBytes/1 MByte
Timer/counter		16-bit timer/counter × 1 8-/16-bit timer/counter × 2 8-/16-bit timer × 1		16-bit timer/counter × 1 8-bit timer/counter × 2 8-bit timer × 1
Clock output function		Provided		None
Watchdog timer		Provided		None
Serial interface		UART/IOE (3-wire serial I/O) × 2 channels CSI (3-wire serial I/O, 2-wire serial I/O, I^2C bus[Note]) × 1 channel	UART/IOE (3-wire serial I/O) × 2 channels CSI (3-wire serial I/O, SBI) × 1 channel	UART × 1 channel CSI (3-wire serial I/O, SBI) × 1 channel
Interrupt	Context switching	Provided		None
	Priority	4 levels		2 levels
Standby function		HALT/STOP/IDLE modes		HALT/STOP modes
Operating clock		Selectable from $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, and $f_{XX}/16$		Fixed to $f_{XX}/2$
Pin function	MODE pin	None		Specifies ROM-less mode (always high level with μPD78233 and 78237)
	TEST pin	Device test pin Usually, low level		None
★ Package		80-pin plastic QFP (14 × 14 mm, 2.7-mm thick) 80-pin plastic QFP (14 × 14 mm, 1.4-mm thick) 80-pin plastic TQFP (fine pitch) (12 × 12 mm) 80-pin ceramic WQFN (14 × 14 mm): μPD78P4038Y and 78P4038 only	80-pin plastic QFP (14 × 14 mm, 2.7-mm thick) 80-pin plastic TQFP (fine pitch) (12 × 12 mm): μPD784021 only 80-pin ceramic WQFN (14 × 14 mm): μPD78P4026 only	80-pin plastic QFP (14 × 14 mm, 2.7-mm thick) 94-pin plastic QFP (20 × 20 mm) 84-pin plastic QFJ (1150 × 1150 mil) 94-pin ceramic WQFN (20 × 20 mm): μPD78P238 only

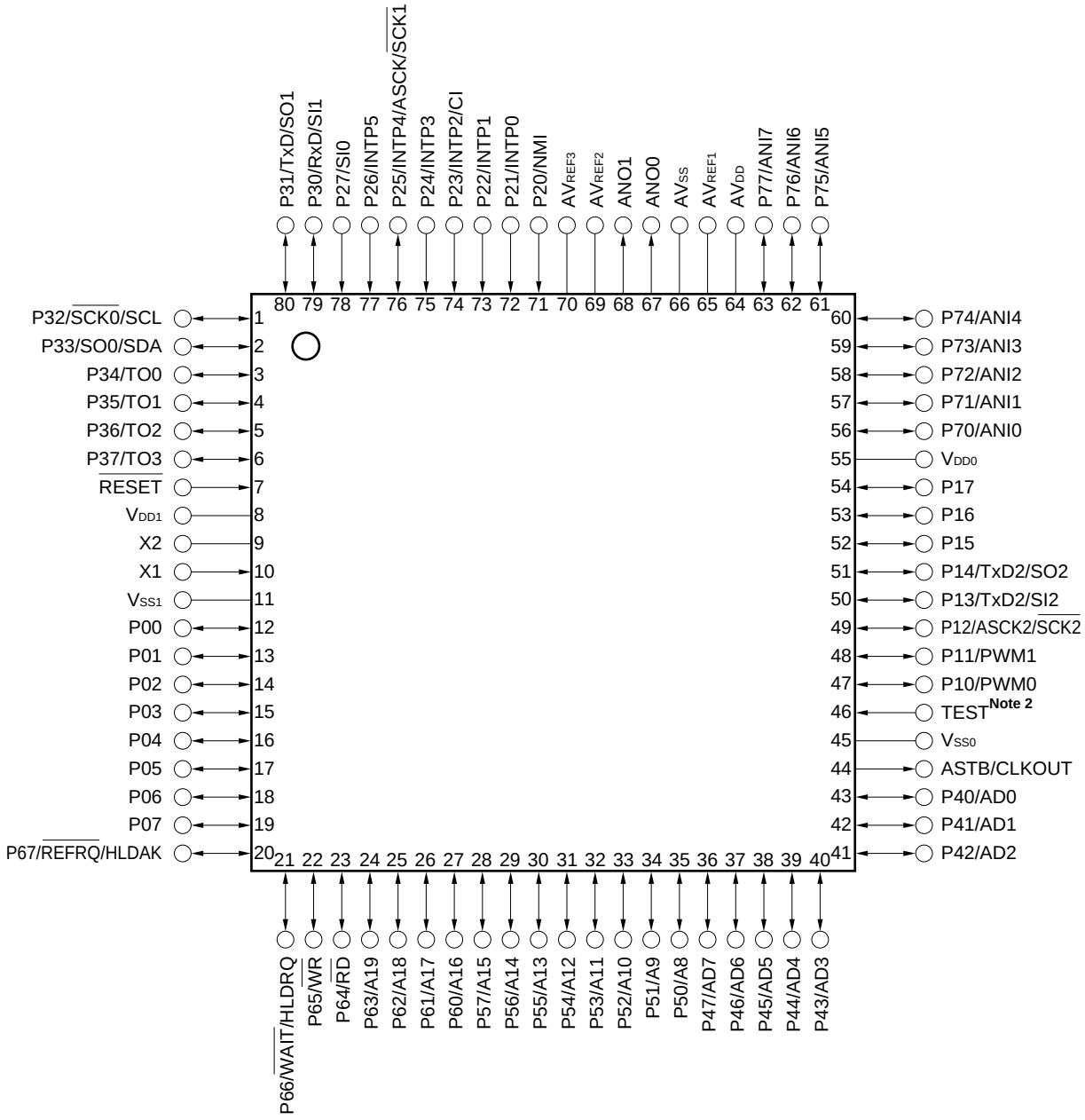
Note μPD784038Y Subseries only

3. PIN CONFIGURATION (Top View)

- 80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)
  μPD784035YGC-×××-3B9, 784036YGC-×××-3B9, 784037YGC-×××-3B9, 784038YGC-×××-3B9

★ • 80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)
  μPD784035YGC-×××-8BT, 784036YGC-×××-8BT, 784037YGC-×××-8BT, 784038YGC-×××-8BT

- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
  μPD784035YGK-×××-BE9[Note 1], 784036YGK-×××-BE9[Note 1], 784037YGK-×××-BE9, 784038YGK-×××-BE9

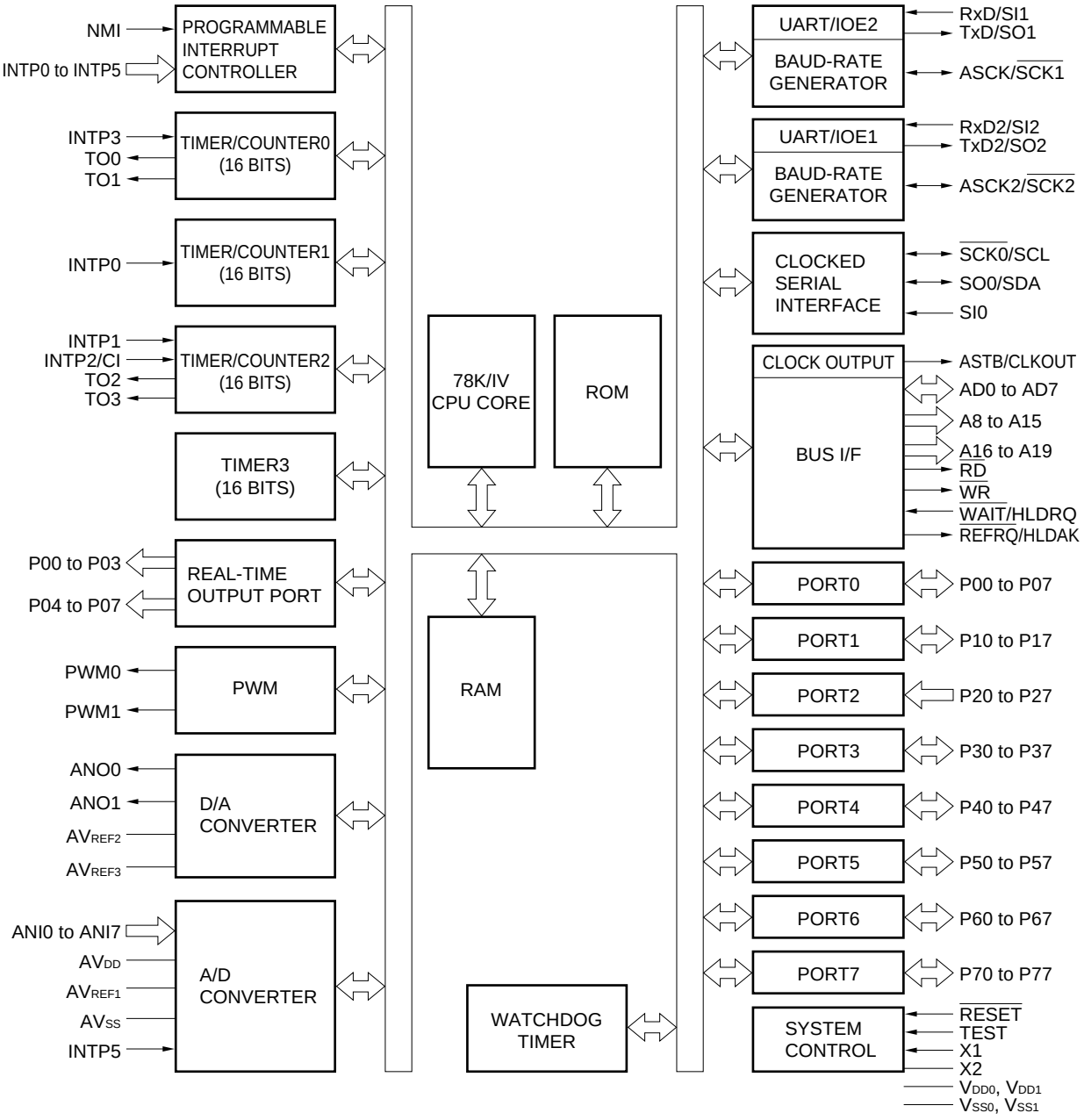


Notes 1. Under development

2. TEST pin should be connected to V_{SS0} directly.

A8 to A19 : Address Bus
AD0 to AD7 : Address/Data Bus
ANI0 to ANI7 : Analog Input
ANO0, ANO1 : Analog Output
ASCK, ASCK2 : Asynchronous Serial Clock
ASTB : Address Strobe
AV_{DD} : Analog Power Supply
AV_{REF1} to AV_{REF3} : Reference Voltage
AV_{SS} : Analog Ground
CI : Clock Input
CLKOUT : Clock Output
HLDAK : Hold Acknowledge
HLDRQ : Hold Request
INTP0 to INTP5 : Interrupt from Peripherals
NMI : Non-maskable Interrupt
P00 to P07 : Port0
P10 to P17 : Port1
P20 to P27 : Port2
P30 to P37 : Port3
P40 to P47 : Port4
P50 to P57 : Port5
P60 to P67 : Port6
P70 to P77 : Port7
PWM0, PWM1 : Pulse Width Modulation Output
$\overline{RD}$: Read Strobe
$\overline{REFRQ}$: Refresh Request
$\overline{RESET}$: Reset
RxD, RxD2 : Receive Data
$\overline{SCK0}$ to $\overline{SCK2}$: Serial Clock
SCL : Serial Clock
SDA : Serial Data
SI0 to SI2 : Serial Input
SO0 to SO2 : Serial Output
TEST : Test
TO0 to TO3 : Timer Output
TxD, TxD2 : Transmit Data
V_{DD0} to V_{DD1} : Power Supply
V_{SS0} to V_{SS1} : Ground
$\overline{WAIT}$: Wait
$\overline{WR}$: Write Strobe
X1, X2 : Crystal

4. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities differ depending on the model.

5. PIN FUNCTION

5.1 Port Pins

Pin Name	I/O	Alternate function	Function
P00 to P07	I/O	–	Port 0 (P0): • 8-bit I/O port • Can be used as real-time output port (4 bits × 2). • Can be set in input or output mode bitwise. • Pins set in input mode can be connected to internal pull-up resistors by software. • Can drive transistor.
P10	I/O	PWM0	Port 1 (P1): • 8-bit I/O port • Can be set in input or output mode bitwise. • Pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.
P11		PWM1	
P12		ASCK2/$\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15 to P17		–	
P20	Input	NMI	Port 2 (P2): • 8-bit input port • P20 cannot be used as general-purpose port pin (non-maskable interrupt). However, its input level can be checked by interrupt routine. • P22 through P27 can be connected to internal pull-up resistors by software in 6-bit units. • P25/INTP4/ASCK/$\overline{\text{SCK1}}$ pin can operate as $\overline{\text{SCK1}}$ output pin if so specified by CSIM1.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	I/O	RxD/S1	Port 3 (P3): • 8-bit I/O port • Can be set in input or output mode bitwise. • Pins set in input mode can be connected to internal pull-up resistors by software.
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$/SCL	
P33		SO0/SDA	
P34 to P37		TO0 to TO3	
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port • Can be set in input or output mode bitwise. • Pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.
P50 to P57	I/O	A8 to A15	Port 5 (P5): • 8-bit I/O port • Can be set in input or output mode bitwise. • Pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.

Pin Name	I/O	Alternate function	Function
P60 to P63	I/O	A16 to A19	Port6 (P6): • 8-bit I/O port • Can be set in input or output mode bitwise. • Pins set in input mode can be connected to internal pull-up resistors by software.
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/HLDRQ	
P67		$\overline{REFRQ}$/HLDAK	
P70 to P77	I/O	AN10 to AN17	Port 7 (P7): • 8-bit I/O port • Can be set in input or output mode bitwise.

5.2 Non-Port Pins

Pin Name	I/O	Alternate function	Function	
TO0 to TO3	Output	P34 to P37	Timer output	
CI	Input	P23/INTP2	Count clock input to timer/counter 2	
RxD	Input	P30/SI1	Serial data input (UART0)	
RxD2		P13/SI2	Serial data input (UART2)	
TxD	Output	P31/SO1	Serial data output (UART0)	
TxD2		P14/SO2	Serial data output (UART2)	
ASCK	Input	P25/INTP4/$\overline{\text{SCK1}}$	Baud rate clock input (UART0)	
ASCK2		P12/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)	
SDA	I/O	P33/SO0	Serial data input/output (2-wire serial I/O, I^2C bus)	
SI0	Input	P27	Serial data input (3-wire serial I/O0)	
SI1		P30/RxD	Serial data input (3-wire serial I/O1)	
SI2		P13/RxD2	Serial data input (3-wire serial I/O2)	
SO0	Output	P33/SDA	Serial data output (3-wire serial I/O0)	
SO1		P31/TxD	Serial data output (3-wire serial I/O1)	
SO2		P14/TxD2	Serial data output (3-wire serial I/O2)	
$\overline{\text{SCK0}}$	I/O	P32/SCL	Serial clock input/output (3-wire serial I/O0)	
$\overline{\text{SCK1}}$		P25/INTP4/ASCK	Serial clock input/output (3-wire serial I/O1)	
$\overline{\text{SCK2}}$		P12/ASCK2	Serial clock input/output (3-wire serial I/O2)	
SCL		P32/$\overline{\text{SCK0}}$	Serial clock input/output (2-wire serial I/O, I^2C bus)	
NMI	Input	P20	External interrupt requests	–
INTP0		P21		• Count clock input to timer/counter 1 • Capture trigger signal of CR11 or CR12
INTP1		P22		• Count clock input to timer/counter 2 • Capture trigger signal of CR22
INTP2		P23/CI		• Count clock input to timer/counter 2 • Capture trigger signal of CR21
INTP3		P24		• Count clock input to timer/counter 0 • Capture trigger signal of CR02
INTP4		P25/ASCK/$\overline{\text{SCK1}}$		–
INTP5		P26		Conversion start trigger input to A/D converter
AD0 to AD7	I/O	P40 to P47	Time-division address/data bus (for external memory connection)	
A8 to A15	Output	P50 to P57	Higher address bus (for external memory connection)	
A16 to A19	Output	P60 to P63	Higher address when address is extended (for external memory connection)	
$\overline{\text{RD}}$	Output	P64	Read strobe to external memory	
$\overline{\text{WR}}$	Output	P65	Write strobe to external memory	
$\overline{\text{WAIT}}$	Input	P66/HLDRQ	Wait insertion	
$\overline{\text{REFRQ}}$	Output	P67/HLDAK	Refresh pulse output to external pseudo static memory	
HLDRQ	Input	P66/$\overline{\text{WAIT}}$	Bus hold request input	
HLDAK	Output	P67/$\overline{\text{REFRQ}}$	Bus hold acknowledge output	
ASTB	Output	CLKOUT	Latch timing output of time-division address (A0 through A7) (when accessing external memory)	
CLKOUT	Output	ASTB	Clock output	

Pin Name	I/O	Alternate function	Function
$\overline{\text{RESET}}$	Input	–	Chip reset
X1	Input	–	Crystal connection for system clock oscillation
X2	–		(Clock can also be input to X1).
ANI0 to ANI7	Input	P70 to P77	Analog voltage input to A/D converter
ANO0, ANO1	Output	–	Analog voltage output from D/A converter
AV_{REF1}	–	–	Reference voltage to A/D converter
AV_{REF2}, AV_{REF3}			Reference voltage to D/A converter
AV_{DD}			A/D converter power supply
AV_{SS}			A/D converter GND
★ V_{DD0} **Note1**			Positive power supply of the port block
★ V_{DD1} **Note1**			Positive power supply except for the port block
★ V_{SS0} **Note2**			GND of the port block
★ V_{SS1} **Note2**			GND except for the port block
TEST			Directly connect to V_{SS0} (IC test pin).

Notes 1. The potential of the V_{DD0} pin must be equal to that of the V_{DD1} pin.

2. The potential of the V_{SS0} pin must be equal to that of the V_{SS1} pin.

5.3 Types of Pin I/O Circuits and Connections for Unused Pins

Table 5-1 shows types of pin I/O circuits and the connections for unused pins.
For the input/output circuit of each type, refer to Figure 5-1.

★ **Table 5-1. Types of Pin I/O Circuits and Connections for Unused Pins**

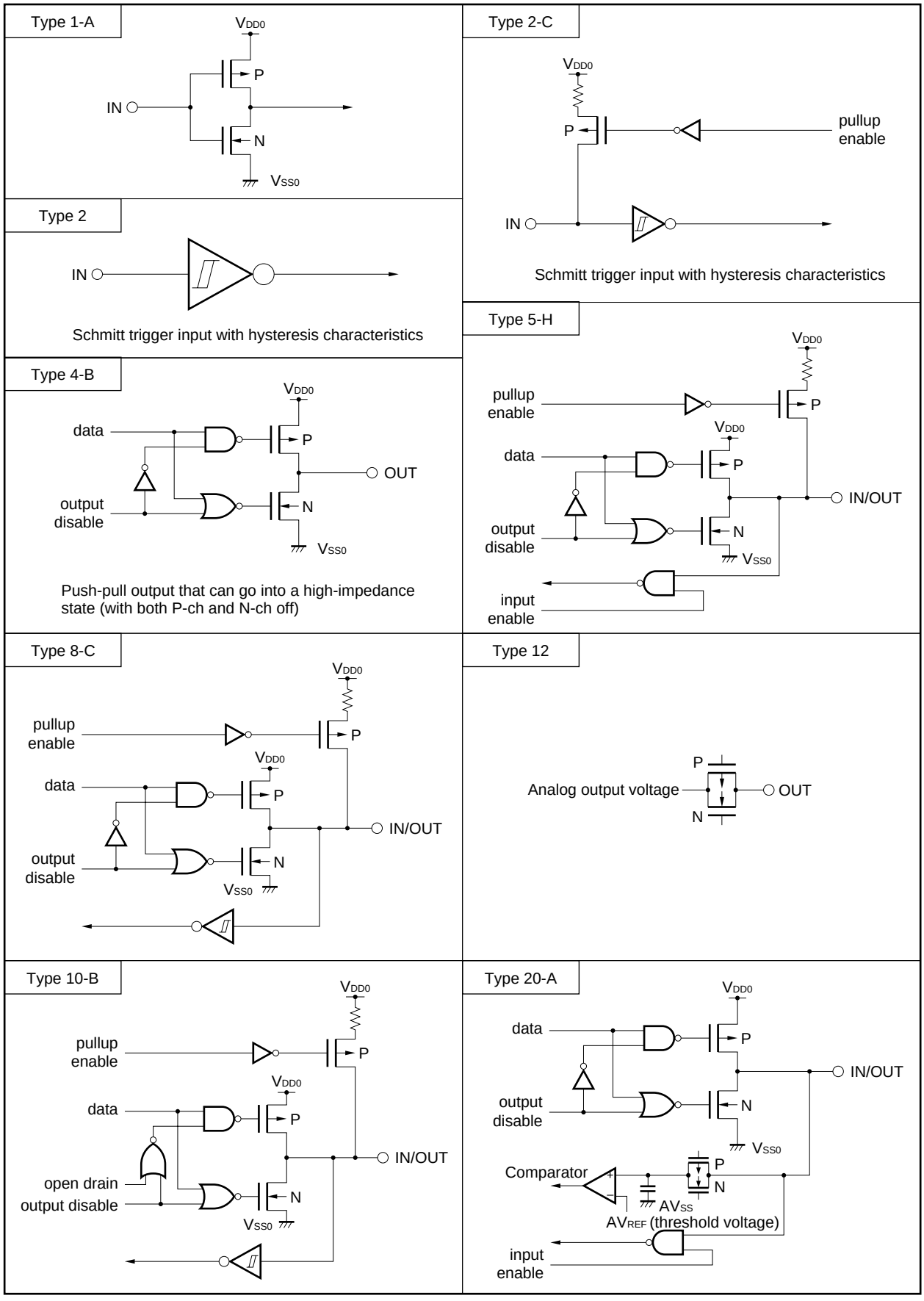
Pin Name	I/O Circuit Type	I/O	Recommended Connection for Unused Pins
P00 to P07	5-H	I/O	Input: Connect to V_{DD0} Output: Open
P10/PWM0 P11/PWM1			
P12/ASCK2/$\overline{SCK2}$	8-C		
P13/RxD2/SI2	5-H		
P14/TxD2/SO2			
P15 to P17			
P20/NMI	2	Input	Connect to V_{DD0} or V_{SS0}.
P21/INTP0			
P22/INTP1	2-C		Connect to V_{DD0}.
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-C	I/O	Input: Connect to V_{DD0} Output: Open
P26/INTP5	2-C	Input	Connect to V_{DD0}.
P27/SI0			
P30/RxD/SI1	5-H	I/O	Input: Connect to V_{DD0}. Output: Open
P31/TxD/SO1			
P32/$\overline{SCK0}$/SCL	10-B		
P33/SO0/SDA			
P34/TO0 to P37/TO3	5-H		
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0 to P77/ANI7	20-A	I/O	Input: Connect to V_{DD0} or V_{SS0}. Output: Open
ANO0, ANO1	12	Output	Open
ASTB/CLKOUT	4-B		

Pin Name	I/O Circuit Type	I/O	Recommended Connection for Unused Pins
$\overline{\text{RESET}}$	2	Input	–
TEST	1-A		Directly connect to V_{SS0}.
AV_{REF1} to AV_{REF3}	–		Connect to V_{SS0}.
AV_{SS}			
AV_{DD}			Connect to V_{DD0}.

Caution Connect an I/O pin whose input/output mode is unstable to V_{DD0} via a resistor of several 10 kΩ (especially if the voltage on the reset input pin rises higher than the low-level input level on power application or when the mode is switched between input and output by software).

Remark Because the circuit type numbers shown in the above table are commonly used with all the models in the 78K Series, these numbers of some models are not serial (because some circuits are not provided to some models).

★ **Figure 5-1. Types of Pin I/O Circuits**



6. CPU ARCHITECTURE

6.1 Memory Space

A memory space of 1 MByte can be accessed. Mapping of the internal data area (special function registers and internal RAM) can be specified the LOCATION instruction. The LOCATION instruction must be always executed after RESET cancellation, and must not be used more than once.

(1) When LOCATION 0 instruction is executed

- **Internal memory**

  The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784035Y	0F700H-0FFFFH	00000H-0BFFFH
μPD784036Y		00000H-0F6FFH
μPD784037Y	0F100H-0FFFFH	00000H-0F0FFH 10000H-17FFFH
μPD784038Y	0EE00H-0FFFFH	00000H-0FDFFH 10000H-1FFFFH

Caution The following areas that overlap the internal data area of the internal ROM cannot be used when the LOCATION 0 instruction is executed.

Part Number	Unusable Area
μPD784035Y	–
μPD784036Y	0F700H-0FFFFH (2304 Bytes)
μPD784037Y	0F100H-0FFFFH (3840 Bytes)
μPD784038Y	0EE00H-0FFFFH (4608 Bytes)

- **External memory**

  The external memory is accessed in external memory expansion mode.

(2) When LOCATION 0FH instruction is executed

- **Internal memory**

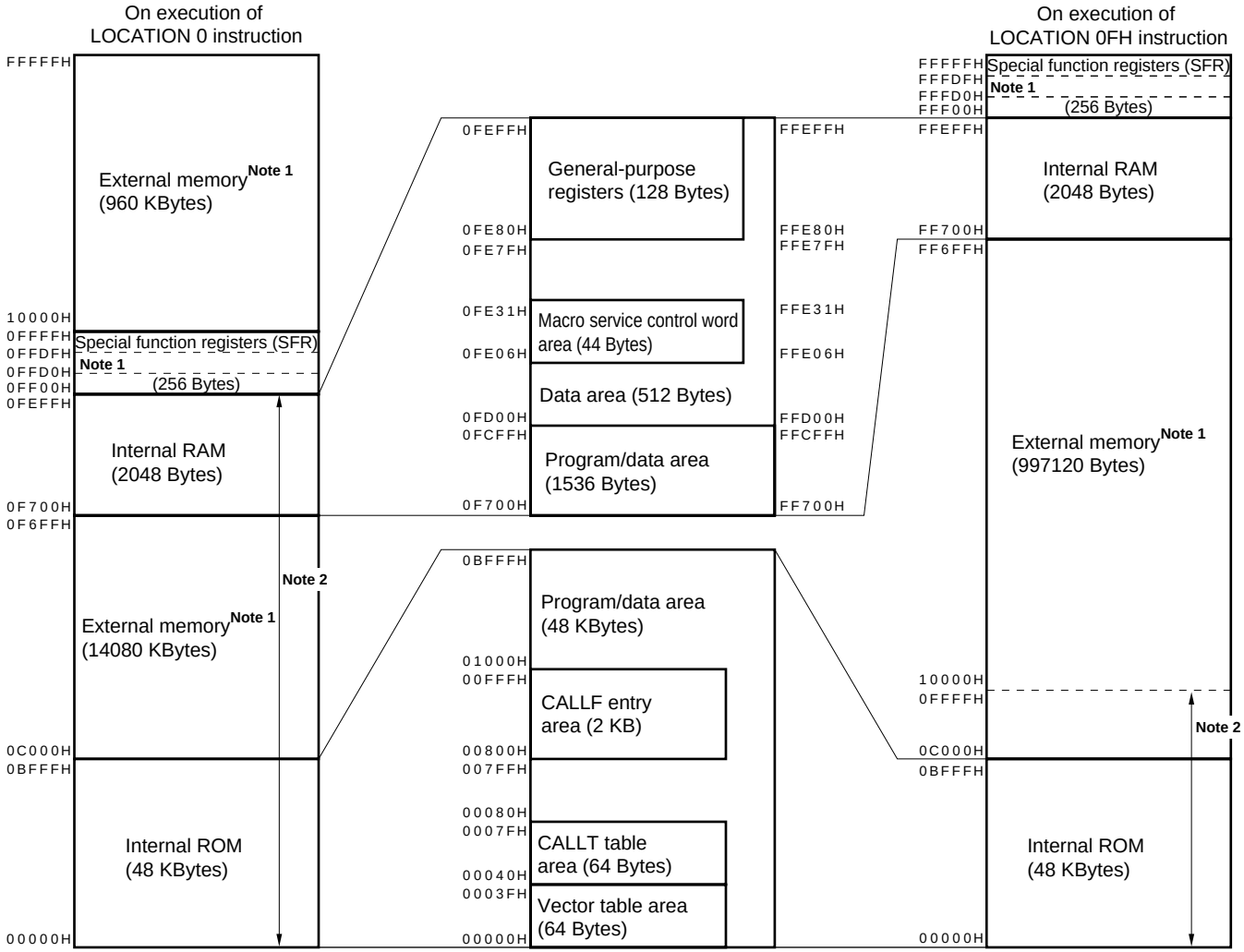
  The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784035Y	FF700H-FFFFFH	00000H-0BFFFH
μPD784036Y		00000H-0FFFFH
μPD784037Y	FF100H-FFFFFH	00000H-17FFFH
μPD784038Y	FEE00H-FFFFFH	00000H-1FFFFH

- **External memory**

  The external memory is accessed in external memory expansion mode.

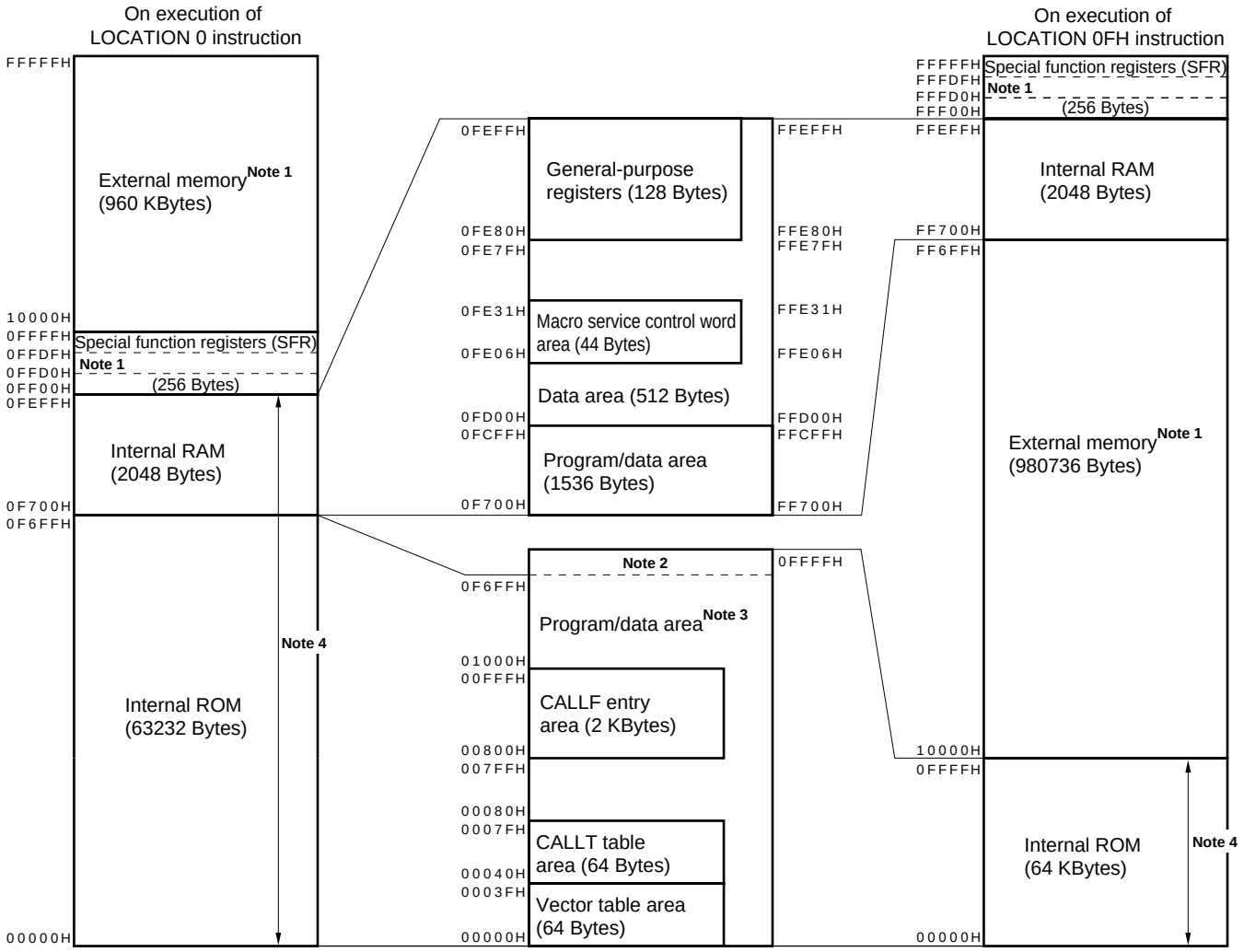
Figure 6-1. Memory Map of μPD784035Y



Notes 1. Accessed in external memory expansion mode.

2. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

Figure 6-2. Memory Map of μPD784036Y



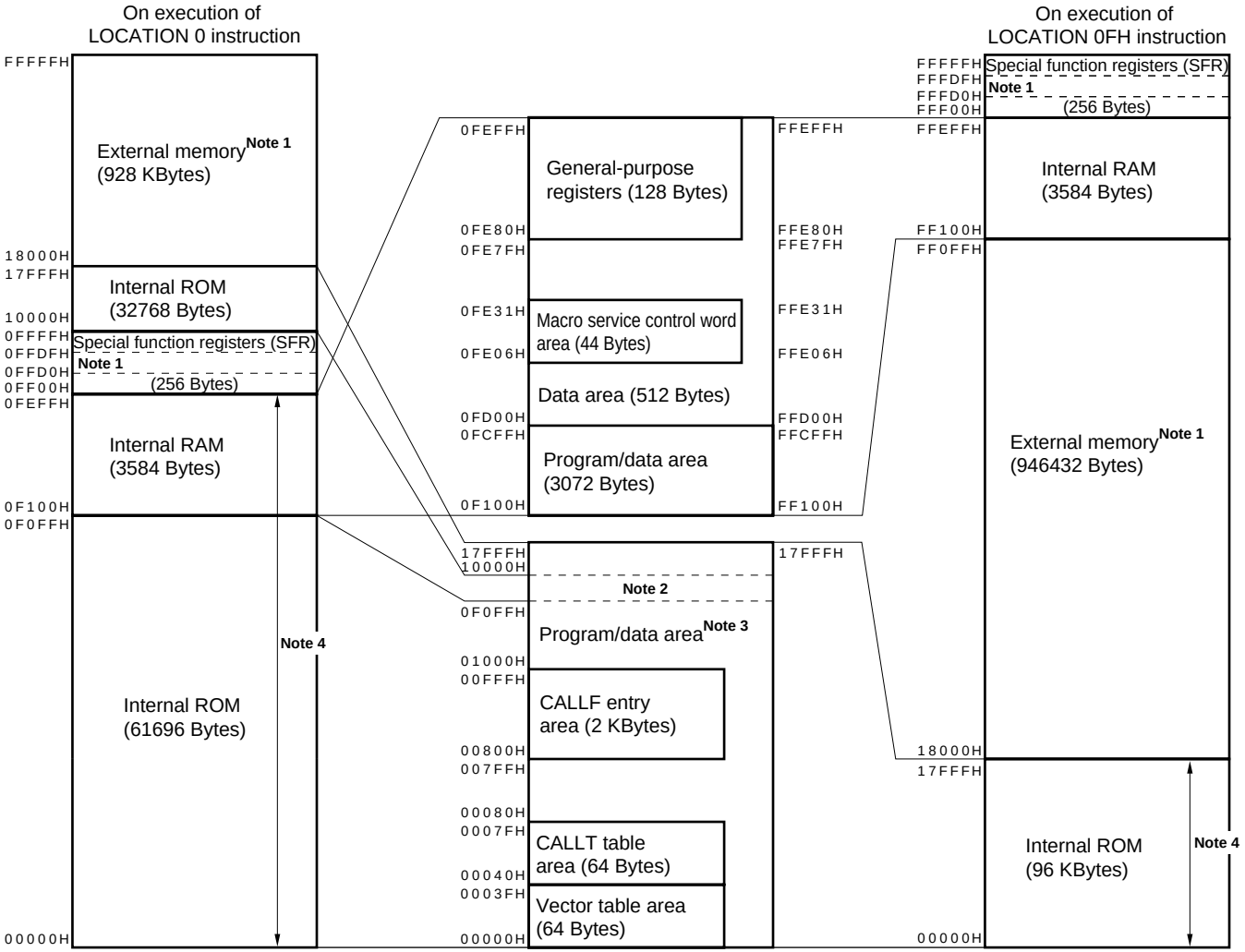
Notes 1. Accessed in external memory expansion mode.

2. This 2304-Byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.

3. On execution of LOCATION 0 instruction: 63232 Bytes, on execution of LOCATION 0FH instruction: 65536 Bytes

4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

Figure 6-3. Memory Map of μPD784037Y



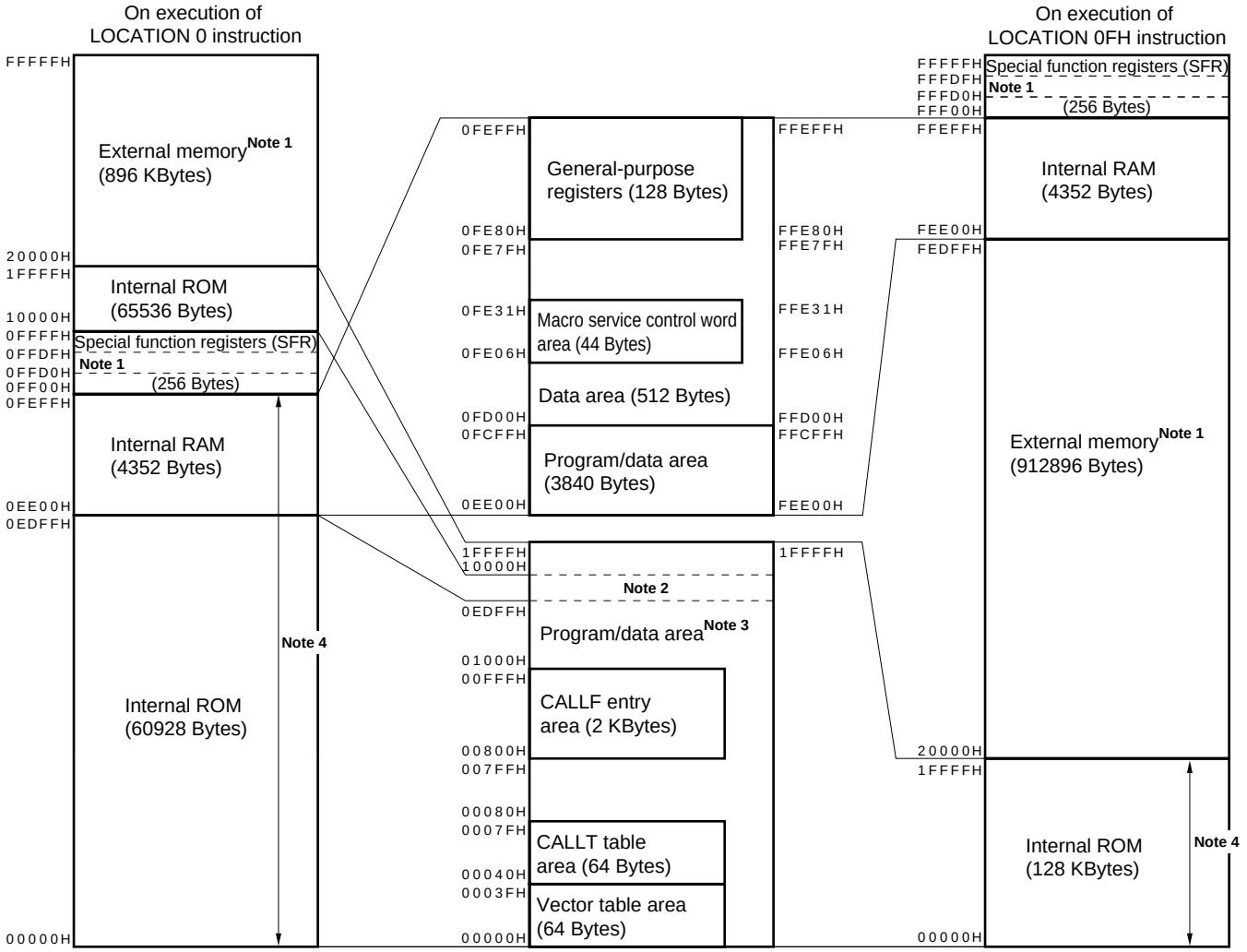
Notes 1. Accessed in external memory expansion mode.

2. This 3840-Byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.

3. On execution of LOCATION 0 instruction: 94464 Bytes, on execution of LOCATION 0FH instruction: 98304 Bytes

4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

Figure 6-4. Memory Map of μPD784038Y



Notes 1. Accessed in external memory expansion mode.

2. This 4608-Byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.

3. On execution of LOCATION 0 instruction: 126464 Bytes, on execution of LOCATION 0FH instruction: 131072 Bytes

4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

6.2 CPU Registers

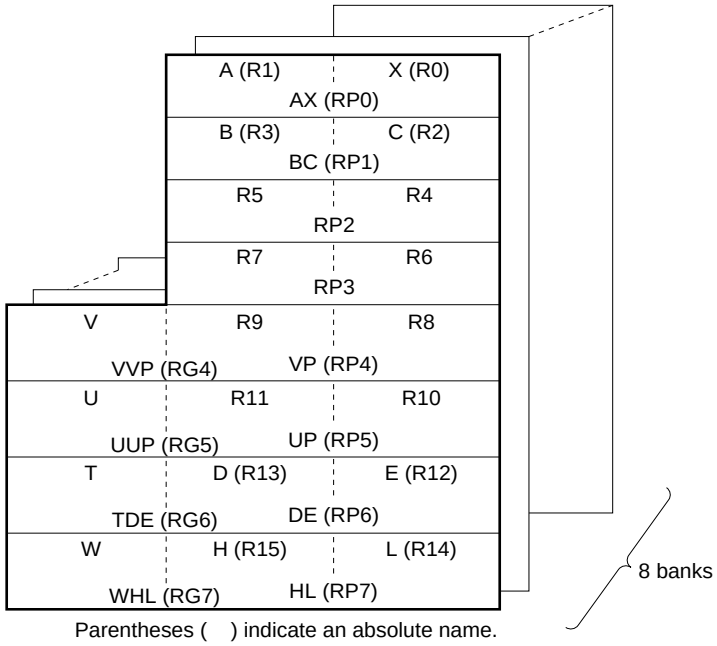
6.2.1 General-purpose registers

Sixteen 8-bit general-purpose registers are available. Two 8-bit registers can be also used in pairs as a 16-bit register. Of the 16-bit registers, four can be used in combination with an 8-bit register for address expansion as 24-bit address specification registers.

Eight banks of these registers are available which can be selected by using software or the context switching function.

The general-purpose registers except V, U, T, and W registers for address expansion are mapped to the internal RAM.

Figure 6-5. General-Purpose Register Format



Parentheses ( ) indicate an absolute name.

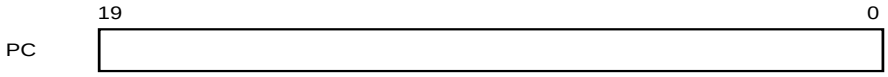
Caution Registers R4, R5, R6, R7, RP2, and RP3 can be used as X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of the PSW to 1. However, use this function only for recycling the program of the 78K/III Series.

6.2.2 Control registers

(1) Program counter (PC)

The program counter is a 20-bit register whose contents are automatically updated when the program is executed.

Figure 6-6. Program Counter (PC) Format



(2) Program status word (PSW)

This register holds the statuses of the CPU. Its contents are automatically updated when the program is executed.

Figure 6-7. Program Status Word (PSW) Format

	15	14	13	12	11	10	9	8
PSWH	UF	RBS2	RBS1	RBS0	–	–	–	–

	7	6	5	4	3	2	1	0
PSWL	S	Z	RSS[Note]	AC	IE	P/V	0	CY

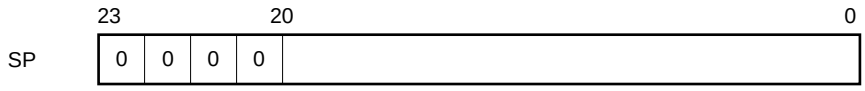
PSW

Note This flag is provided to maintain compatibility with the 78K/III Series. Be sure to clear this flag to 0, except when the software for the 78K/III Series is used.

(3) Stack pointer (SP)

This is a 24-bit pointer that holds the first address of the stack. Be sure to write 0 to the higher 4 bits of this pointer.

Figure 6-8. Stack Pointer (SP) Format



6.2.3 Special function registers (SFRs)

The special function registers, such as the mode registers and control registers of the internal peripheral hardware, are registers to which special functions are allocated. These registers are mapped to a 256-Byte space of addresses 0FF00H through 0FFFFH[Note].

Note On execution of the LOCATION 0 instruction. FFF00H through FFFFFH on execution of the LOCATION 0FH instruction.

Caution Do not access an address in this area to which no SFR is allocated. If such an address is accessed by mistake, the μPD784038Y may be in the deadlock status. This deadlock status can be cleared only by inputting the RESET signal.

Table 6-1 lists the special function registers (SFRs). The meanings of the symbols in this table are as follows:

- Symbol ..... Symbol indicating an SFR. This symbol is reserved for NEC's assembler (RA78K4). It can be used as an sfr variable by the #pragma sfr command with the C compiler (CC78K4).

- R/W ..... Indicates whether the SFR is read-only, write-only, or read/write.
  R/W : Read/write
  R : Read-only
  W : Write-only

- Bit units for manipulation .. Bit units in which the value of the SFR can be manipulated.
  SFRs that can be manipulated in 16-bit units can be described as the operand sfrp of an instruction. To specify the address of this SFR, describe an even address.
  SFRs that can be manipulated in 1-bit units can be described as the operand of a bit manipulation instruction.

- After reset ..... Indicates the status of the register when the $\overline{\text{RESET}}$ signal has been input.

Table 6-1. Special Function Registers (SFRs)

Address[Note]	Special Function Register (SFR) Name	Symbol		R/W	Bit units for manipulation			After reset
					1 bit	8 bits	16 bits	
0FF00H	Port 0	P0		R/W	○	○	–	Undefined
0FF01H	Port 1	P1			○	○	–	
0FF02H	Port 2	P2		R	○	○	–	
0FF03H	Port 3	P3		R/W	○	○	–	
0FF04H	Port 4	P4			○	○	–	
0FF05H	Port 5	P5			○	○	–	
0FF06H	Port 6	P6			○	○	–	00H
0FF07H	Port 7	P7			○	○	–	Undefined
0FF0EH	Port 0 buffer register L	P0L			○	○	–	
0FF0FH	Port 0 buffer register H	P0H			○	○	–	
0FF10H	Compare register (timer/counter 0)	CR00			–	–	○	
0FF12H	Capture/compare register (timer/counter 0)	CR01			–	–	○	
0FF14H	Compare register L (timer/counter 1)	CR10	CR10W		–	○	○	
0FF15H	Compare register H (timer/counter 1)	–			–	–		
0FF16H	Capture/compare register L (timer/counter 1)	CR11	CR11W		–	○	○	
0FF17H	Capture/compare register H (timer/counter 1)	–			–	–		
0FF18H	Compare register L (timer/counter 2)	CR20	CR20W		–	○	○	
0FF19H	Compare register H (timer/counter 2)	–			–	–		
0FF1AH	Capture/compare register L (timer/counter 2)	CR21	CR21W		–	○	○	
0FF1BH	Capture/compare register H (timer/counter 2)	–			–	–		
0FF1CH	Compare register L (timer 3)	CR30	CR30W		–	○	○	
0FF1DH	Compare register H (timer 3)	–			–	–		
0FF20H	Port 0 mode register	PM0			○	○	–	FFH
0FF21H	Port 1 mode register	PM1			○	○	–	
0FF23H	Port 3 mode register	PM3			○	○	–	
0FF24H	Port 4 mode register	PM4			○	○	–	
0FF25H	Port 5 mode register	PM5			○	○	–	
0FF26H	Port 6 mode register	PM6			○	○	–	
0FF27H	Port 7 mode register	PM7			○	○	–	
0FF2EH	Real-time output port control register	RTPC			○	○	–	00H
0FF30H	Capture/compare control register 0	CRC0			–	○	–	10H
0FF31H	Timer output control register	TOC			○	○	–	00H
0FF32H	Capture/compare control register 1	CRC1			–	○	–	
0FF33H	Capture/compare control register 2	CRC2			–	○	–	10H

Note When the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, "F0000H" is added to this value.

Address[Note 1]	Special Function Register (SFR) Name	Symbol		R/W	Bit units for manipulation			After reset
					1 bit	8 bits	16 bits	
0FF36H	Capture register (timer/counter 0)	CR02		R	–	–	○	0000H
0FF38H	Capture register L (timer/counter 1)	CR12	CR12W		–	○	○	
0FF39H	Capture register H (timer/counter 1)	–			–	–		
0FF3AH	Capture register L (timer/counter 2)	CR22	CR22W		–	○	○	
0FF3BH	Capture register H (timer/counter 2)	–			–	–		
0FF41H	Port 1 mode control register	PMC1		R/W	○	○	–	00H
0FF43H	Port 3 mode control register	PMC3			○	○	–	
0FF4EH	Pull-up resistor option register	PUO			○	○	–	
0FF50H	Timer register 0	TM0		R	–	–	○	0000H
0FF51H					–	–		
0FF52H	Timer register 1	TM1	TM1W		–	○	○	
0FF53H		–			–	–		
0FF54H	Timer register 2	TM2	TM2W		–	○	○	
0FF55H		–			–	–		
0FF56H	Timer register 3	TM3	TM3W		–	○	○	
0FF57H		–			–	–		
0FF5CH	Prescaler mode register 0	PRM0		R/W	–	○	–	11H
0FF5DH	Timer control register 0	TMC0			○	○	–	00H
0FF5EH	Prescaler mode register 1	PRM1			–	○	–	11H
0FF5FH	Timer control register 1	TMC1			○	○	–	00H
0FF60H	D/A conversion value setting register 0	DACS0			–	○	–	
0FF61H	D/A conversion value setting register 1	DACS1			–	○	–	
★ 0FF62H	D/A converter mode register	DAM			○	○	–	03H
0FF68H	A/D converter mode register	ADM			○	○	–	00H
0FF6AH	A/D conversion result register	ADCR		R	–	○	–	Undefined
★ 0FF70H	PWM control register	PWMC		R/W	○	○	–	05H
0FF71H	PWM prescaler register	PWPR			–	○	–	00H
0FF72H	PWM modulo register 0	PWM0			–	–	○	Undefined
0FF74H	PWM modulo register 1	PWM1			–	–	○	
0FF7DH	One-shot pulse output control register	OSPC			○	○	–	00H
0FF80H	I^2C bus control register	IICC			○	○	–	
0FF81H	Prescaler mode register for serial clock	SPRM			–	○	–	04H
0FF82H	Clocked serial interface mode register	CSIM			○	○	–	00H
0FF83H	Slave address register	SVA		R/W[Note 2]	○[Note 3]	○	–	01H

Notes 1. When the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, "F0000H" is added to this value.

2. Bit 0 is read-only.

3. Only bit 0 can be manipulated in bit units.

Address[Note 1]	Special Function Register (SFR) Name	Symbol	R/W	Bit units for manipulation			After reset
				1 bit	8 bits	16 bits	
0FF84H	Clocked serial interface mode register 1	CSIM1	R/W	○	○	–	00H
0FF85H	Clocked serial interface mode register 2	CSIM2		○	○	–	
0FF86H	Serial shift register	SIO		–	○	–	
0FF88H	Asynchronous serial interface mode register	ASIM		○	○	–	
0FF89H	Asynchronous serial interface mode register 2	ASIM2		○	○	–	
0FF8AH	Asynchronous serial interface status register	ASIS	R	○	○	–	
0FF8BH	Asynchronous serial interface status register 2	ASIS2		○	○	–	
0FF8CH	Serial receive buffer: UART0	RXB		–	○	–	Undefined
	Serial transmit shift register: UART0	TXS	W	–	○	–	
	Serial shift register: IOE1	SIO1	R/W	–	○	–	
0FF8DH	Serial receive buffer: UART2	RXB2	R	–	○	–	
	Serial transmit shift register: UART2	TXS2	W	–	○	–	
	Serial shift register: IOE2	SIO2	R/W	–	○	–	
0FF90H	Baud rate generator control register	BRGC		–	○	–	00H
0FF91H	Baud rate generator control register 2	BRGC2		–	○	–	
0FFA0H	External interrupt mode register 0	INTM0		○	○	–	
0FFA1H	External interrupt mode register 1	INTM1		○	○	–	
0FFA4H	Sampling clock select register	SCS0		–	○	–	
0FFA8H	In-service priority register	ISPR	R	○	○	–	
0FFAAH	Interrupt mode control register	IMC	R/W	○	○	–	80H
0FFACH	Interrupt mask register 0L	MK0L | MK0		○	○	○	FFFFH
0FFADH	Interrupt mask register 0H	MK0H		○	○		
0FFAEH	Interrupt mask register 1L	MK1L		○	○	–	FFH
0FFC0H	Standby control register	STBC		–	○[Note 2]	–	30H
0FFC2H	Watchdog timer mode register	WDM		–	○[Note 2]	–	00H
0FFC4H	Memory expansion mode register	MM		○	○	–	20H
0FFC5H	Hold mode register	HLDM		○	○	–	00H
0FFC6H	Clock output mode register	CLOM		○	○	–	
0FFC7H	Programmable wait control register 1	PWC1		–	○	–	AAH
0FFC8H	Programmable wait control register 2	PWC2		–	–	○	AAAAH

Notes 1. When the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, "F0000H" is added to this value.

2. Data can be written by using only a dedicated instruction such as "MOV STBC, #byte instruction" and "MOV WDM, #byte instruction", and cannot be written with any other instructions.

Address[Note]	Special Function Register (SFR) Name	Symbol	R/W	Bit units for manipulation			After reset
				1 bit	8 bits	16 bits	
0FFCCH	Refresh mode register	RFM	R/W	○	○	–	00H
0FFCDH	Refresh area specification register	RFA		○	○	–	
0FFCFH	Oscillation stabilization time specification register	OSTS		–	○	–	
0FFD0H-0FFDFH	External SFR area	–		○	○	–	–
0FFE0H	Interrupt control register (INTP0)	PIC0		○	○	–	43H
0FFE1H	Interrupt control register (INTP1)	PIC1		○	○	–	
0FFE2H	Interrupt control register (INTP2)	PIC2		○	○	–	
0FFE3H	Interrupt control register (INTP3)	PIC3		○	○	–	
0FFE4H	Interrupt control register (INTC00)	CIC00		○	○	–	
0FFE5H	Interrupt control register (INTC01)	CIC01		○	○	–	
0FFE6H	Interrupt control register (INTC10)	CIC10		○	○	–	
0FFE7H	Interrupt control register (INTC11)	CIC11		○	○	–	
0FFE8H	Interrupt control register (INTC20)	CIC20		○	○	–	
0FFE9H	Interrupt control register (INTC21)	CIC21		○	○	–	
0FFEAH	Interrupt control register (INTC30)	CIC30		○	○	–	
0FFEBH	Interrupt control register (INTP4)	PIC4		○	○	–	
0FFECH	Interrupt control register (INTP5)	PIC5		○	○	–	
0FFEDH	Interrupt control register (INTAD)	ADIC		○	○	–	
0FFEEH	Interrupt control register (INTSER)	SERIC		○	○	–	
0FFEFH	Interrupt control register (INTSR)	SRIC		○	○	–	
	Interrupt control register (INTCSI1)	CSIIC1		○	○	–	
0FFF0H	Interrupt control register (INTST)	STIC		○	○	–	
0FFF1H	Interrupt control register (INTCSI)	CSIIC		○	○	–	
0FFF2H	Interrupt control register (INTSER2)	SERIC2		○	○	–	
0FFF3H	Interrupt control register (INTSR2)	SRIC2		○	○	–	
	Interrupt control register (INTCSI2)	CSIIC2		○	○	–	
0FFF4H	Interrupt control register (INTST2)	STIC2		○	○	–	
0FFF5H	Interrupt control register (INTSPC)	SPCIC		○	○	–	

Note When the LOCATION 0 instruction is executed. When the LOCATION 0FH instruction is executed, "F0000H" is added to this value.

7. PERIPHERAL HARDWARE FUNCTIONS

7.1 Ports

The ports shown in Figure 7-1 are provided to make various control operations possible. Table 7-1 shows the function of each port. Ports 0 through 6 can be connected to internal pull-up resistors by software when inputting.

Figure 7-1. Port Configuration

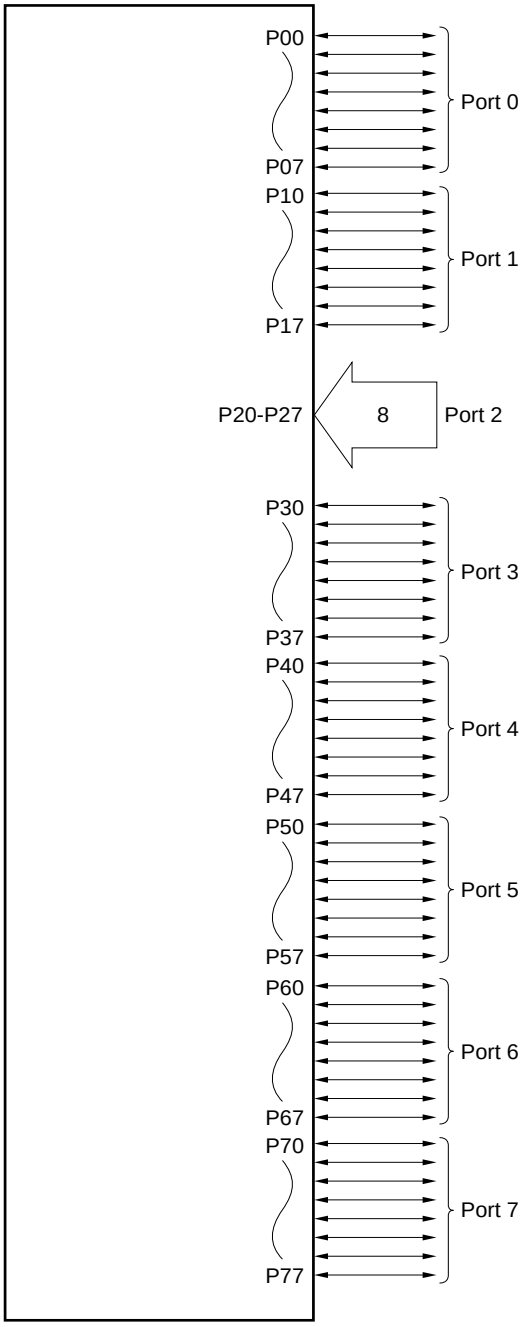


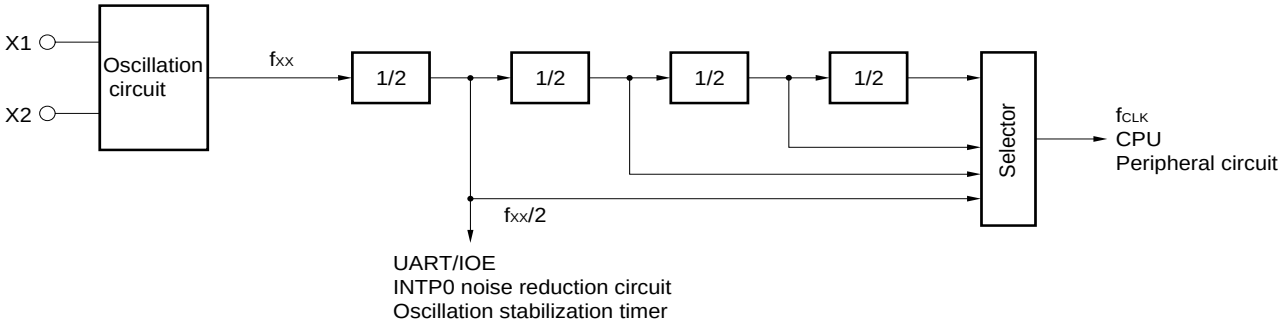
Table 7-1. Port Functions

Port Name	Pin Name	Function	Specification of Pull-up Resistor Connection by Software
Port 0	P00 to P07	• Can be set in input or output mode in 1-bit units. • Can operate as 4-bit real-time output port (P00 through P03 and P04 through P07) • Can drive transistor.	All port pins in input mode
Port 1	P10 to P17	• Can be set in input or output mode in 1-bit units. • Can drive LEDs.	All port pins in input mode
Port 2	P20 to P27	• Input port	In 6-bit units (P22 through P27)
Port 3	P30 to P37	• Can be set in input or output mode in 1-bit units.	All port pins in input mode
Port 4	P40 to P47	• Can be set in input or output mode in 1-bit units. • Can drive LEDs.	All port pins in input mode
Port 5	P50 to P57	• Can be set in input or output mode in 1-bit units. • Can drive LEDs.	All port pins in input mode
Port 6	P60 to P67	• Can be set in input or output mode in 1-bit units.	All port pins in input mode
Port 7	P70 to P77	• Can be set in input or output mode in 1-bit units.	–

7.2 Clock Generation Circuit

An on-chip clock generation circuit necessary for operation is provided. This clock generation circuit has a divider circuit. If high-speed operation is not necessary, the internal operating frequency can be lowered by the divider circuit to reduce the current consumption.

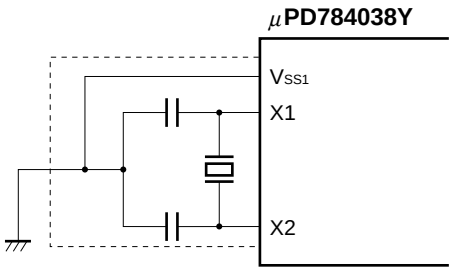
Figure 7-2. Block Diagram of Clock Generation Circuit



Remark f_{XX} : oscillation frequency or external clock input
f_{CLK}: internal operating frequency

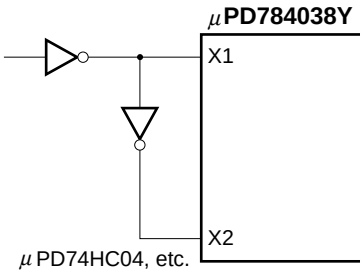
Figure 7-3. Example of Using Oscillation Circuit

(1) Crystal/ceramic oscillation

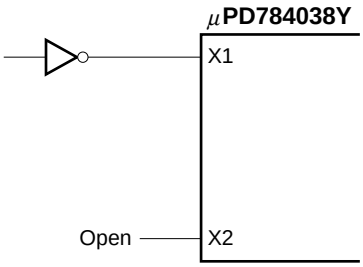


(2) External clock

- **EXTC bit of OSTS = 1**



- **EXTC bit of OSTS = 0**



Caution When using the clock oscillation circuit, wire the dotted portion in the above figure as follows to avoid adverse influences of wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the potential at the ground point of the capacitor in the oscillation circuit the same as V_{SS1}. Do not ground to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

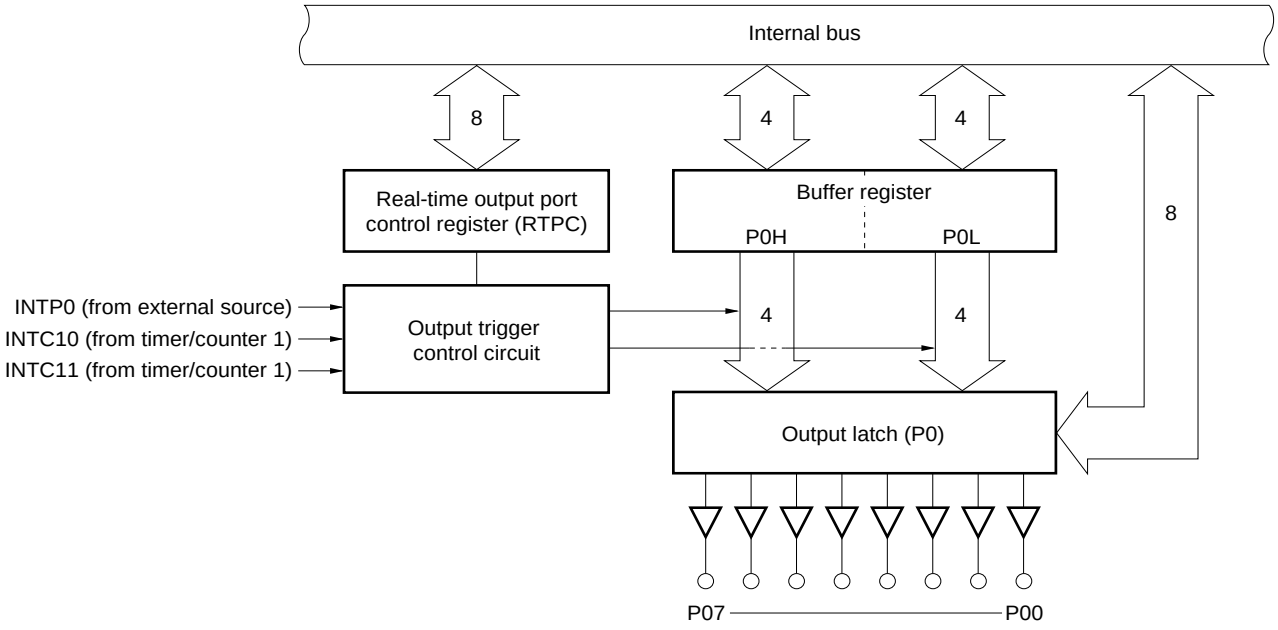
7.3 Real-Time Output Port

The real-time output port outputs data stored in a buffer in synchronization with the coincidence interrupt generated by timer/counter 1 or with an external interrupt. As a result, pulses without jitter can be output.

The real-time output port is therefore ideal for applications where arbitrary patterns must be output at specific intervals (such as open loop control of a stepping motor).

The real-time output port mainly consists of port 0 and port 0 buffer registers (P0H and P0L) as shown in Figure 7-4.

Figure 7-4. Block Diagram of Real-Time Output Port



7.4 Timer/Counter

Three units of timers/counters and one unit of timer are provided.

Because a total of seven interrupt requests are supported, these timers/counters and timer can be used as seven units of timers/counters.

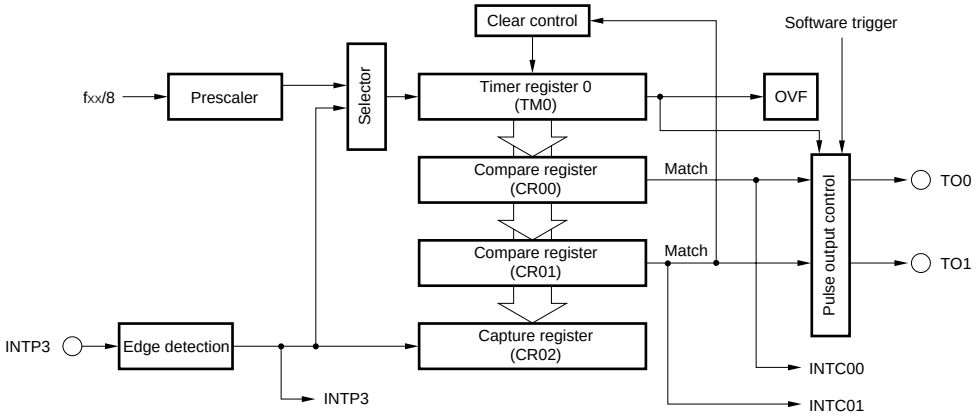
Table 7-2. Operations of Timers/Counters

Item \ Name		Timer/Counter 0	Timer/Counter 1	Timer/Counter 2	Timer 3
Count width	8 bits	–	○	○	○
	16 bits	○	○	○	○
Operation mode	Interval timer	2ch	2ch	2ch	1ch
	External event counter	○	○	○	–
	One-shot timer	–	–	○	–
Function	Timer output	2ch	–	2ch	–
	Toggle output	○	–	○	–
	PWM/PPG output	○	–	○	–
	One-shot pulse output[Note]	○	–	–	–
	Real-time output	–	○	–	–
	Pulse width measurement	1 input	1 input	2 inputs	–
	Number of interrupt requests	2	2	2	1

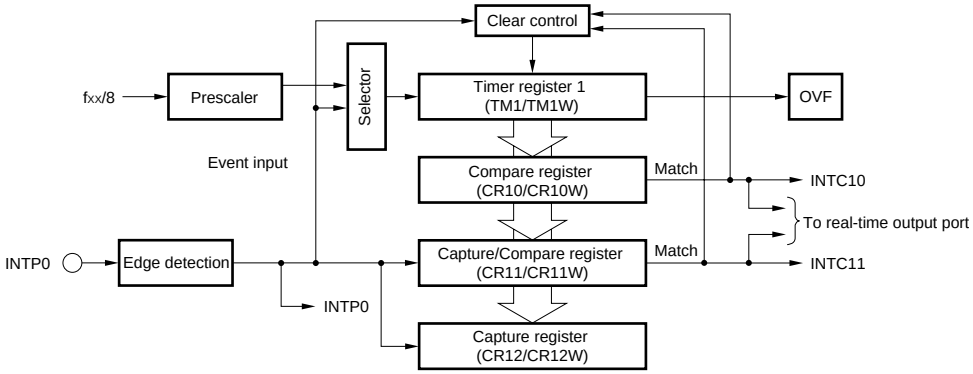
Note The one-shot pulse output function makes a pulse output level active by software and inactive by hardware (interrupt request signal).
This function is different in nature from the one-shot timer function of timer/counter 2.

Figure 7-5. Block Diagram of Timers/Counters

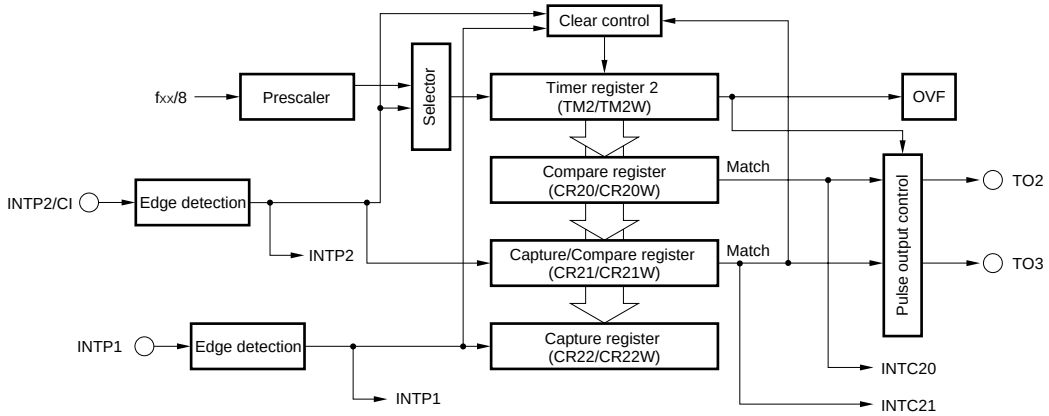
Timer/counter 0



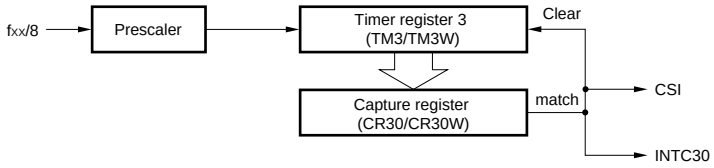
Timer/counter 1



Timer/counter 2



Timer 3

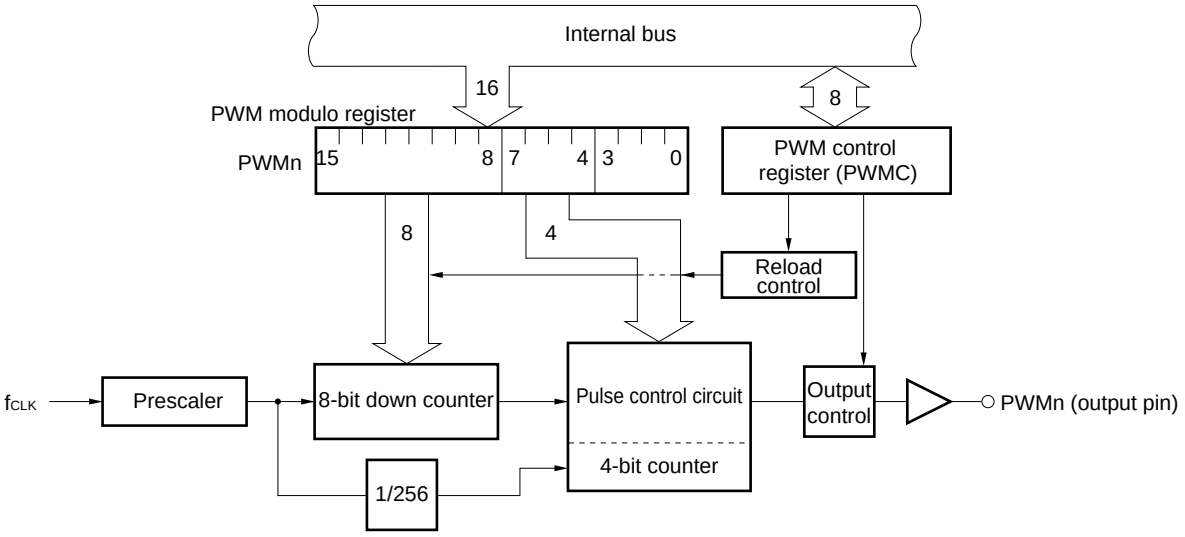


Remark OVF: overflow flag

7.5 PWM Output (PWM0, PWM1)

Two channels of PWM (pulse width modulation) output circuits with a resolution of 12 bits and a repeat frequency of 62.5 kHz (f_{CLK} = 16 MHz) are provided. Both these PWM output channels can select a high or low level as the active level. These outputs are ideal for controlling the speed of a DC motor.

Figure 7-6. Block Diagram of PWM Output Unit



Remark n = 0 or 1

7.6 A/D Converter

An analog-to-digital (A/D) converter with eight multiplexed inputs (ANI0 through ANI7) is provided.

This A/D converter is of successive approximation type. The result of conversion is retained by an 8-bit A/D conversion result register (ADCR). Therefore, high-speed, high-accuracy conversion can be performed (conversion time: approx. 7.5 μs at f_{CLK} = 16 MHz).

A/D conversion can be started in either of the following two modes:

- Hardware start: Conversion is started by trigger input (INTP5).
- Software start: Conversion is started by setting a bit of the A/D converter mode register (ADM).

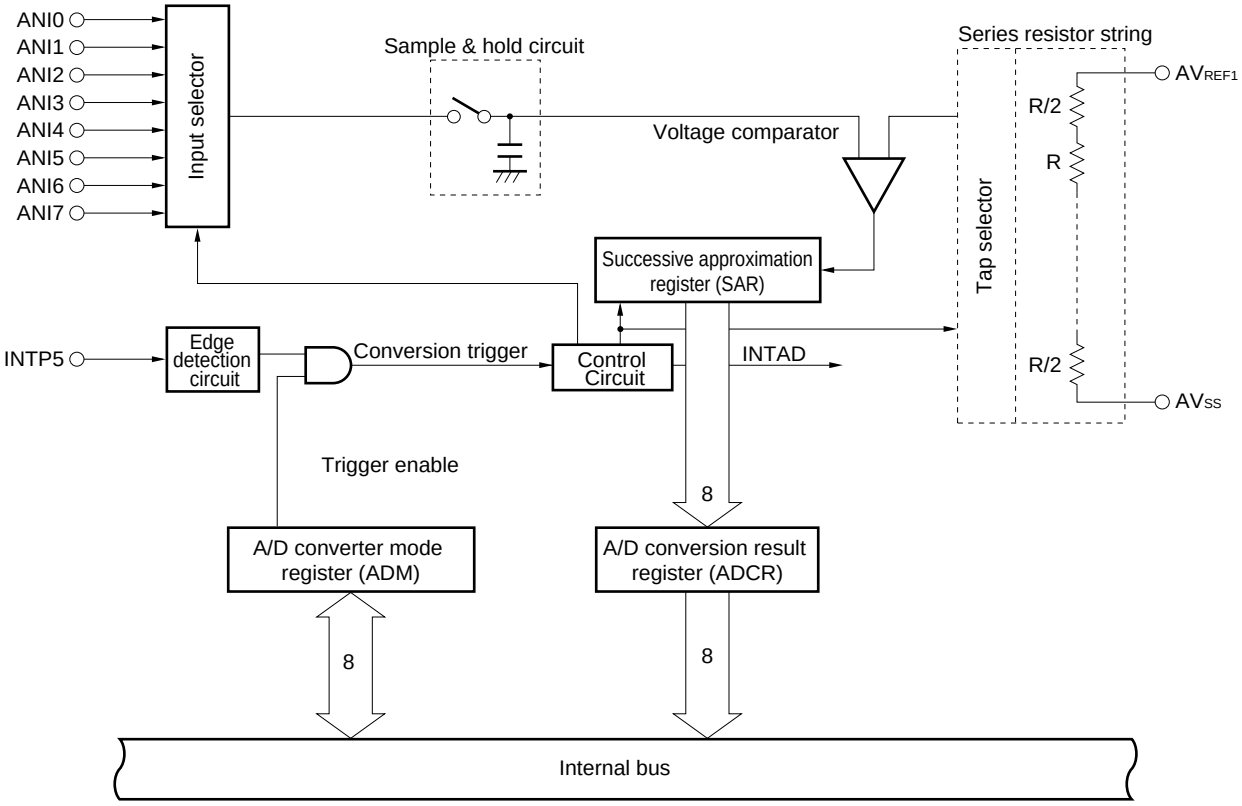
After started, the A/D converter operates in the following modes:

- Scan mode: Two or more analog inputs are sequentially selected, and data to be converted are obtained from all the input pins.
- Select mode: Only one analog input pin is used to continuously obtain converted values.

These operation modes and whether starting or stopping the A/D converter are specified by the ADM.

When the result of conversion is transferred to the ADCR, interrupt request INTAD is generated. By using this request and macro service, the converted values can be successively transferred to the memory.

Figure 7-7. Block Diagram of A/D Converter



7.7 D/A Converter

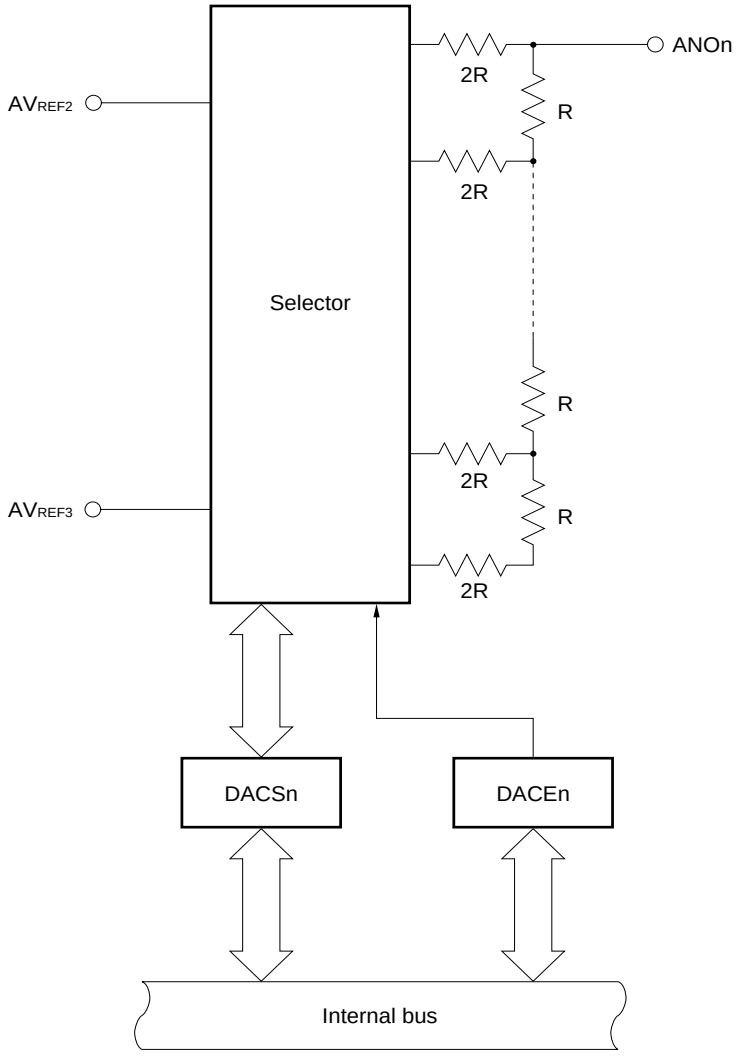
Two circuits of digital-to-analog (D/A) converters are provided. These D/A converters are of voltage output type and have a resolution of 8 bits.

The conversion method is of R-2R resistor ladder type. By writing a value to be output to an 8-bit D/A conversion value setting register (DACSn: n = 0 or 1), an analog value is output to the ANOn (n = 0 or 1) pin. The output voltage range is determined by the voltage applied across the AV_{REF2} and AV_{REF3} pins.

Because the output impedance is high, no current can be extracted from the output. If the impedance of the load is low, insert a buffer amplifier between the load and output pin.

The ANOn pin goes into a high-impedance state while the $\overline{\text{RESET}}$ signal is low. When the $\overline{\text{RESET}}$ signal is deasserted, DACSn is cleared to 0.

Figure 7-8. Block Diagram of D/A Converter



Remark n = 0 or 1

7.8 Serial Interface

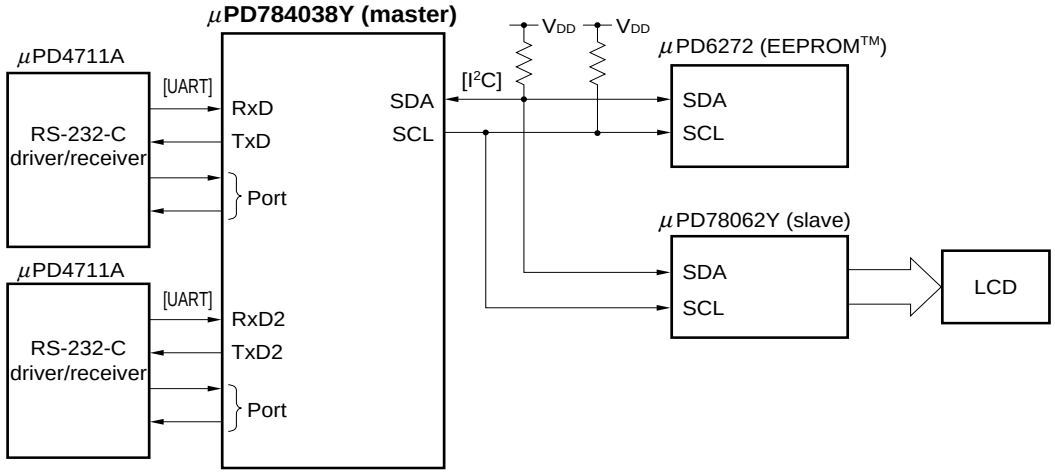
Three independent serial interface channels are provided.

- Asynchronous serial interface (UART)/3-wire serial I/O (IOE) × 2
- Clocked serial interface (CSI) × 1
  - 3-wire serial I/O (IOE)
  - 2-wire serial I/O (IOE)
  - I^2C bus interface (I^2C)

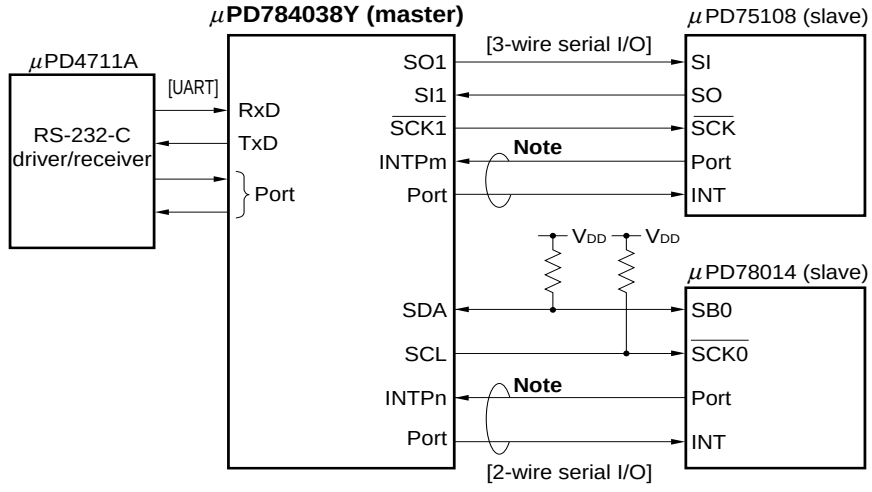
Therefore, communication with an external system and local communication within the system can be simultaneously executed (refer to Figure 7-9).

Figure 7-9. Example of Serial Interface

(a) UART + I^2C



(b) UART + 3-wire serial I/O + 2-wire serial I/O



Note Handshake line

7.8.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE)

Two channels of serial interfaces that can select an asynchronous serial interface mode and 3-wire serial I/O mode are provided.

(1) Asynchronous serial interface mode

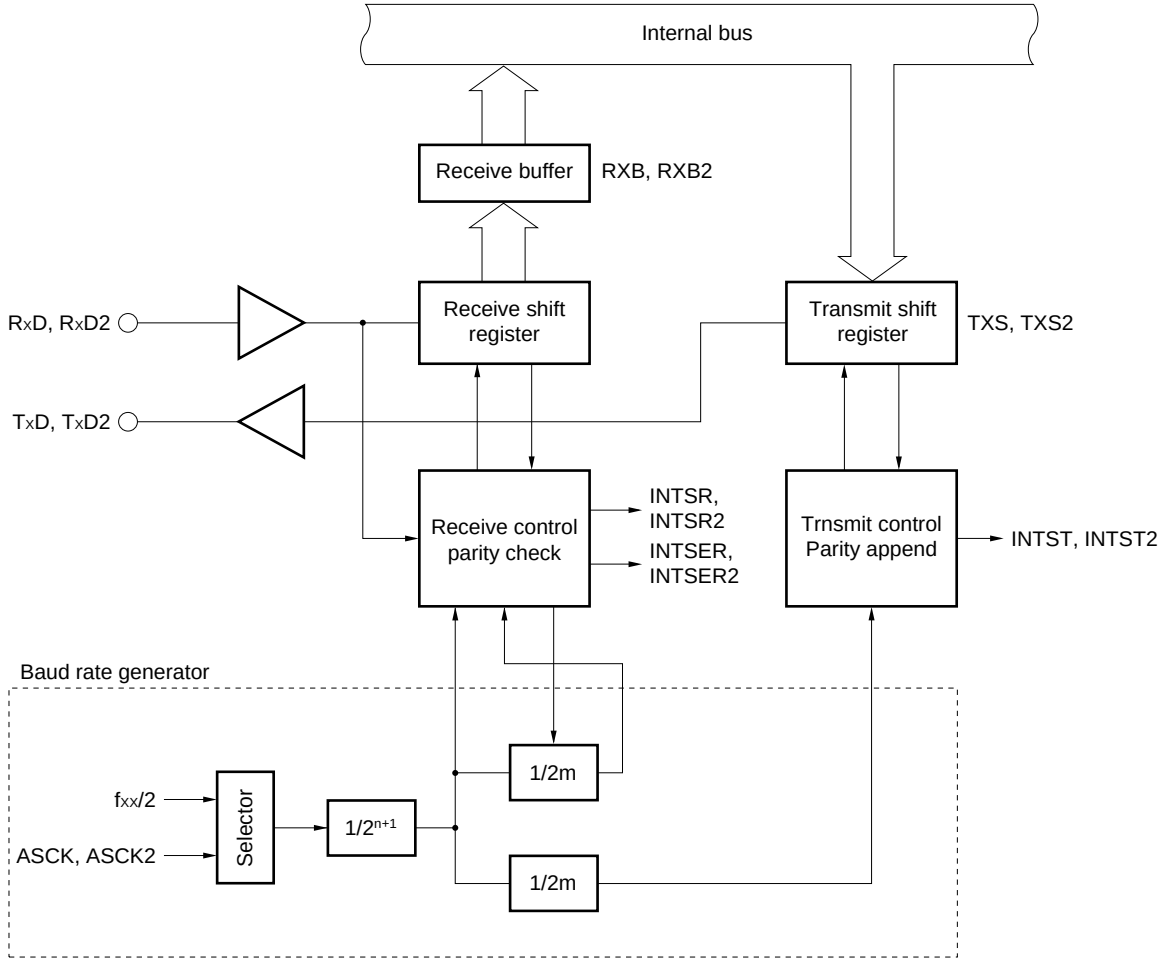
In this mode, data of 1 byte following the start bit is transferred or received.

Because an on-chip baud rate generator is provided, a wide range of baud rates can be set.

Moreover, the clock input to the ASCK pin can be divided to define a baud rate.

When the baud rate generator is used, a baud rate conforming to the MIDI standard (31.25 kbps) can be also obtained.

Figure 7-10. Block Diagram in Asynchronous Serial Interface Mode



Remark f_{XX}: oscillation frequency or external clock input
n = 0 through 11
m = 16 through 30

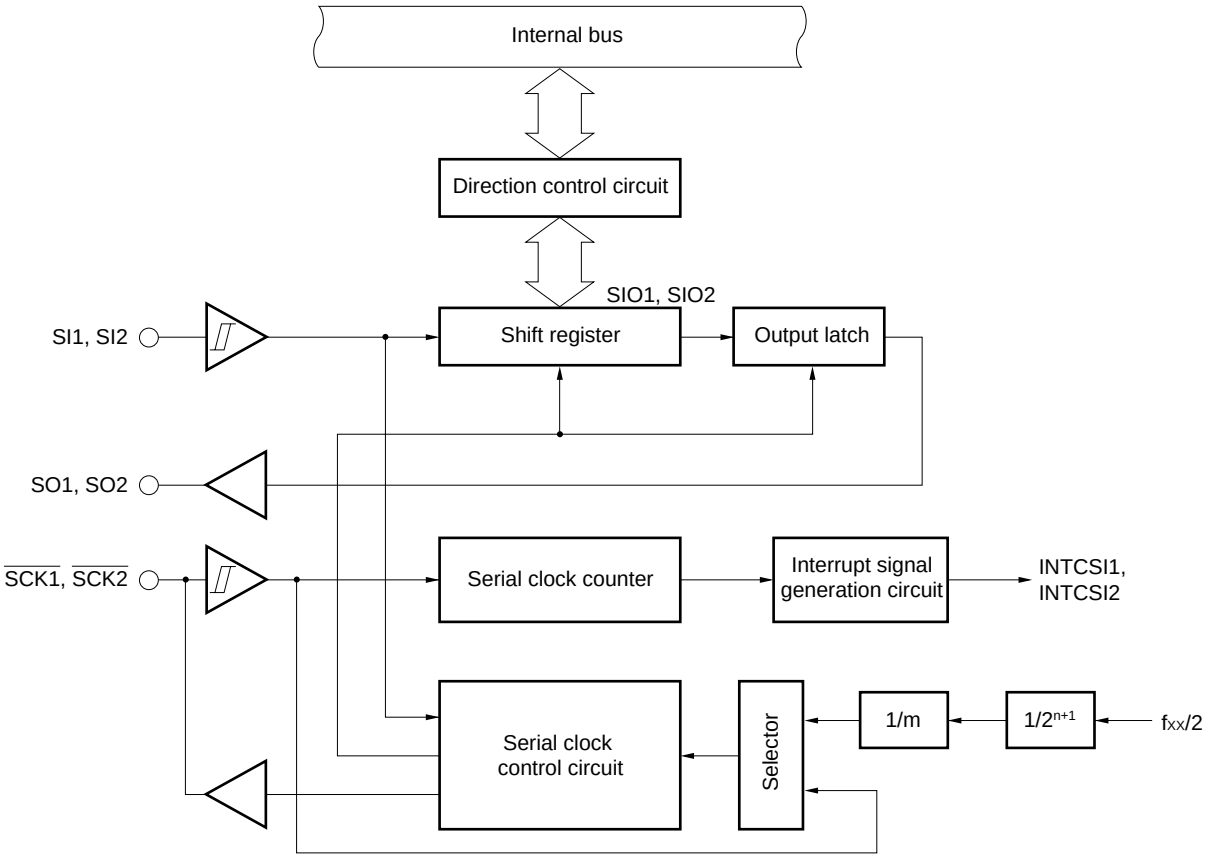
(2) 3-wire serial I/O mode

In this mode, the master device starts transfer by making the serial clock active and transfers 1-byte data in synchronization with this clock.

This mode is used to communicate with a device having the conventional clocked serial interface. Basically, communication is established by using three lines: one serial clock ($\overline{SCK}$) and two serial data (SI and SO) lines.

★ Generally, a handshake line is necessary to check the communication state.

Figure 7-11. Block Diagram in 3-wire Serial I/O Mode

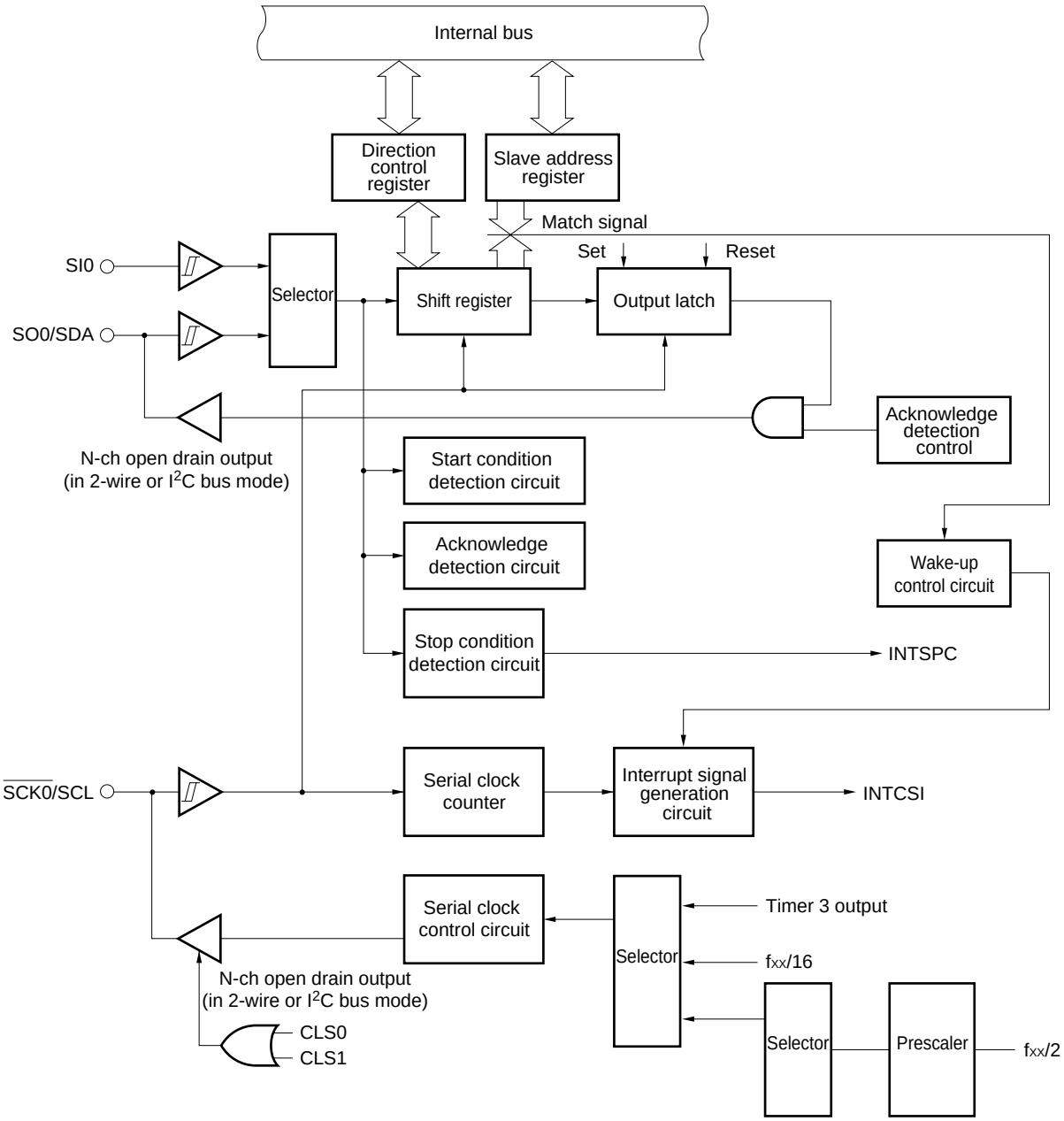


Remark f_{XX}: oscillation frequency or external clock input
n = 0 through 11
m = 1 or 16 through 30

7.8.2 Clocked serial interface (CSI)

In this mode, the master device starts transfer by making the serial clock active and communicates 1-byte data in synchronization with this clock.

Figure 7-12. Block Diagram of Clocked Serial Interface



Remark f_{XX}: oscillation frequency or external clock input

(1) 3-wire serial I/O mode

This mode is to communicate with devices having the conventional clocked serial interface.

Basically, communication is established in this mode with three lines: one serial clock ($\overline{SCK0}$) and two serial data (SI0 and SO0) lines.

Generally, a handshake line is necessary to check the communication status.

(2) 2-wire serial I/O mode

This mode is to transfer 8-bit data by using two lines: serial clock (SCL) and serial data bus (SDA).

Generally, a handshake line is necessary to check the communication status.

(3) I^2C (Inter IC) bus mode

This mode is to communicate with devices conforming to the I^2C bus format.

This mode is to transfer 8-bit data with two or more devices by using two lines: serial clock (SCL) and serial data bus (SDA).

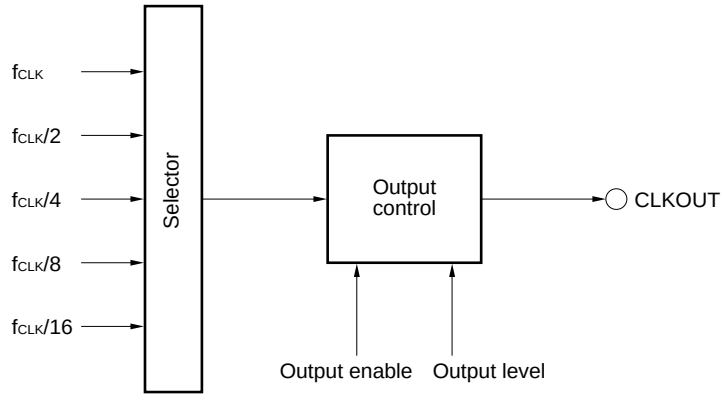
During transfer, a “start condition”, “data”, and “stop condition” can be output onto the serial data bus. During reception, these data can be automatically detected by hardware.

7.9 Clock Output Function

The operating clock of the CPU can be divided and output to an external device. The pin that outputs the clock can also be used as a 1-bit port.

When this function is used, the local bus interface cannot be used because the ASTB and CLKOUT pins are multiplexed.

Figure 7-13. Block Diagram of Clock Output Function



7.10 Edge Detection Function

The interrupt input pins (NMI and INTP0 through INTP5) are used not only to input interrupt requests but also to input trigger signals to the internal hardware units. Because these pins operate at an edge of the input signal, they have a function to detect an edge. Moreover, a noise reduction circuit is also provided to prevent erroneous detection due to noise.

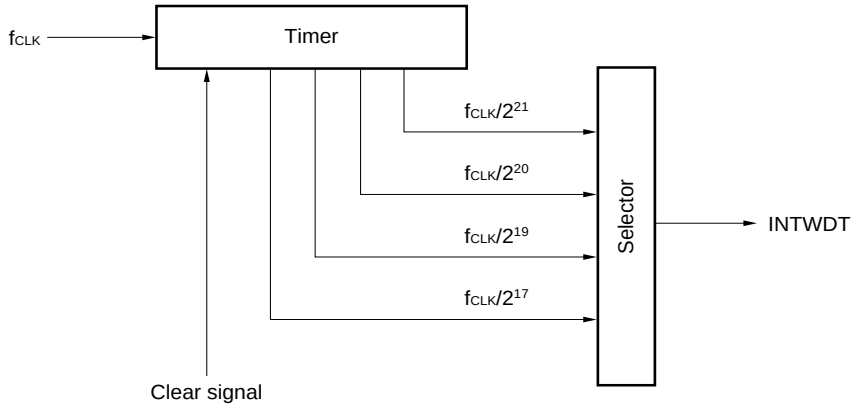
Pin Name	Detectable Edge	Noise Reduction
NMI	Either of rising or falling edge	By analog delay
INTP0-INTP3	Either or both of rising and falling edges	By clock sampling[Note]
INTP4, INTP5		By analog delay

Note INTP0 can select a sampling clock.

7.11 Watchdog Timer

A watchdog timer is provided to detect a hang up of the CPU. This watchdog timer generates a non-maskable interrupt unless it is cleared by software within a specified interval time. Once enabled to operate, the watchdog timer cannot be stopped by software. Whether the interrupt by the watchdog timer or the interrupt input from the NMI pin takes precedence can be specified.

Figure 7-14. Block Diagram of Watchdog Timer



8. INTERRUPT FUNCTION

As the servicing in response to an interrupt request, the three types shown in Table 8-1 can be selected by program.

Table 8-1. Servicing of Interrupt Request

Servicing Mode	Entity of Servicing	Servicing	Contents of PC and PSW
Vectored interrupt	Software	Branches and executes servicing routine (servicing is arbitrary).	Saves to and restores from stack.
Context switching		Automatically switches register bank, branches and executes servicing routine (servicing is arbitrary).	Saves to or restores from fixed area in register bank
Macro service	Firmware	Executes data transfer between memory and I/O (servicing is fixed)	Retained

8.1 Interrupt Sources

★ Table 8-2 shows the interrupt sources available. As shown, interrupts are generated by 24 types of sources, execution of the BRK instruction or BRKCS instruction, or an operand error.

The priority of interrupt servicing can be set to four levels, so that nesting can be controlled during interrupt servicing and that which of the two or more interrupts that simultaneously occur should be serviced first. When the macro service function is used, however, nesting always proceeds.

The default priority is the priority (fixed) of the service that is performed if two or more interrupt requests, having the same request, simultaneously generate (refer to Table 8-2).

★ **Table 8-2. Interrupt Sources**

Type	Default Priority	Source		Internal/ External	Macro service
		Name	Trigger		
Software	–	BRK instruction	Instruction execution	–	–
		BRKCS instruction			
		Operand error	If result of exclusive OR between byte of operand and byte is not FFH when “MOV STBC, #byte”, “MOV WDM, #byte”, or “LOCATION” instruction is executed		
Non-maskable	–	NMI	Detection of pin input edge	External	–
		WDT	Overflow of watchdog timer	Internal	
Maskable	0 (highest)	INTP0	Detection of pin input edge (TM1/TM1W capture trigger, TM1/TM1W event counter input)	External	○
	1	INTP1	Detection of pin input edge (TM2/TM2W capture trigger, TM2/TM2W event counter input)		
	2	INTP2	Detection of pin input edge (TM2/TM2W capture trigger , TM2/TM2W event counter input)		
	3	INTP3	Detection of pin input edge (TM0 capture trigger, TM0 event counter input)		
	4	INTC00	Generation of TM0-CR00 match signal	Internal	○
	5	INTC01	Generation of TM0-CR01 match signal		
	6	INTC10	Generation of TM1-CR10 match signal (in 8-bit operation mode) Generation of TM1W-CR10W match signal (in 16-bit operation mode)		
	7	INTC11	Generation of TM1-CR11 match signal (in 8-bit operation mode) Generation of TM1W-CR11W match signal (in 16-bit operation mode)		
	8	INTC20	Generation of TM2-CR20 match signal (in 8-bit operation mode) Generation of TM2W-CR20W match signal (in 16-bit operation mode)		
	9	INTC21	Generation of TM2-CR21 match signal (in 8-bit operation mode) Generation of TM2W-CR21W match signal (in 16-bit operation mode)		
	10	INTC30	Generation of TM3-CR30 match signal (in 8-bit operation mode) Generation of TM3W-CR30W match signal (in 16-bit operation mode)		
	11	INTP4	Detection of pin input edge	External	○
	12	INTP5	Detection of pin input edge		
	13	INTAD	End of A/D conversion (transfer of ADCR)	Internal	○
	14	INTSER	Occurrence of ASI0 reception error		–
	15	INTSR	End of ASI0 reception or CSI1 transfer		○
		INTCSI1			
	16	INTST	End of ASI0 transfer		
	17	INTCSI	End of CSI1 transfer		
	18	INTSER2	Occurrence of ASI2 reception error		–
	19	INTSR2	End of ASI2 reception or CSI2 transfer		○
		INTCSI2			
	20	INTST2	End of ASI2 transfer		
	21 (lowest)	INTSPC	I^2C bus stop condition interrupt		

Remark ASI: asynchronous serial interface
CSI: clocked serial interface

8.2 Vectored Interrupt

Execution branches to a servicing routing by using the memory contents of a vector table address corresponding to the interrupt source as the address of the branch destination.

So that the CPU performs interrupt servicing, the following operations are performed:

- On branching: Saves the status of the CPU (contents of PC and PSW) to stack
- On returning: Restores the status of the CPU (contents of PC and PSW) from stack

To return to the main routine from an interrupt service routine, the RETI instruction is used.

The branch destination address is in a range of 0 to FFFFH.

Table 8-3. Vector Table Address

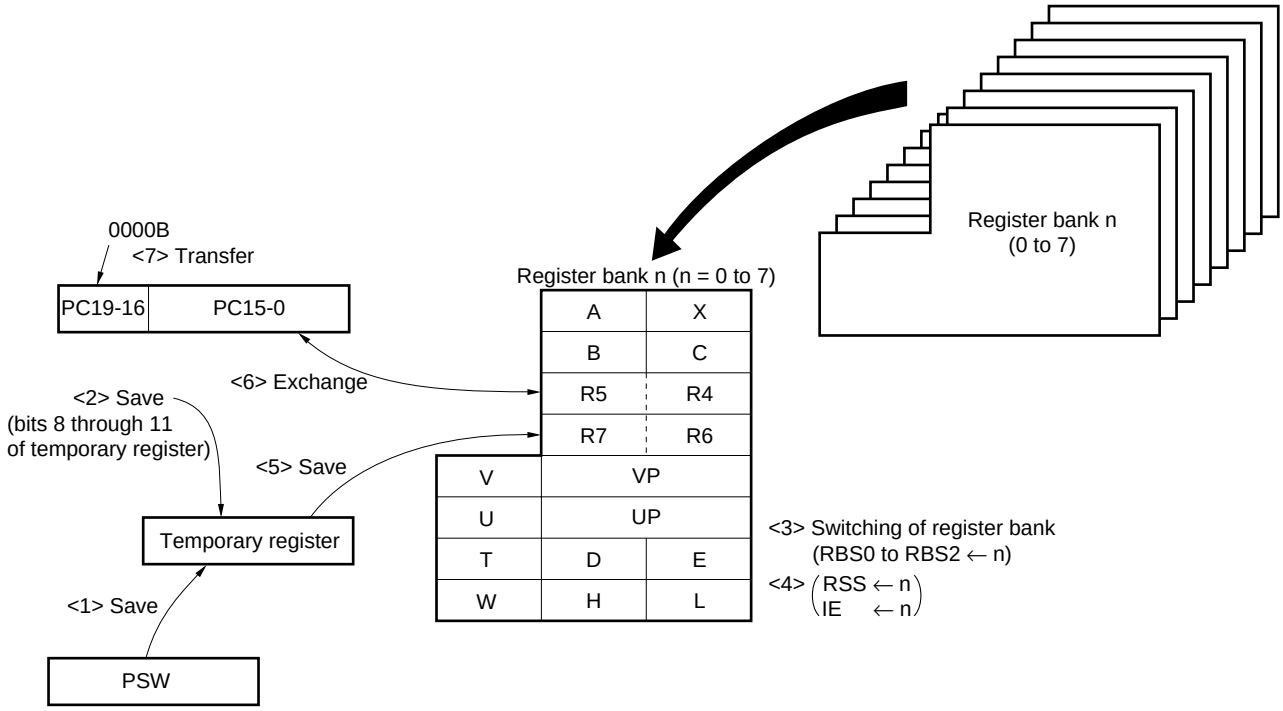
Interrupt Source	Vector Table Address
BRK instruction	003EH
Operand error	003CH
NMI	0002H
WDT	0004H
INTP0	0006H
INTP1	0008H
INTP2	000AH
INTP3	000CH
INTC00	000EH
INTC01	0010H
INTC10	0012H
INTC11	0014H
INTC20	0016H
INTC21	0018H
INTC30	001AH
INTP4	001CH
INTP5	001EH
INTAD	0020H
INTSER	0022H
INTSR	0024H
INTCSI1	
INTST	0026H
INTCSI	0028H
INTSER2	002AH
INTSR2	002CH
INTCSI2	
INTST2	002EH
INTSPC	0030H

8.3 Context Switching

When an interrupt request is generated or when the BRKCS instruction is executed, a predetermined register bank is selected by hardware. Context switching is a function that branches execution to a vector address stored in advance in the register bank, and to stack the current contents of the program counter (PC) and program status word (PSW) to the register bank.

The branch address is in a range of 0 to FFFFH.

Figure 8-1. Context Switching Operation When Interrupt Request Is Generated

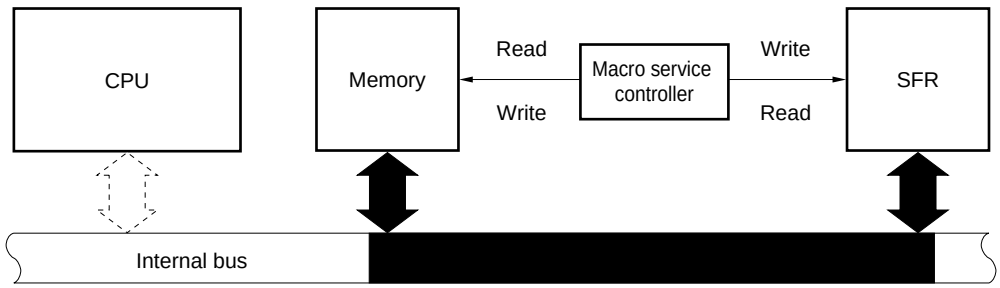


8.4 Macro Service

This function is to transfer data between memory and a special function register (SFR) without intervention by the CPU. A macro service controller accesses the memory and SFR in the same transfer cycle and directly transfers data without loading it.

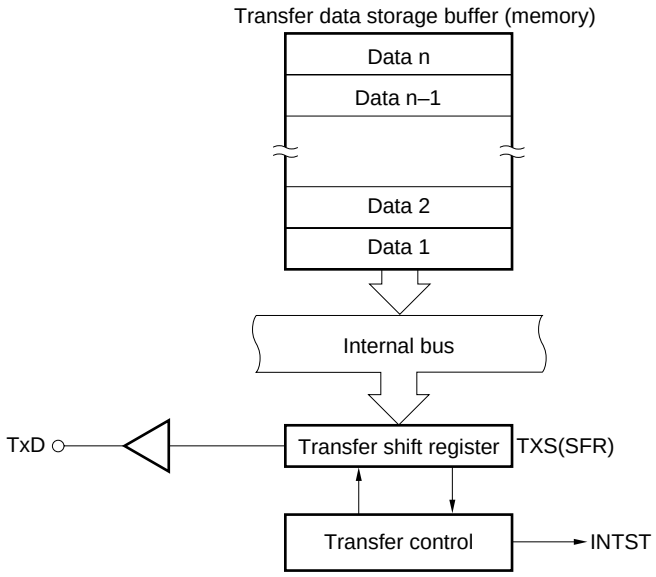
Because this function does not save or restore the status of the CPU, or load data, data can be transferred at high speeds.

Figure 8-2. Macro Service



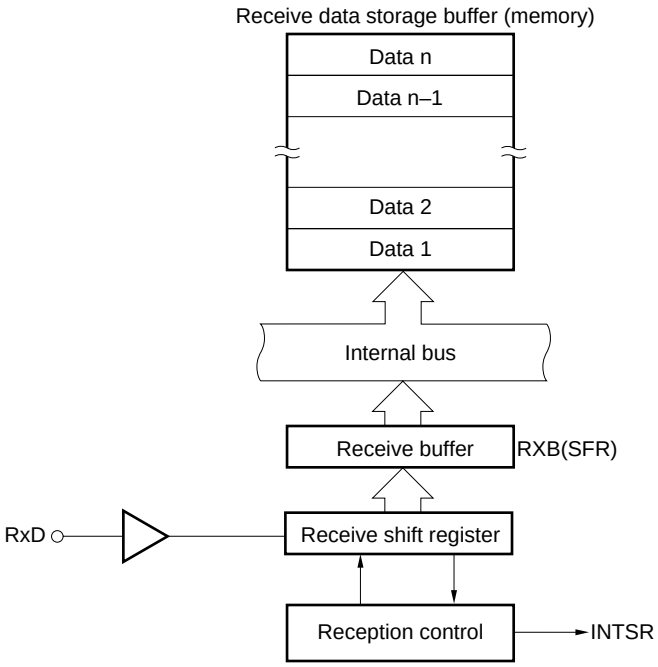
8.5 Application Example of Macro Service

(1) Transfer of serial interface



Each time macro service request (INTST) is generated, the next transfer data is transferred from memory to TXS. When data n (last byte) has been transferred to TXS (when the transfer data storage buffer has become empty), vectored interrupt request (INTST) is generated.

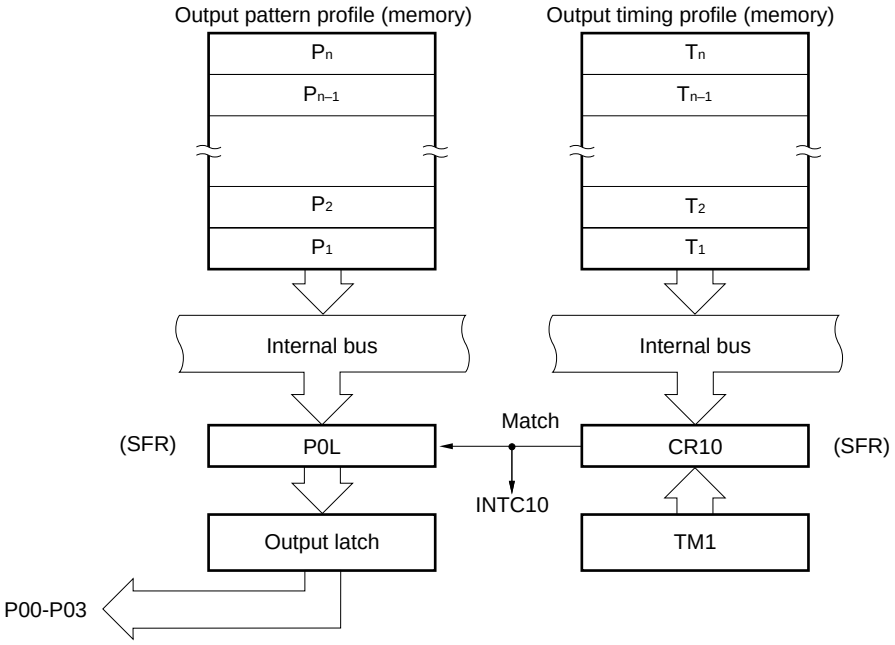
(2) Reception of serial interface



Each time macro service request (INTSR) is generated, the receive data is transferred from RXB to memory. When data n (last byte) has been transferred to memory (when the receive data storage buffer has become full), vectored interrupt request (INTSR) is generated.

(3) Real-time output port

INTC10 and INTC11 serve as the output triggers of the real-time output port. The macro services for these can set the following output pattern and intervals simultaneously. Therefore, INTC10 and INTC11 can control two stepping motors independently of each other. They can also be used for PWM output or to control DC motors.



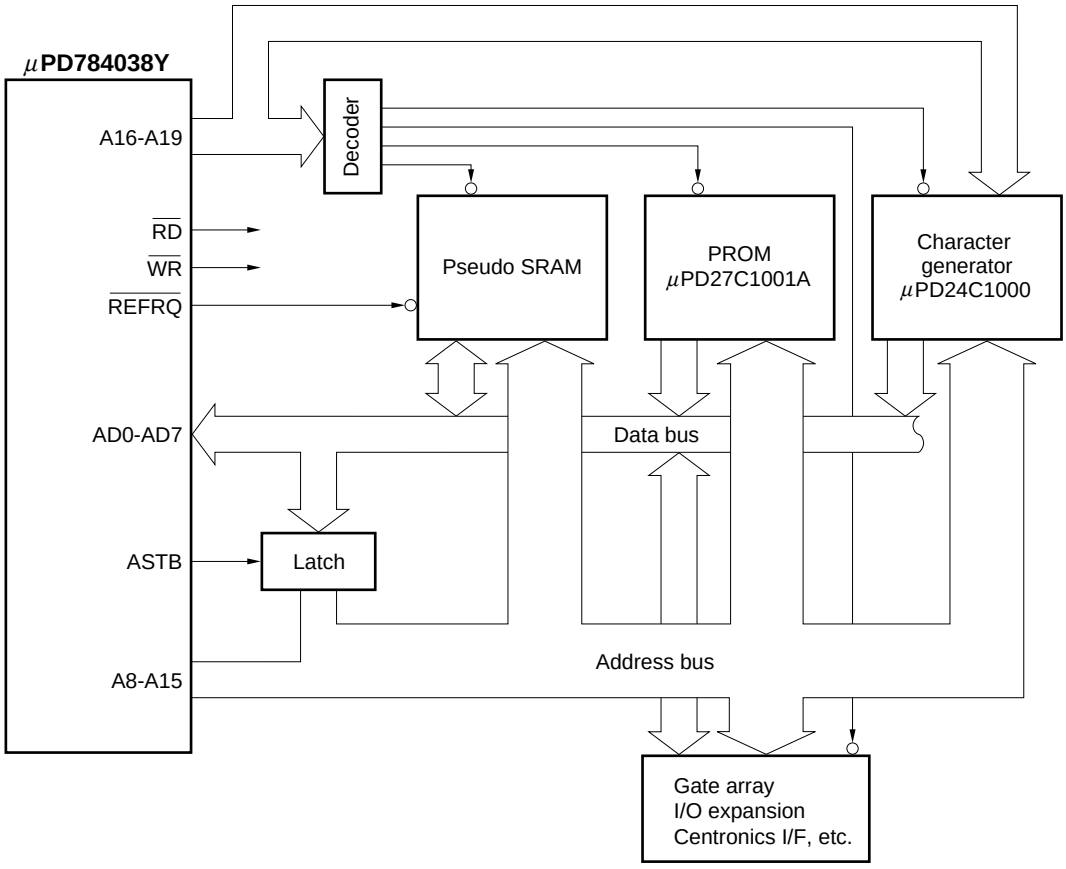
Each time macro service request (INTC10) is generated, the pattern and timing are transferred to the buffer register (P0L) and compare register (CR10), respectively. When the contents of the timer register 1 (TM1) coincide with those of CR10, INTC10 is generated again, and the contents of P0L are transferred to the output latch. When Tn (last byte) has transferred to CR10, vectored interrupt request (INTC10) is generated.

The same applies to INTC11.

9. LOCAL BUS INTERFACE

The local bus interface can connect an external memory or I/O (memory mapped I/O) and support a memory space of 1 MByte (refer to Figure 9-1).

Figure 9-1. Example of Local Bus Interface



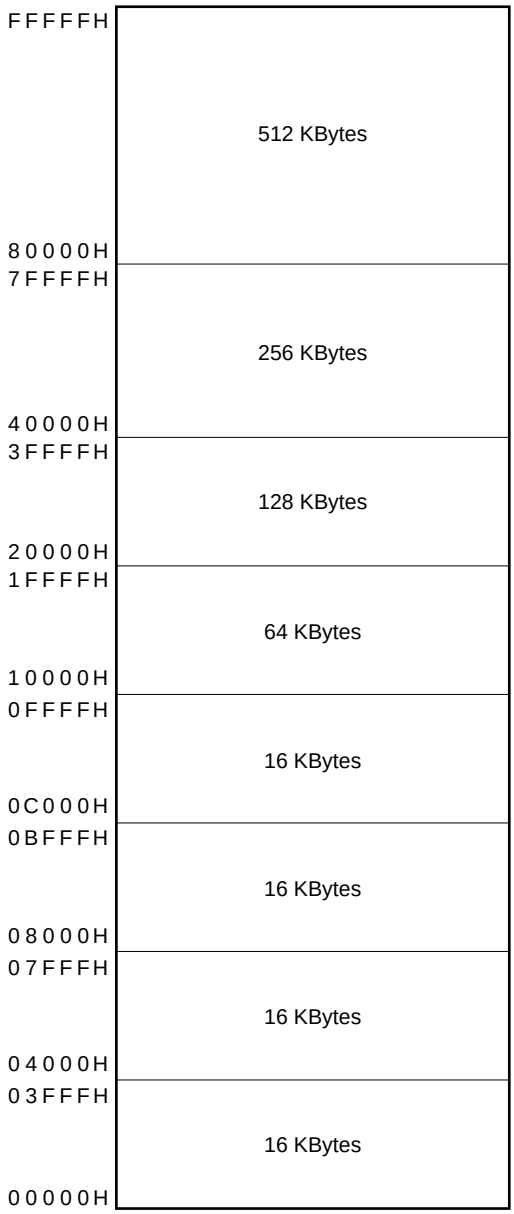
9.1 Memory Expansion

The memory capacity can be expanded in seven steps, from 256 Bytes to 1 MByte, by connecting an external program memory and data memory.

9.2 Memory Space

The 1-MByte memory space is divided into eight spaces of logical addresses. Each space can be controlled by using the programmable wait function and pseudo static RAM refresh function.

Figure 9-2. Memory Space



9.3 Programmable Wait

The memory space can be divided into eight spaces and wait states can be independently inserted in each of these spaces while the $\overline{RD}$ and $\overline{WR}$ signals are active. Even when a memory with a different access time is connected, therefore, the efficiency of the entire system does not drop.

In addition, an address wait function that extends the active period of the ASTB signal is also provided so as to have a sufficient address decode time (this function can be set to the entire space).

9.4 Pseudo Static RAM Refresh Function

The following refresh operations can be performed:

- Pulse refresh: A bus cycle that outputs a refresh pulse to the $\overline{REFRQ}$ pin at a fixed cycle is inserted. The memory spaces is divided into eight spaces, and a refresh pulse can be output from the $\overline{REFRQ}$ pin while a specified memory space is accessed. Therefore, the normal memory access is not kept to wait by the refresh cycle.
- Power-down self-refresh: The low level is output to the $\overline{REFRQ}$ pin in the standby mode to retain the contents of the pseudo static RAM.

9.5 Bus Hold Function

A bus hold function is provided to facilitate connection of a DMA controller. When a bus hold request signal (HLDRQ) is received from an external bus master, the address bus, address/data bus, and ASTB, $\overline{RD}$, and $\overline{WR}$ pins go into a high-impedance state when the current bus cycle has been completed. This makes the bus hold acknowledge (HLDAK) signal active, and releases the bus to the external bus master.

Note that, while the bus hold function is used, the external wait function and pseudo static RAM refresh function cannot be used.

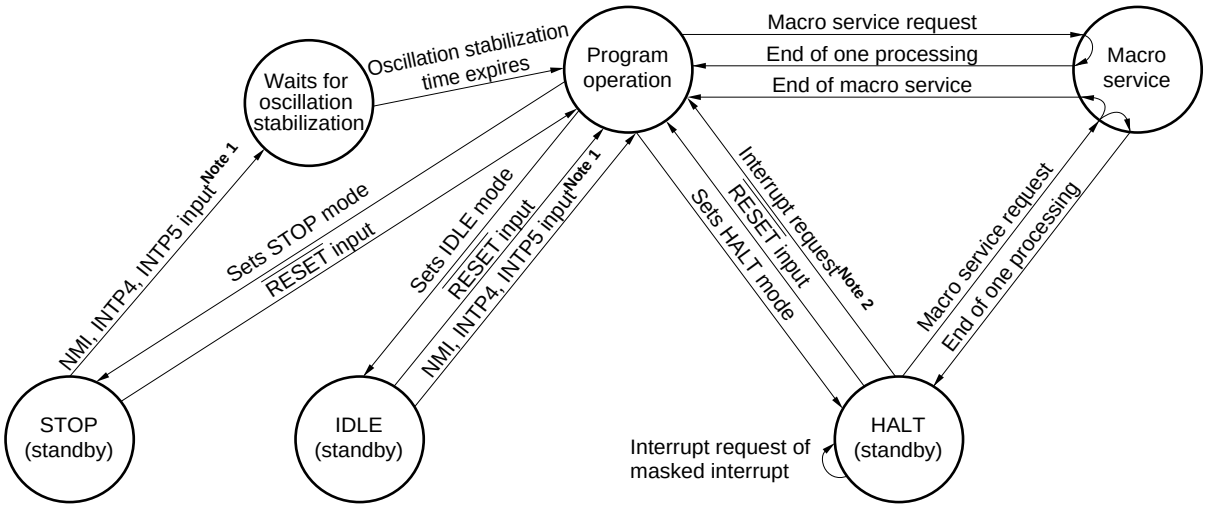
10. STANDBY FUNCTION

This function is to reduce the power dissipation of the chip, and can be used in the following modes:

- HALT mode: Stops supply of the operating clock to the CPU. This mode is used in combination with the normal operation mode for intermittent operation to reduce the average power dissipation.
- IDLE mode: Stops the entire system with the oscillation circuit continuing operation. The power dissipation in this mode is close to that in the STOP mode. However, the time required to restore the normal program operation from this mode is almost the same as that from the HALT mode.
- STOP mode: Stops the oscillator and thereby to stop all the internal operations of the chip. Consequently, the power dissipation is minimized with only leakage current flowing.

These modes are programmable.
The macro service can be started from the HALT mode.

Figure 10-1. Transition of Standby Status



Notes **1.** When INTP4 and INTP5 are not masked
2. Only interrupt requests that are not masked

Remark Only the externally input NMI is valid. The watchdog timer cannot be used to release the standby mode (STOP/IDLE mode).

11. RESET FUNCTION

When the low level is input to the $\overline{\text{RESET}}$ pin, the internal hardware is initialized (reset status).

When the $\overline{\text{RESET}}$ pin goes high, the following data are set to the program counter (PC).

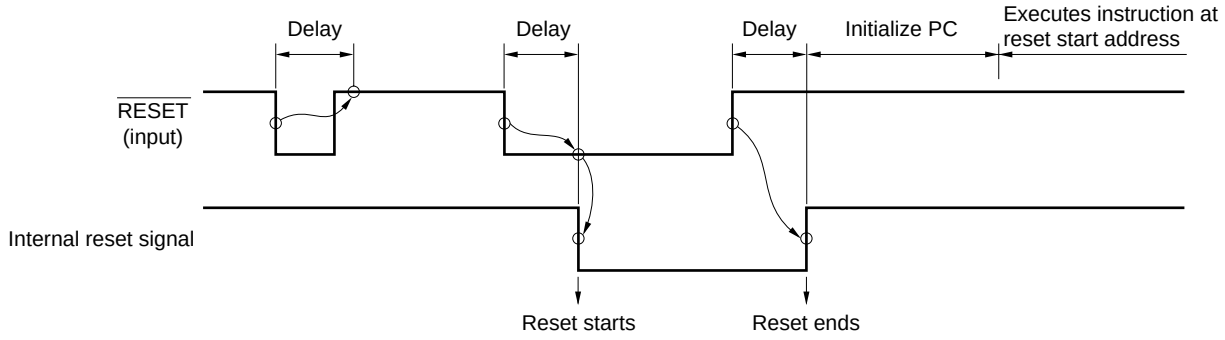
- Lower 8 bits of PC: contents of address 0000H
- Middle 8 bits of PC: contents of address 0001H
- Higher 4 bits of PC: 0

Program execution is started from a branch destination address which is the contents of the PC. Therefore, the system can be reset and started from any address.

Set the contents of each register by program as necessary.

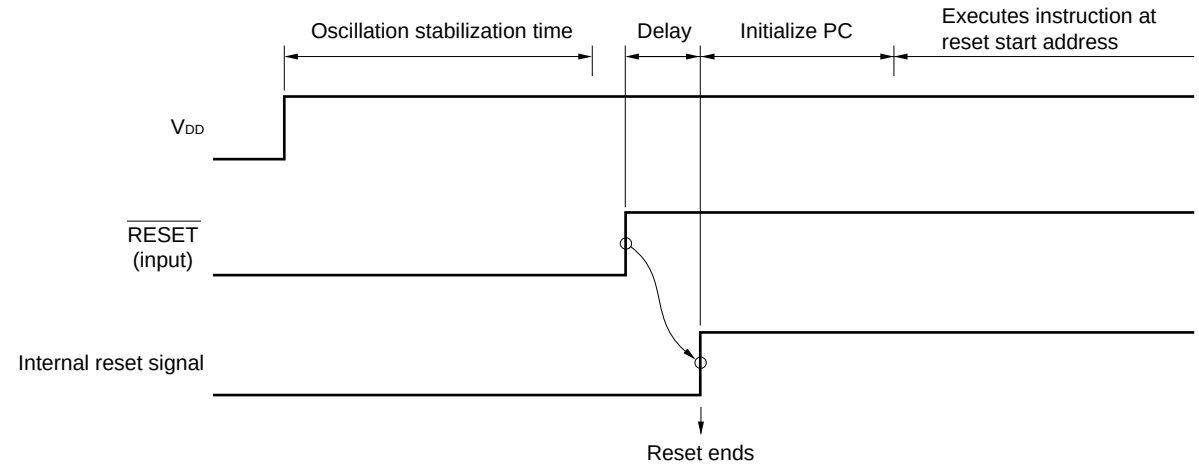
The $\overline{\text{RESET}}$ input circuit has a noise reduction circuit to prevent malfunctioning due to noise. This noise reduction circuit is a sampling circuit by analog delay.

Figure 11-1. Accepting RESET Signal



Assert the $\overline{\text{RESET}}$ signal active until the oscillation stabilization time (approx. 40 ms) elapses to execute a power-ON reset operation.

Figure 11-2. Power-ON Reset Operation



12. INSTRUCTION SET

(1) 8-bit instructions (The instructions in parentheses are combinations realized by describing A as r)

MOV, XCH, ADD, ADDC, SU B, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC, CHIKL, CHKLA

Table 12-1. Instruction List by 8-Bit Addressing

First Operand \ Second Operand	#byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+] [WHL–]	n	None[Note 2]
A	(MOV) ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH (ADD)[Note 1]	(MOV)[Note 6] (XCH)[Note 6] (ADD)[Note 1,6]	MOV (XCH) (ADD)[Note 1]	(MOV) (XCH) ADD[Note 1]	MOV XCH ADD[Note 1]	MOV	(MOV) (XCH) (ADD)[Note 1]		
r	MOV ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH				ROR[Note 3]	MULU DIVUW INC DEC
saddr	MOV ADD[Note 1]	(MOV)[Note 6] (ADD)[Note 1]	MOV ADD[Note 1]	MOV XCH ADD[Note 1]							INC DEC DBNZ
sfr	MOV ADD[Note 1]	MOV (ADD)[Note 1]	MOV ADD[Note 1]								PUSH POP CHKL CHKLA
!addr16 !!addr24	MOV	(MOV) ADD[Note 1]	MOV								
mem [saddrp] [%saddrg]		MOV ADD[Note 1]									
mem3											ROR4 ROL4
r3 PSWL PSWH	MOV	MOV									
B, C											DBNZ
STBC, WDM	MOV										
[TDE+] [TDE–]		(MOV) (ADD)[Note 1] MOVM[Note 4]							MOVBK[Note 5]		

Notes
1. The operands of ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as that of ADD.
2. Either the second operand is not used, or the second operand is not an operand address.
3. The operands of ROL, RORC, ROLC, SHR, and SHL are the same as that of ROR.
4. The operands of XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as that of MOVM.
5. The operands of XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as that of MOVBK.
6. The code length of some instructions having saddr2 as saddr in this combination is short.

(2) 16-bit instructions (The instructions in parentheses are combinations realized by describing AX as rp)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 12-2. Instruction List by 16-Bit Addressing

First Operand \ Second Operand	#word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None[Note 2]
AX	(MOVW) ADDW[Note 1]	(MOVW) (XCHW) (ADD)[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	(MOVW)[Note 3] (XCHW)[Note 3] (ADDW)[Note 1,3]	MOVW (XCHW) (ADDW)[Note 1]	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW				SHRW SHLW	MULW[Note 4] INCW DECW
saddrp	MOVW ADDW[Note 1]	(MOVW)[Note 3] (ADDW)[Note 1]	MOVW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]							INCW DECW
sfrp	MOVW ADDW[Note 1]	MOVW (ADDW)[Note 1]	MOVW ADDW[Note 1]								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. The operands of SUBW and CMPW are the same as that of ADDW.

2. Either the second operand is not used, or the second operand is not an operand address.

3. The code length of some instructions having saddrp2 as saddrp in this combination is short.

4. The operands of MULUW and DIVUX are the same as that of MULW.

(3) 24-bit instructions (The instructions in parentheses are combinations realized by describing WHL as rg)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 12-3. Instruction List by 24-Bit Addressing

First Operand \ Second Operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note Either the second operand is not used, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 12-4. Bit Manipulation Instructions

Second Operand / First Operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr. bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note Either the second operand is not used, or the second operand is not an operand address.

(5) Call and return/branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 12-5. Call and Return/Branch Instructions

Operand of Instruction Address	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLF	BRKCS	BRK RET RETI RETB
Compound instruction	BF BT BTCLR BFSET DBNZ											

Note The operands of BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

★ 13. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

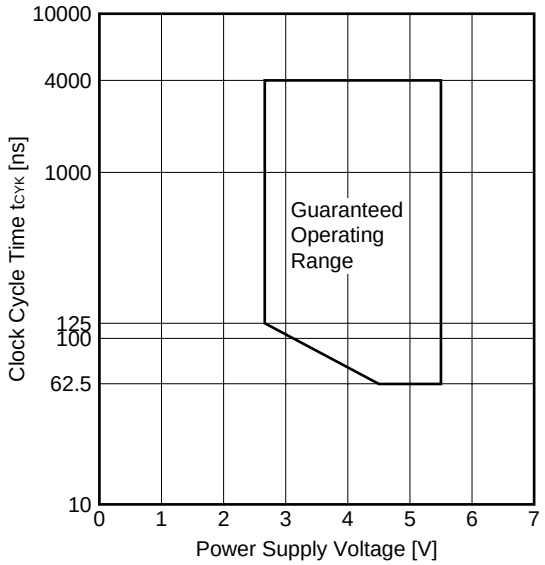
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD}+0.5	V
	AV_{SS}		–0.5 to +0.5	V
Input voltage	V_I		–0.5 to V_{DD}+0.5	V
Output voltage	V_O		–0.5 to V_{DD}+0.5	V
Low-level output current	I_{OL}	Per pin	15	mA
		Total of all output pins	100	mA
High-level output current	I_{OH}	Per pin	–10	mA
		Total of all output pins	–100	mA
A/D converter reference input voltage	AV_{REF1}		–0.5 to V_{DD}+0.3	V
D/A converter reference input voltage	AV_{REF2}		–0.5 to V_{DD}+0.3	V
	AV_{REF3}		–0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

OPERATING CONDITIONS

- Operating ambient temperature (T_A) : –40 to +85°C
- Rising time and falling time (tr, tf) (at pins which are not specified) : 0 to 200 μs
- Power supply voltage and clock cycle time : See Figure 13-1

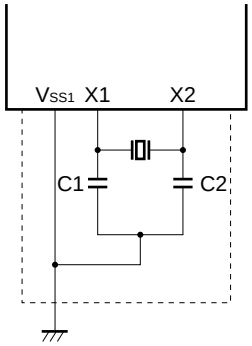
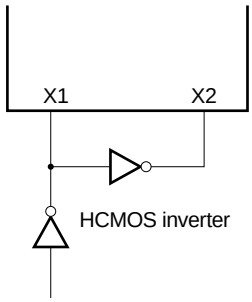
Figure 13-1. Power Supply Voltage and Clock Cycle Time



CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz		10	pF	
Output capacitance	C_O	Unmeasured pins returned to 0 V.			10	pF
I/O capacitance	C_{IO}				10	pF

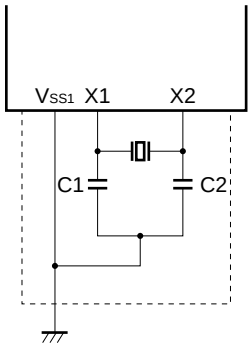
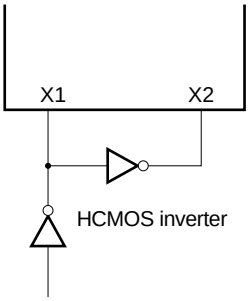
OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = +4.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillator frequency (f_{XX})	4	32	MHz
External clock		X1 input frequency (f_X)	4	32	MHz
		X1 input rising/falling time (t_{XR}, t_{XF})	0	10	ns
		X1 input high-/low-level width (t_{WXH}, t_{WXL})	10	125	ns

Caution When using the system clock oscillator, wiring the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS1}. Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = +2.7 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillator frequency (f_{XX})	4	16	MHz
External clock		X1 input frequency (f_X)	4	16	MHz
		X1 input rising/falling time (t_{XR}, t_{XF})	0	10	ns
		X1 input high-/low-level width (t_{WXH}, t_{WXL})	10	125	ns

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- **Do not fetch a signal from the oscillator.**

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL1}	For pins other than those described in **Notes 1, 2, 3, 4,** and **6**	–0.3		$0.3V_{DD}$	V
	V_{IL2}	For pins described in **Notes 1**, **2**, **3**, **4**, and **6**	–0.3		$0.2V_{DD}$	V
	V_{IL3}	V_{DD} = +5.0 V±10% For pins described in **Notes 2**, **3**, and **4**	–0.3		+0.8	V
High-level input voltage	V_{IH1}	For pins other than those described in **Notes 1** and **6**	$0.7V_{DD}$		V_{DD}+0.3	V
	V_{IH2}	For pins described in **Notes 1** and **6**	$0.8V_{DD}$		V_{DD}+0.3	V
	V_{IH3}	V_{DD} = +5.0 V±10% For pins described in **Notes 2**, **3**, and **4**	2.2		V_{DD}+0.3	V
Low-level output voltage	V_{OL1}	I_{OL} = 2 mA For pins other than those described in **Note 6**			0.4	V
	V_{OL2}	I_{OL} = 3 mA For pins described in **Note 6**			0.4	V
		I_{OL} = 6 mA For pins described in **Note 6**			0.6	V
	V_{OL3}	V_{DD} = +5.0 V±10% I_{OL} = 8 mA For pins described in **Notes 2** and **5**			1.0	V
High-level output voltage	V_{OH1}	I_{OH} = –2 mA	V_{DD}–1.0			V
	V_{OH2}	V_{DD} = +5.0 V±10% I_{OH} = –5 mA For pins other than those described in **Note 4**	V_{DD}–1.4			V
X1 low-level input current	I_{IL}	EXTC = 0 0 V ≤ V_I ≤ V_{IL2}			–30	μA
X1 high-level input current	I_{IH}	EXTC = 0 V_{IH2} ≤ V_I ≤ V_{DD}			+30	μA

Notes 1. X1, X2, $\overline{\text{RESET}}$, P12/ASCK2/$\overline{\text{SCK2}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, and TEST

2. P40/AD0 to P47/AD7 and P50/A8 to P57/A15

3. P60/A16 to P63/A19, P64/$\overline{\text{RD}}$, P65/$\overline{\text{WR}}$, P66/$\overline{\text{WAIT}}$/HLDRQ, and P67/$\overline{\text{REFRQ}}$/HLDAK

4. P00 to P07

5. P10 to P17

6. P32/$\overline{\text{SCK0}}$/SCL and P33/SO0/SDA

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD} For pins other than pin X1 when EXTC = 0				±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current	I_{DD1}	Operation mode	f_{XX} = 32 MHz V_{DD} = +5.0 V±10%		25	45	mA
			f_{XX} = 16 MHz V_{DD} = +2.7 to 3.3 V		12	25	mA
	I_{DD2}	HALT mode	f_{XX} = 32 MHz V_{DD} = +5.0 V±10%		13	26	mA
			f_{XX} = 16 MHz V_{DD} = +2.7 to 3.3 V		8	12	mA
	I_{DD3}	IDLE mode (EXTC = 0)	f_{XX} = 32 MHz V_{DD} = +5.0 V±10%			12	mA
			f_{XX} = 16 MHz V_{DD} = +2.7 to 3.3 V			8	mA
Pull-up resistance	R_L	V_I = 0 V		15		80	kΩ

AC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Address setup time	t_{SAST}	V_{DD} = +5.0 V±10%		(0.5+a)T–15		ns
				(0.5+a)T–31		ns
ASTB high-level width	t_{WSTH}	V_{DD} = +5.0 V±10%		(0.5+a)T–17		ns
				(0.5+a)T–40		ns
Address hold time (from ASTB↓)	t_{HSTLA}	V_{DD} = +5.0 V±10%		0.5T–24		ns
				0.5T–34		ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}			0.5T–14		ns
$\overline{RD}$↓ delay time from address	t_{DAR}	V_{DD} = +5.0 V±10%		(1+a)T–9		ns
				(1+a)T–15		ns
Address float time (from $\overline{RD}$↓)	t_{FRA}				0	ns
Data input time from address	t_{DAID}	V_{DD} = +5.0 V±10%			(2.5+a+n)T–37	ns
					(2.5+a+n)T–52	ns
Data input time from ASTB↓	t_{DSTID}	V_{DD} = +5.0 V±10%			(2+n)T–40	ns
					(2+n)T–60	ns
Data input time from $\overline{RD}$↓	t_{DRID}	V_{DD} = +5.0 V±10%			(1.5+n)T–50	ns
					(1.5+n)T–70	ns
$\overline{RD}$↓ delay time from ASTB↓	t_{DSTR}			0.5T–9		ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}			0		ns
Address active time from $\overline{RD}$↑	t_{DRA}	After program is read	V_{DD} = +5.0 V±10%	0.5T–8		ns
				0.5T–12		ns
		After data is read	V_{DD} = +5.0 V±10%	1.5T–8		ns
				1.5T–12		ns
ASTB↑ delay time from $\overline{RD}$↑	t_{DRST}			0.5T–17		ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = +5.0 V±10%		(1.5+n)T–30		ns
				(1.5+n)T–40		ns
Address hold time (from $\overline{WR}$↑)	t_{HWA}			0.5T–14		ns
$\overline{WR}$↓ delay time from address	t_{DAW}	V_{DD} = +5.0 V±10%		(1+a)T–5		ns
				(1+a)T–15		ns
Data output delay time from ASTB↓	t_{DSTOD}	V_{DD} = +5.0 V±10%			0.5T+19	ns
					0.5T+35	ns
Data output delay time from $\overline{WR}$↓	t_{DWOD}				0.5T–11	ns
$\overline{WR}$↓ output delay time from ASTB↓	t_{DSTW}			0.5T–9		ns

Remark T : T_{CYK} (system clock cycle time)
a : 1 (during address wait), otherwise, 0
n : Number of wait states (n ≥ 0)

(1) Read/write operation (2/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (to $\overline{WR}$↑)	t_{SODW}	V_{DD} = +5.0 V±10%	(1.5+n)T–30		ns
			(1.5+n)T–40		ns
Data hold time (from $\overline{WR}$↑) Note	t_{HWOD}	V_{DD} = +5.0 V±10%	0.5T–5		ns
			0.5T–25		ns
ASTB↑ delay time (from $\overline{WR}$↑)	t_{DWST}		0.5T–12		ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = +5.0 V±10%	(1.5+n)T–30		ns
			(1.5+n)T–40		ns

Note The hold time includes the time during which V_{OH1} and V_{OL1} are held under the load conditions of C_L = 50 pF and R_L = 4.7 kΩ.

Remark T: T_{CYK} (system clock cycle time)
n: Number of wait states (n ≥ 0)

(2) Bus hold timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Float delay time from HLDRQ↑	t_{FHQC}			(6+a+n)T+50	ns
HLDAK↑ delay time from HLDRQ↑	$t_{DHQHHAH}$	V_{DD} = +5.0 V±10%		(7+a+n)T+30	ns
				(7+a+n)T+40	ns
HLDAK↑ delay time from float	t_{DCFHA}			1T+30	ns
HLDAK↓ delay time from HLDRQ↓	$t_{DHQLHAL}$	V_{DD} = +5.0 V±10%		2T+40	ns
				2T+60	ns
Active delay time from HLDAK↓	t_{DHAC}	V_{DD} = +5.0 V±10%	1T–20		ns
			1T–30		ns

Remark T: T_{CYK} (system clock cycle time)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

(3) External wait timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{WAIT}$↓ input time from address	t_{DAWT}	V_{DD} = +5.0 V±10%		(2+a)T–40	ns
				(2+a)T–60	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	V_{DD} = +5.0 V±10%		1.5T–40	ns
				1.5T–60	ns
$\overline{WAIT}$ hold time from ASTB↓	t_{HSTWTH}	V_{DD} = +5.0 V±10%	(0.5+n)T+5		ns
			(0.5+n)T+10		ns
$\overline{WAIT}$↑ delay time from ASTB↓	t_{DSTWTH}	V_{DD} = +5.0 V±10%		(1.5+n)T–40	ns
				(1.5+n)T–60	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{DRWTL}	V_{DD} = +5.0 V±10%		T–50	ns
				T–70	ns
$\overline{WAIT}$↓ hold time from $\overline{RD}$↓	t_{HRWT}	V_{DD} = +5.0 V±10%	nT+5		ns
			nT+10		ns
$\overline{WAIT}$↑ delay time from $\overline{RD}$↓	t_{DRWTH}	V_{DD} = +5.0 V±10%		(1+n)T–40	ns
				(1+n)T–60	ns
Data input time from $\overline{WAIT}$↑	t_{DWTID}	V_{DD} = +5.0 V±10%		0.5T–5	ns
				0.5T–10	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{DWTW}		0.5T		ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{DWTR}		0.5T		ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{DWWTL}	V_{DD} = +5.0 V±10%		T–5	ns
				T–75	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	t_{HWWT}	V_{DD} = +5.0 V±10%	nT+5		ns
			nT+10		ns
$\overline{WAIT}$↑ delay time from $\overline{WR}$↓	t_{DWWTH}	V_{DD} = +5.0 V±10%		(1+n)T–40	ns
				(1+n)T–70	ns

Remark T: T_{CYK} (system clock cycle time)
a: 1 (during address wait), otherwise, 0
n: Number of wait states ($n \geq 0$)

(4) Refresh timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Random read/write cycle time	t_{RC}		3T		ns
$\overline{REFRQ}$ low-level pulse width	t_{WRFQL}	V_{DD} = +5.0 V±10%	1.5T–25		ns
			1.5T–30		ns
$\overline{REFRQ}$ delay time from ASTB↓	t_{DSTRFQ}		0.5T–9		ns
$\overline{REFRQ}$ delay time from $\overline{RD}$↑	t_{DRRFQ}		1.5T–9		ns
$\overline{REFRQ}$ delay time from $\overline{WR}$↑	t_{DWRFQ}		1.5T–9		ns
ASTB delay time from $\overline{REFRQ}$↑	t_{DRFQST}		0.5T–15		ns
$\overline{REFRQ}$ high-level pulse width	t_{WRFQH}	V_{DD} = +5.0 V±10%	1.5T–25		ns
			1.5T–30		ns

Remark T: T_{CYK} (system clock cycle time)

SERIAL OPERATION (T_A = –40 to +85°C, V_{DD} = +2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

(1) CSI

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time ($\overline{SCK0}$)	t_{CYSK0}	Input	External clock When $\overline{SCK0}$ and SO0 are CMOS I/O	10/f_{XX}+380		ns
		Output		T		μs
Serial clock low-level width ($\overline{SCK0}$)	t_{WSKL0}	Input	External clock When $\overline{SCK0}$ and SO0 are CMOS I/O	5/f_{XX}+150		ns
		Output		0.5T–40		μs
Serial clock high-level width ($\overline{SCK0}$)	t_{WSKH0}	Input	External clock When $\overline{SCK0}$ and SO0 are CMOS I/O	5/f_{XX}+150		ns
		Output		0.5T–40		μs
SI0 setup time (to $\overline{SCK0}$↑)	t_{SSSK0}			40		ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{HSSK0}			5/f_{XX}+40		ns
SO0 output delay time (from $\overline{SCK0}$↓)	t_{DSBSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	5/f_{XX}+150	ns
	t_{DSBSK2}	Open-drain output (2-wire serial I/O mode), R_L = 1 kΩ		0	5/f_{XX}+400	ns

Remarks 1. The values in this table are those when C_L is 100 pF.

2. T: Serial clock cycle set by software. The minimum value is 16/f_{XX}.

3. f_{XX}: Oscillation frequency

(2) I^2C

Parameter	Symbol	Standard mode I^2C bus f_{XX} = 4 to 32 MHz		High-speed mode I^2C bus f_{XX} = 8 to 32 MHz		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time of SCL clock low-level state	t_{LOW}	4.7		1.3		μs
Hold time of SCL clock high-level state	t_{HIGH}	4.0		0.6		μs
Data hold time	$t_{HD;DAT}$	300		300	900	ns
Data setup time	$t_{SU;DAT}$	250		100		ns
Rising time of SDA and SCL signals	t_R		1000	20+0.1Cb	300	ns
Falling time of SDA and SCL signals	t_F		300	20+0.1Cb	300	ns
Load capacitance of each bus line	Cb		400		400	pF

(3) IOE1, IOE2

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1}	Input	V_{DD} = +5.0 V±10%	250		ns
				500		ns
		Output	Internal clock divided by 16	T		ns
Serial clock low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1}	Input	V_{DD} = +5.0 V±10%	85		ns
				210		ns
		Output	Internal clock divided by 16	0.5T–40		ns
Serial clock high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1}	Input	V_{DD} = +5.0 V±10%	85		ns
				210		ns
		Output	Internal clock divided by 16	0.5T–40		ns
SI1, SI2 setup time (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}			40		ns
SI1, SI2 hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}			40		ns
SO1, SO2 output delay time (from $\overline{SCK1}$, $\overline{SCK2}$↓)	t_{DSOSK}			0	50	ns
SO1, SO2 output hold time (from $\overline{SCK1}$, $\overline{SCK2}$ ↑)	t_{HSOSK}	During data transfer		$0.5t_{CYSK1}$–40		ns

Remarks 1. The values in this table are those when C_L is 100 pF.

2. T: Serial clock cycle set by software. The minimum value is $16/f_{XX}$.

(4) UART, UART2

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASCK clock input cycle time	t_{CYASK}	V_{DD} = +5.0 V±10%	125		ns
			250		ns
ASCK clock low-level width	t_{WASKL}	V_{DD} = +5.0 V±10%	52.5		ns
			85		ns
ASCK clock high-level width	t_{WASKH}	V_{DD} = +5.0 V±10%	52.5		ns
			85		ns

CLOCK OUTPUT OPERATION

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CLKOUT cycle time	t_{CYCL}		nT		ns
CLKOUT low-level width	t_{CLL}	V_{DD} = +5.0 V±10%	$0.5t_{CYCL}$–10		ns
			$0.5t_{CYCL}$–20		ns
CLKOUT high-level width	t_{CLH}	V_{DD} = +5.0 V±10%	$0.5t_{CYCL}$–10		ns
			$0.5t_{CYCL}$–20		ns
CLKOUT rising time	t_{CLR}	V_{DD} = +5.0 V±10%		10	ns
				20	ns
CLKOUT falling time	t_{CLF}	V_{DD} = +5.0 V±10%		10	ns
				20	ns

Remark n: Divided frequency ratio set by software in the CPU (n = 1, 2, 4, 8, 16)
T: t_{CYK} (system clock cycle time)

OTHER OPERATIONS

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 low-level width	t_{WIT0L}		$3t_{CYSMP}$+10		ns
INTP0 high-level width	t_{WIT0H}		$3t_{CYSMP}$+10		ns
INTP1 to INTP3, CI low-level width	t_{WIT1L}		$3t_{CYCPU}$+10		ns
INTP1 to INTP3, CI high-level width	t_{WIT1H}		$3t_{CYCPU}$+10		ns
INTP4, INTP5 low-level width	t_{WIT2L}		10		μs
INTP4, INTP5 high-level width	t_{WIT2H}		10		μs
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

Remark t_{CYSMP}: Sampling clock set by software
t_{CYCPU}: CPU operation clock set by software in the CPU

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF1} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Total error Note					1.0	%
Linearity calibration Note					0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	FR = 1	120			t_{CYK}
		FR = 0	180			t_{CYK}
Sampling time	t_{SAMP}	FR = 1	24			t_{CYK}
		FR = 0	36			t_{CYK}
Analog input voltage	V_{IAN}		–0.3		AV_{REF1}+0.3	V
Analog input impedance	R_{AN}			1000		MΩ
AV_{REF1} current	AI_{REF1}			0.5	1.5	mA
AV_{DD} supply current	AI_{DD1}	f_{XX} = 32 MHz, CS = 1		2.0	5.0	mA
	AI_{DD2}	STOP mode, CS = 0		1.0	20	μA

Note Quantization error is not included. This parameter is indicated as the ratio to the full-scale value.

Remark t_{CYK}: System clock cycle time

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = AV_{DD} = +2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

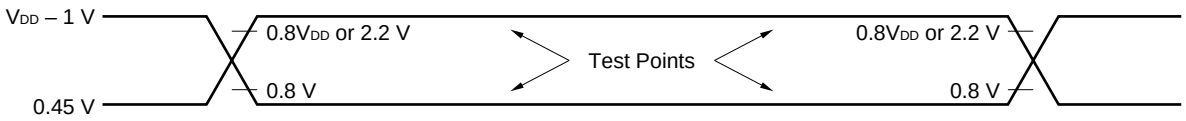
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8			bit
Total error		Load conditions: 4 MΩ, 30 pF	V_{DD} = AV_{DD} = AV_{REF2} = +2.7 to 5.5 V, AV_{REF3} = 0 V			0.6	%
			V_{DD} = AV_{DD} = +2.7 to 5.5 V, AV_{REF2} = 0.75V_{DD}, AV_{REF3} = 0.25V_{DD}			0.8	%
		Load conditions: 2 MΩ, 30 pF	V_{DD} = AV_{DD} = AV_{REF2} = +2.7 to 5.5 V, AV_{REF3} = 0 V			0.8	%
			V_{DD} = AV_{DD} = +2.7 to 5.5 V, AV_{REF2} = 0.75V_{DD}, AV_{REF3} = 0.25V_{DD}			1.0	%
Settling time		Load conditions: 2 MΩ, 30 pF				10	μs
Output resistance	R_O	DACS0, 1 = 55 H			10		kΩ
Analog reference voltage	AV_{REF2}			0.75V_{DD}		V_{DD}	V
	AV_{REF3}			0		0.25V_{DD}	V
AV_{REF2}, AV_{REF3} resistance	R_{AIREF}	DACS0, 1 = 55 H		4	8		kΩ
Reference power supply input current	AI_{REF2}			0		5	mA
	AI_{REF3}			–5		0	mA

DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = +2.7 to 5.5 V		10	50	μA
		V_{DDDR} = +2.5 V		2	10	μA
V_{DD} rising time	t_{RVD}		200			μs
V_{DD} falling time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	Specific pins **Note**	0		$0.1V_{DDDR}$	V
High-level input voltage	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

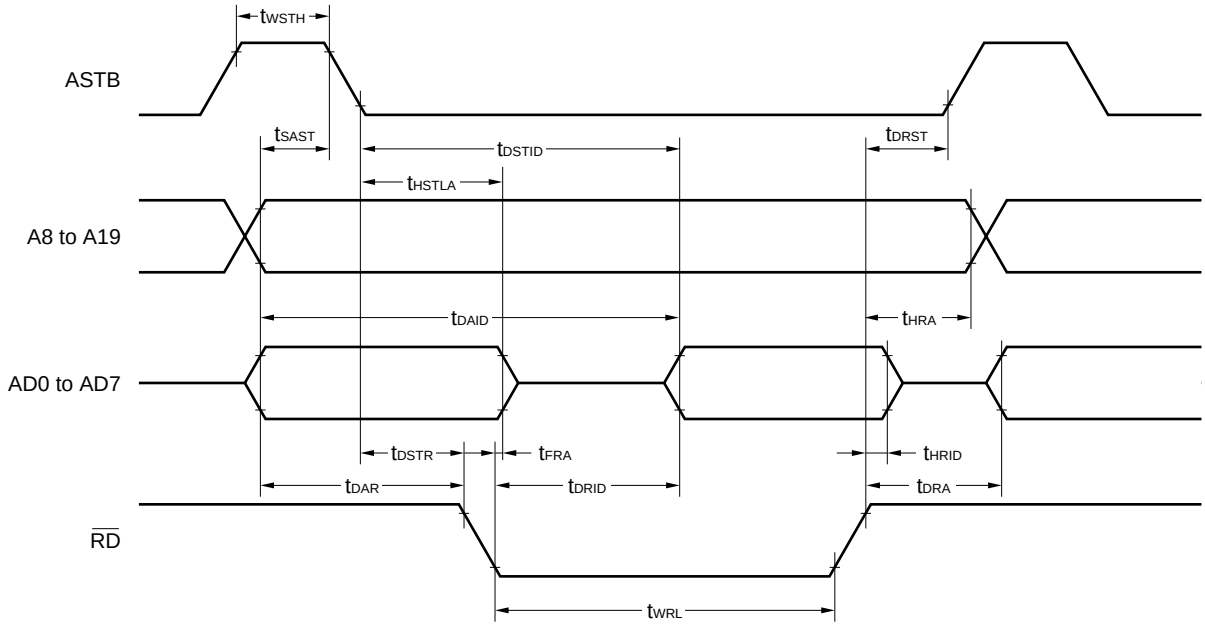
Note $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P32/$\overline{\text{SCK0}}$/SCL, and P33/SO0/SDA pins

AC TIMING TEST POINTS

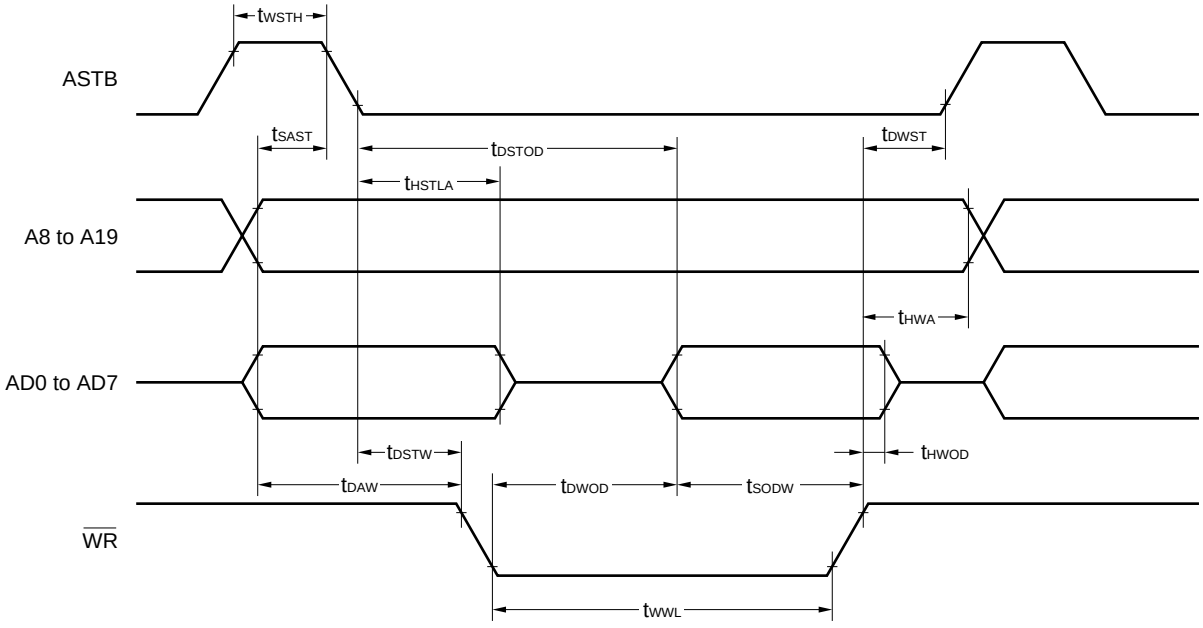


TIMING WAVEFORM

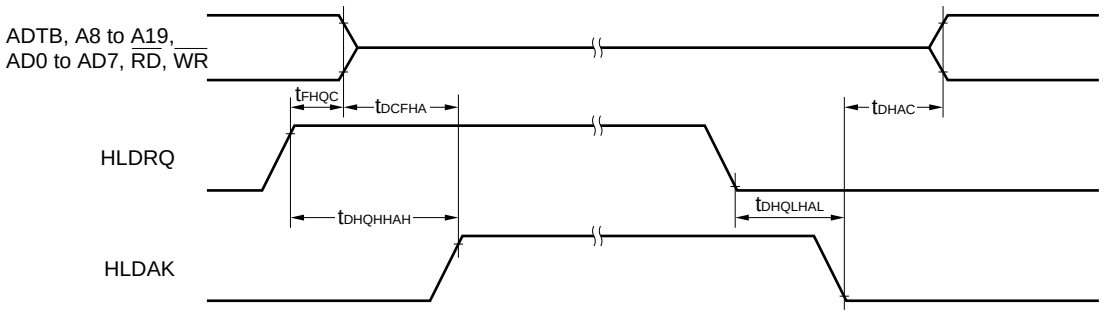
(1) Read operation



(2) Write operation

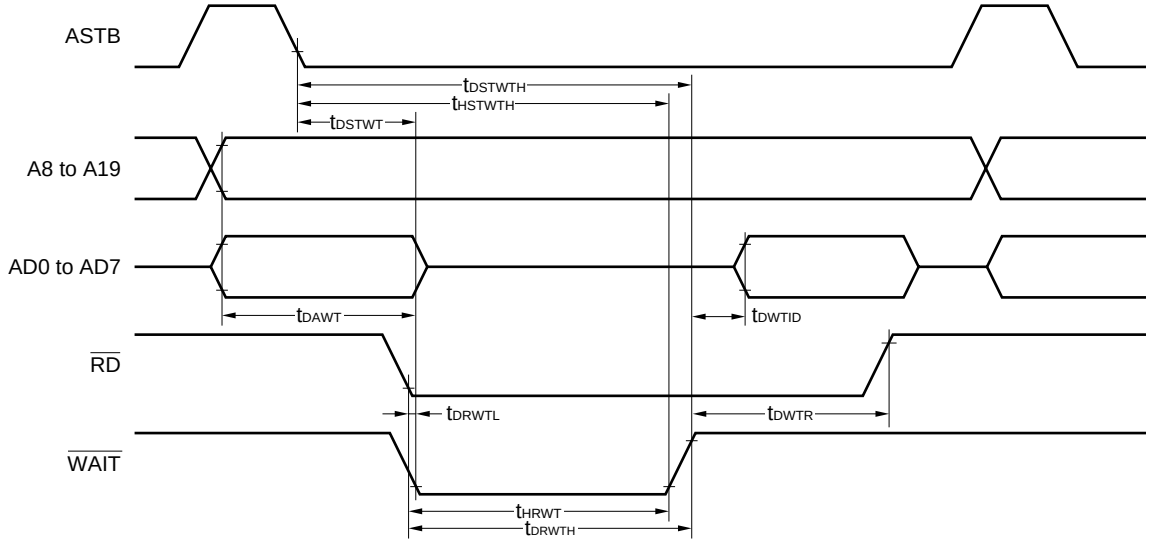


HOLD TIMING

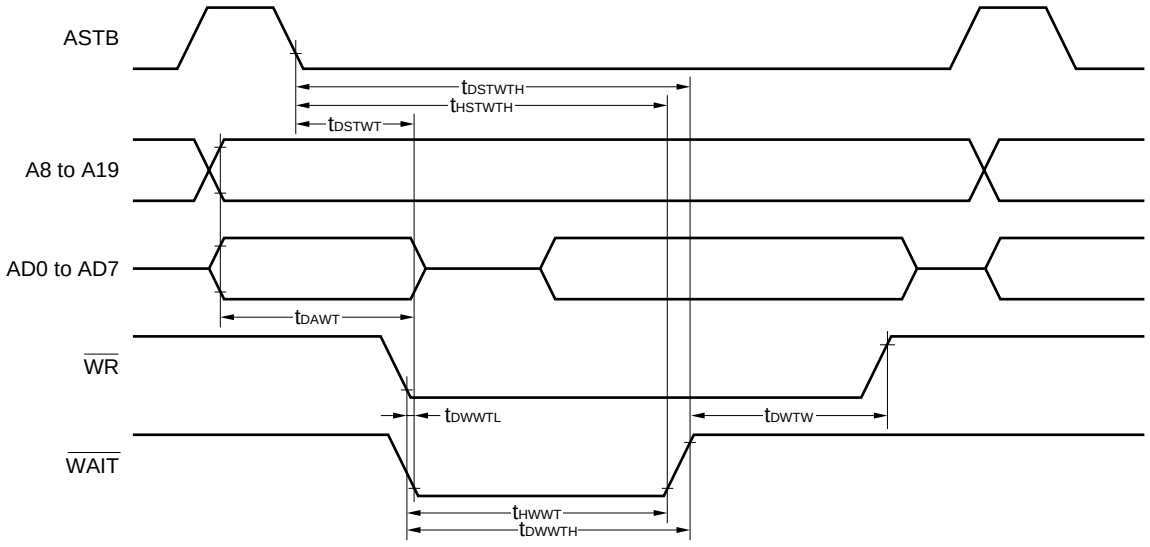


EXTERNAL WAIT SIGNAL INPUT TIMING

(1) Read operation

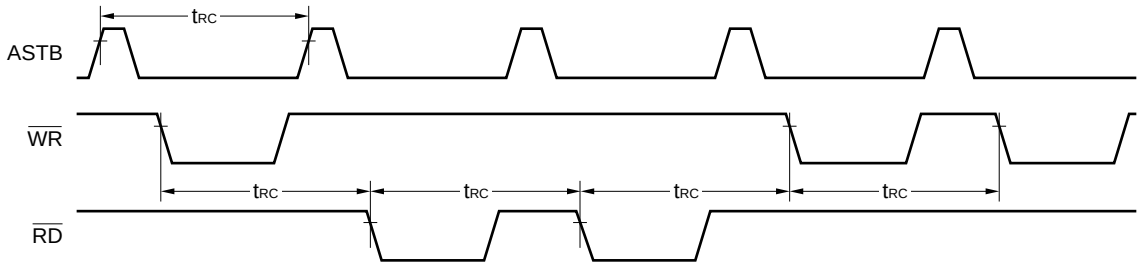


(2) Write operation

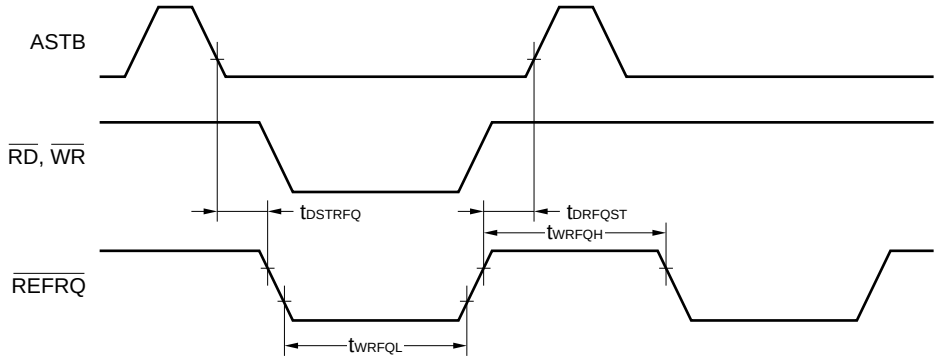


REFRESH TIMING WAVEFORM

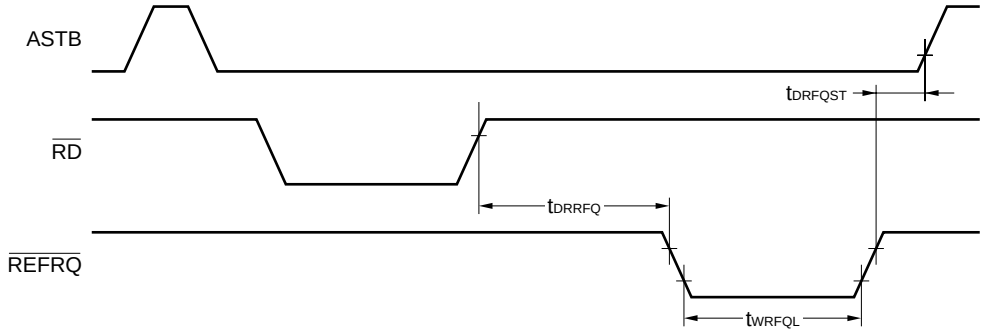
(1) Random read/write cycle



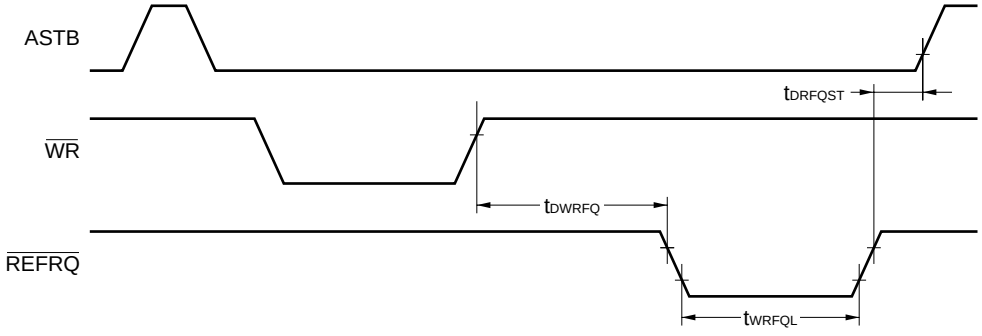
(2) When refresh memory is accessed for read and write at the same time



(3) Refresh after read

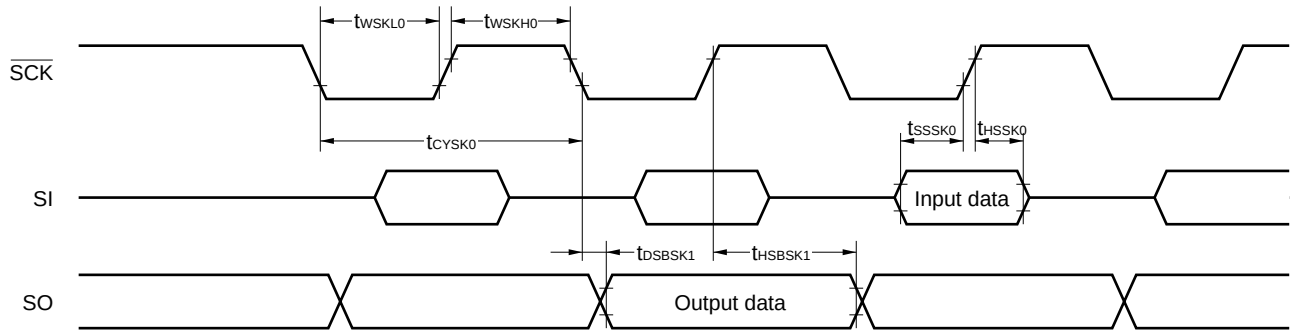


(4) Refresh after write

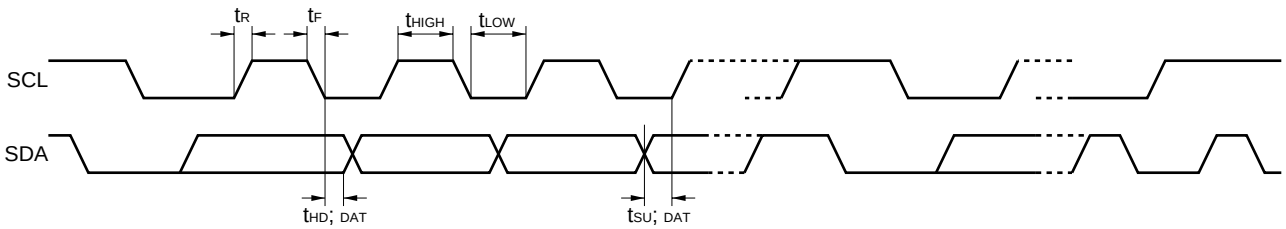


SERIAL OPERATION

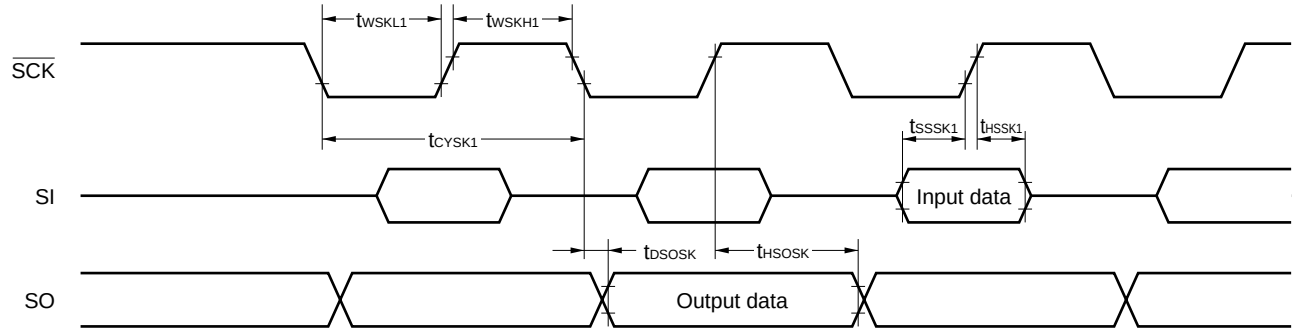
(1) CSI



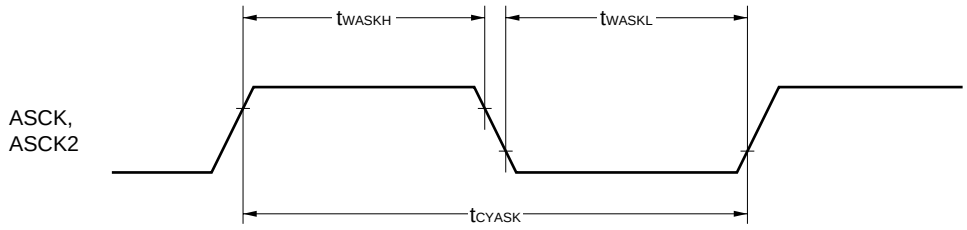
(2) I²C



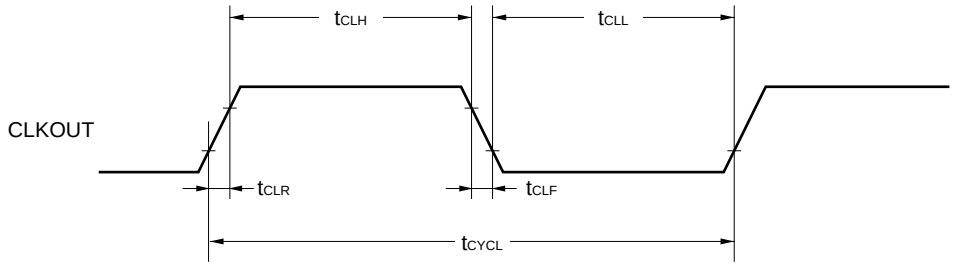
(3) IOE1, IOE2



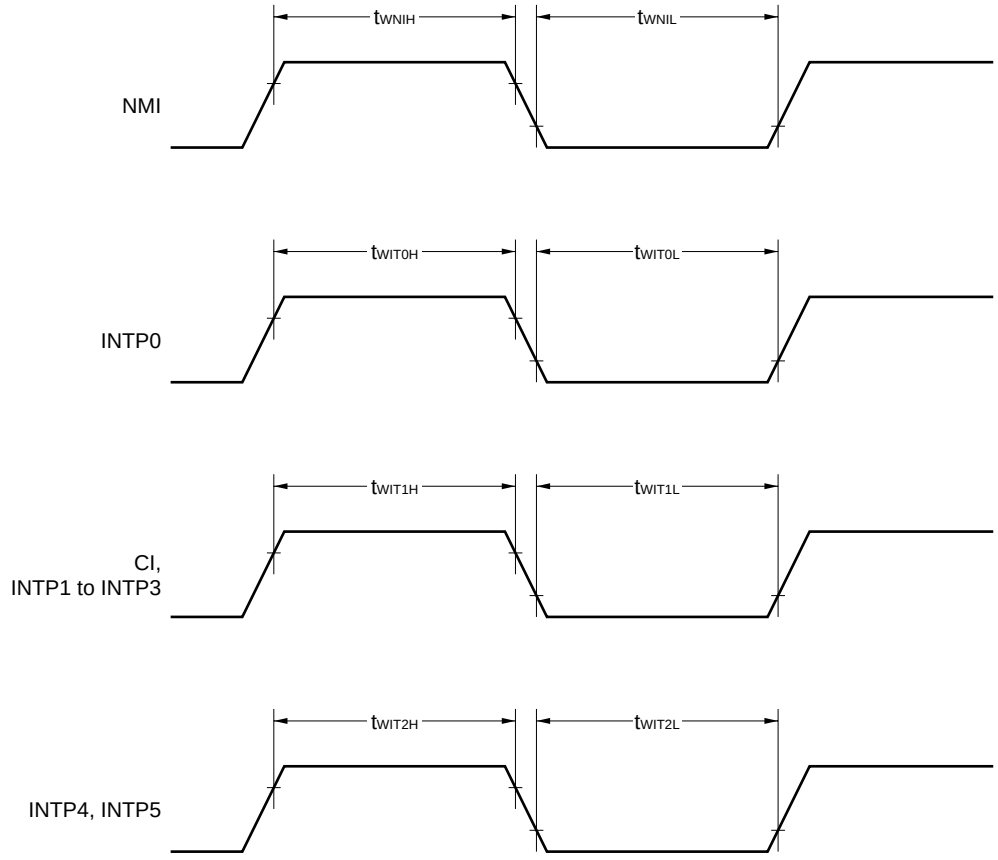
(4) UART, UART2



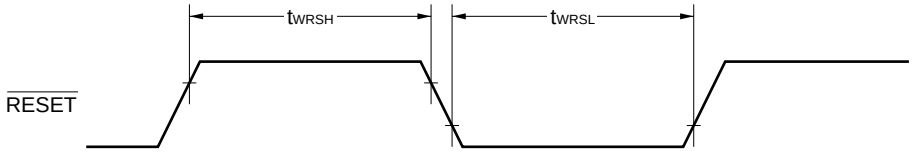
CLOCK OUTPUT TIMING



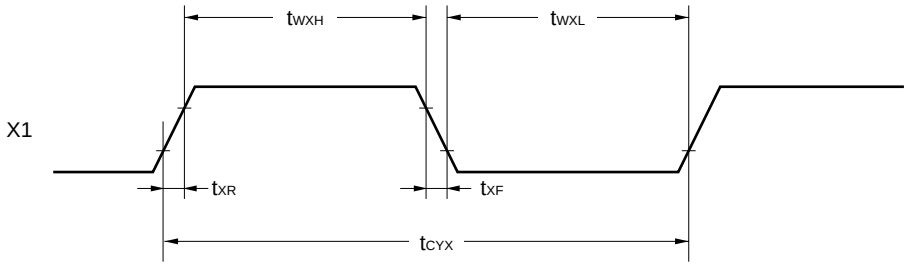
INTERRUPT INPUT TIMING



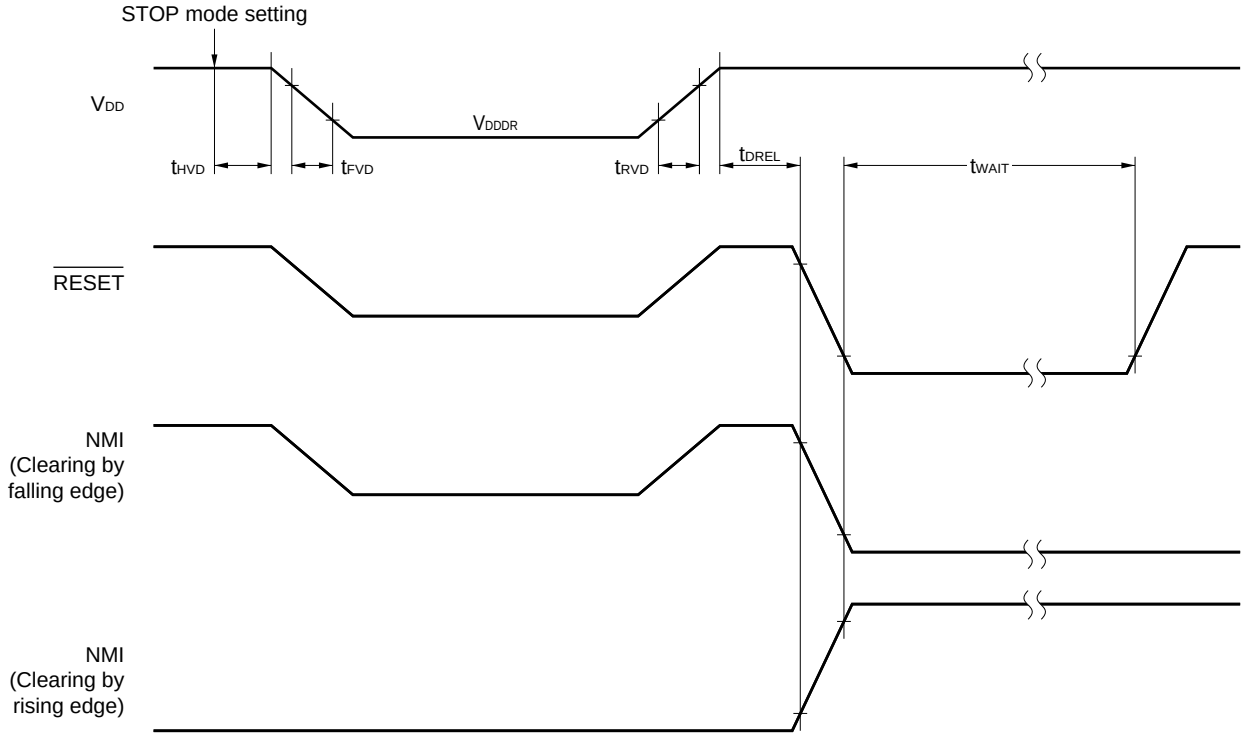
RESET INPUT TIMING



EXTERNAL CLOCK TIMING

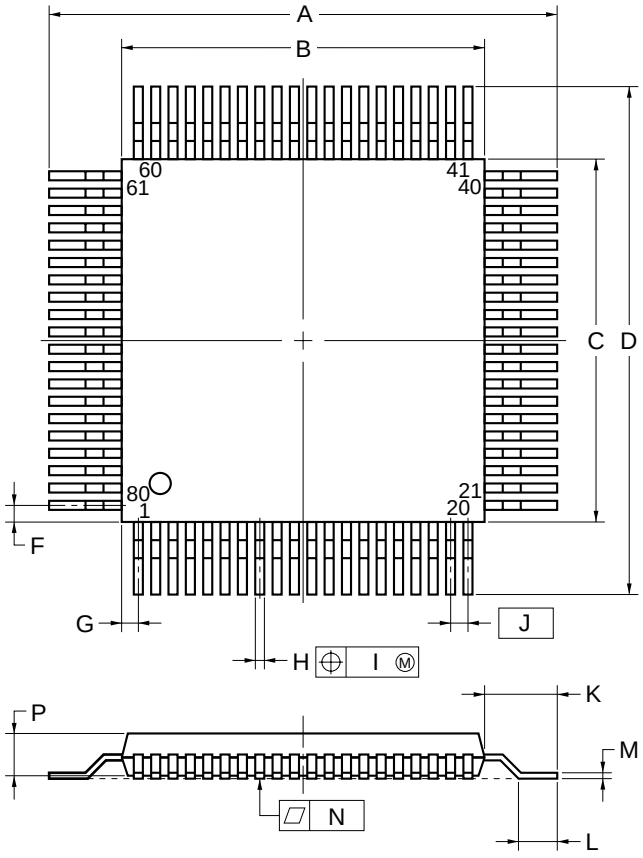


DATA RETENTION CHARACTERISTICS

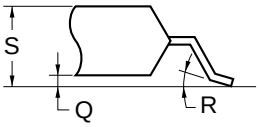


14. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

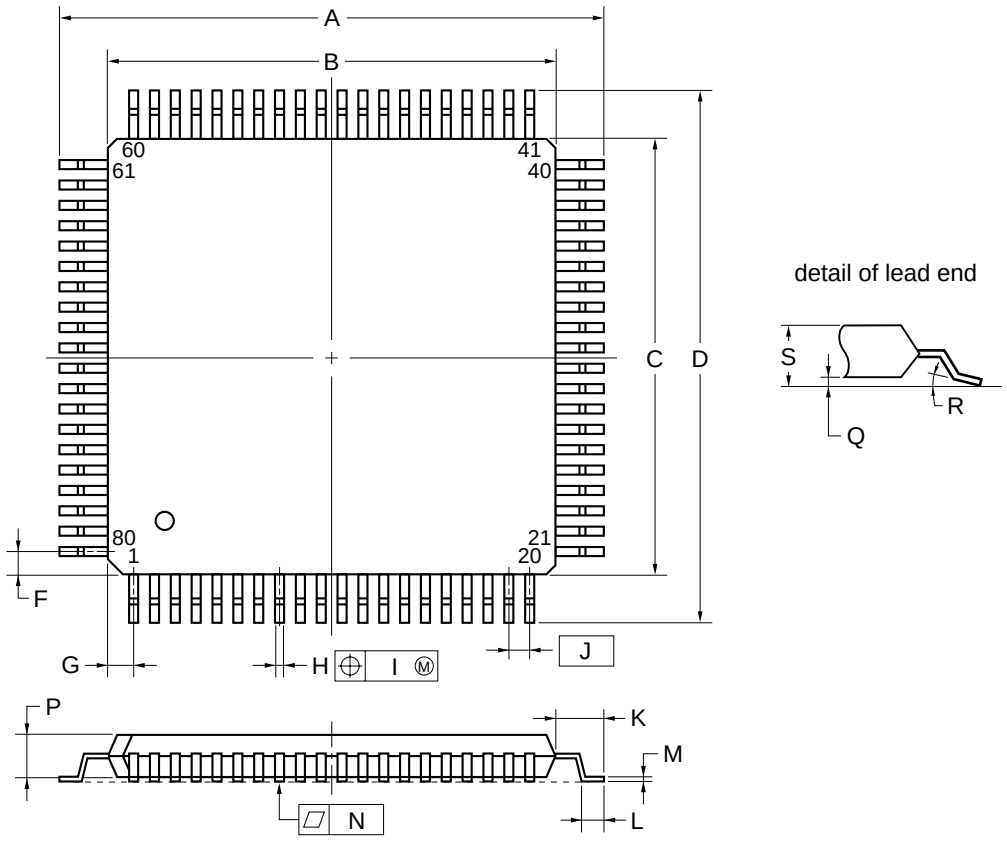
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

★ 80 PIN PLASTIC QFP (14×14)



NOTE

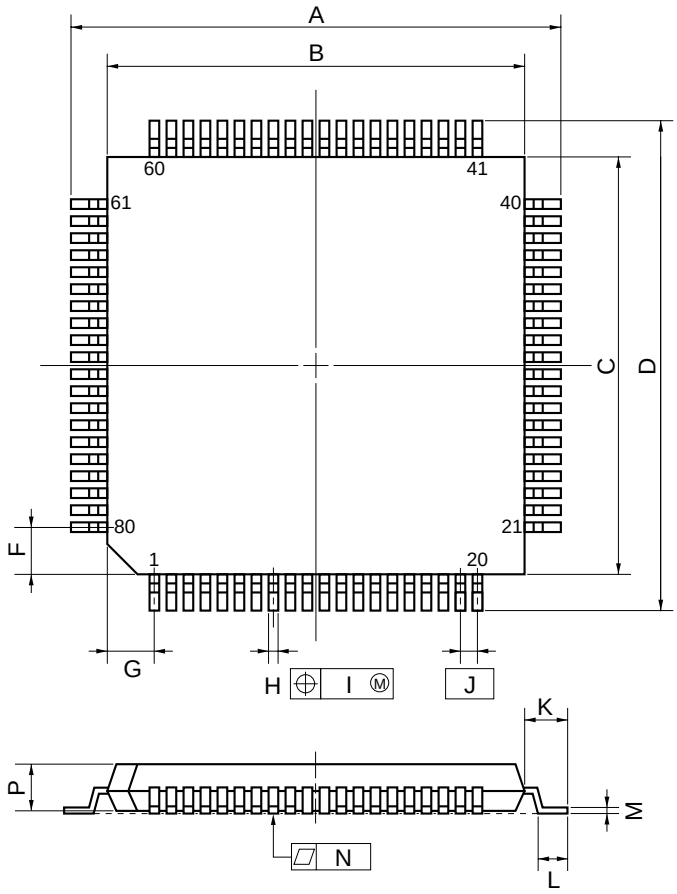
Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

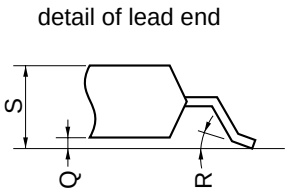
ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

★ 15. RECOMMENDED SOLDERING CONDITIONS

It is recommended that the μPD784035Y, 784036Y, 784037Y, and 784038Y be soldered under the following conditions.

For details on the recommended soldering conditions, refer to information document "Semiconductor Device Mounting Technology Manual" (C10535E).

For soldering methods and conditions other than those recommended, please consult an NEC representative.

Caution The soldering conditions for the μPD784035YGK-×××-BE9 and 784036YGK-×××-BE9 are undefined because these products are currently under development.

Table 15-1. Soldering Conditions for Surface Mount Type (1/2)

(1) μPD784035YGC-×××-3B9: 80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)
μPD784036YGC-×××-3B9: 80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)
μPD784037YGC-×××-3B9: 80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)
μPD784038YGC-×××-3B9: 80-pin plastic QFP (14 × 14 mm, 2.7-mm thick)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or less (210°C or more) Number of reflow processes: 3 or less	IR35-00-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or less (200°C or more) Number of reflow processes: 3 or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C or less, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or less, Flow time: 3 seconds or less (for one side of the a device)	—

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method).

(2) μPD784035YGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)
μPD784036YGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)
μPD784037YGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)
μPD784038YGC-×××-8BT: 80-pin plastic QFP (14 × 14 mm, 1.4-mm thick)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or less (210°C or more) Number of reflow processes: 2 or less	IR35-00-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or less (200°C or more) Number of reflow processes: 2 or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C or less, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or less, Flow time: 3 seconds or less (for one side of the a device)	—

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method).

Table 15-1. Soldering Conditions for Surface Mount Type (2/2)

(3) μPD784037YGK-×××-BE9: 80-pin plastic TQFP (fine-pitch) (12 × 12 mm)
μPD784038YGK-×××-BE9: 80-pin plastic TQFP (fine-pitch) (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or less (210°C or more) Number of reflow processes: 2 or less Exposure limit: 7 days[Note] (10 hours of pre-baking is required at 125°C afterward)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or less (200°C or more) Number of reflow processes: 2 or less Exposure limit: 7 days[Note] (10 hours of pre-baking is required at 125°C afterward)	VP15-107-2
Partial heating	Pin temperature: 300°C or less, Flow time: 3 seconds or less (per side of a device)	—

Note Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for supporting development of a system using the μPD784038Y.

Language processor software

RA78K4[Note 1]	Assembler package common to 78K/IV Series
CC78K4[Note 1]	C compiler package common to 78K/IV Series
CC78K4-L[Note 1]	C compiler library source file common to 78K/IV Series

PROM writing tool

PG-1500	PROM program writer
PA-78P4026GC PA-78P4038GK PA-78P4026KK	Programmer adapter connected to PG-1500
PG-1500 controller[Note 2]	PG-1500 control program

Debugging tool

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-784000-R-BK	Break board common to 78K/IV Series
IE-784038-R-EM1 IE-784000-R-EM	Emulation board for evaluation of μPD784038Y Subseries
IE-70000-98-IF-B	Interface adapter when PC-9800 series (except notebook type) is used as host machine
IE-70000-98N-IF	Interface adapter and cable when notebook type PC-9800 series is used as host machine
IE-70000-PC-IF-B	Interface adapter when IBM PC/AT™ is used as host machine
IE-78000-R-SV3	Interface adapter and cable when EWS is used as host machine
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-3B9, GC-8BT type) common to μPD784038Y Subseries
EP-78054GK-R	Emulation probe for 80-pin plastic TQFP (fine pitch) (GK-BE9 type) common to μPD784038Y Subseries
EV-9200GC-80	Socket mounted on board of target system created for 80-pin plastic QFP (GC-3B9, GC-8BT type)
TGK-080SDW	Adapter mounted on board of target system created for 80-pin plastic TQFP (fine pitch) (GK-BE9)
EV-9900	Jig used to remove μPD78P4038YKK-T from EV-9200GC-80
SM78K4[Note 3]	System simulator common to 78K/IV Series
ID78K4[Note 3]	Integrated debugger for IE-784000-R
DF784038[Note 4]	Device file for μPD784038Y Subseries

Real-time OS

RX78K/IV[Note 4]	Real-time OS for 78K/IV Series
MX78K4[Note 2]	OS for 78K/IV Series

Notes. 1.
- PC-9800 series (MS-DOS™) base
- IBM PC/AT and compatible machine (PC DOS™, Windows™, MS-DOS, IBM DOS™) base
- HP9000 series 700™ (HP-UX™) base
- SPARCstation™ (SunOS™) base
- NEWS™ (NEWS-OS™) base

2.
- PC-9800 series (MS-DOS) base
- IMB PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base

3.
- PC-9800 series (MS-DOS+Windows) base
- IBM PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base
- HP9000 series 700 (HP-UX) base
- SPARCstation (SunOS) base

4.
- PC-9800 series (MS-DOS) base
- IBM PC/AT and compatible machine (PC DOS, Windows, MS-DOS, IBM DOS) base
- HP9000 series 700 (HP-UX) base
- SPARCstation (SunOS) base

Remarks 1. RA78K4, CC78K4, SM78K4, and ID78K4 are used in combination with DF784038.

2. The TGK-080SDW is a product of TOKYO ELETECH CORPORATION (Tokyo, 03-5295-1661). Consult an NEC sales representative about purchasing.

APPENDIX B RELATED DOCUMENTS

Documents related to device

Document Name	Document No.	
	Japanese	English
μPD784031Y Data Sheet	U11504J	U11504E
μPD784035Y, 784036Y, 784037Y, 784038Y Data Sheet	U10741J	This manual
μPD78P4038Y Data Sheet	U10742J	U10742E
μPD784038, 784038Y Subseries User's Manual - Hardware	U11316J	U11316J
μPD784038Y Subseries Special Function Register Table	U11091J	–
78K/IV Series User's Manual - Instructions	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note - Software Basics	U10095J	U10095E

Documents related to development tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	—
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K4 Series	Operation	EEU-960	—
	Language	EEU-961	—
CC78K Series Library Source File		U12322J	—
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller - PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller - IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-784000-R		EEU-5004	EEU-1534
IE-784038-R-EM1		U11383J	U11383E
EP-78230		EEU-985	EEU-1515
EP-78054GK-R		EEU-932	EEU-1468
SM78K4 System Simulator - Windows Based	Reference	U10093J	U10093E
SM78K Series System Simulator	External component user open interface specification	U10092J	U10092E
ID78K4 Integrated Debugger - Windows Based	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP9000 Series 700 (HP-UX) Based	Reference	U11960J	Under preparation

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of a document for designing.

Documents related to embedded software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Basics	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	—
78K/IV Series OS MX78K4	Basics	U11779J	—

Other documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	C11893J	MEI-1202
Guide to Microcontroller-Related Products by Third Parties	U11416J	—

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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