DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78F9177, 78F9177Y

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F9177 and μPD78F9177Y are μPD789177, 789177Y Subseries (small, general-purpose) in the 78K/0S Series.

The μPD78F9177 replaces the internal ROM of the μPD789176 and μPD789177 with flash memory, while the μPD78F9177Y replaces the ROM of the μPD789176Y and μPD789177Y with flash memory.

Because flash memory allows the program to be written and erased electrically with the device mounted on the board, this product is ideal for the evolution stages of system development, small-scale production and rapid development of new products.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual: U14186E
78K/0S Series User's Manual Instruction: U11047E

FEATURES

- Pin compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 24 Kbytes
- High-speed RAM: 512 bytes
- Minimum instruction execution time can be changed from high-speed (0.4 μs: @5.0-MHz operation with main system clock) to ultra-low-speed (122 μs: @ 32.768-kHz operation with subsystem clock)
- 10-bit resolution A/D converter: 8 channels
- I/O ports: 31
- Serial interface: 2 channels
  - 3-wire serial I/O mode / UART mode: 1 channel
  - ★ SMB (μPD78F9177Y only): 1 channel
- Timers: 6 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- On-chip 16-bit multiplier
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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The mark ★ shows major revised

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APPLICATIONS

Power windows, battery management unit, side air bags, etc

ORDERING INFORMATION

(1) μPD78F9177

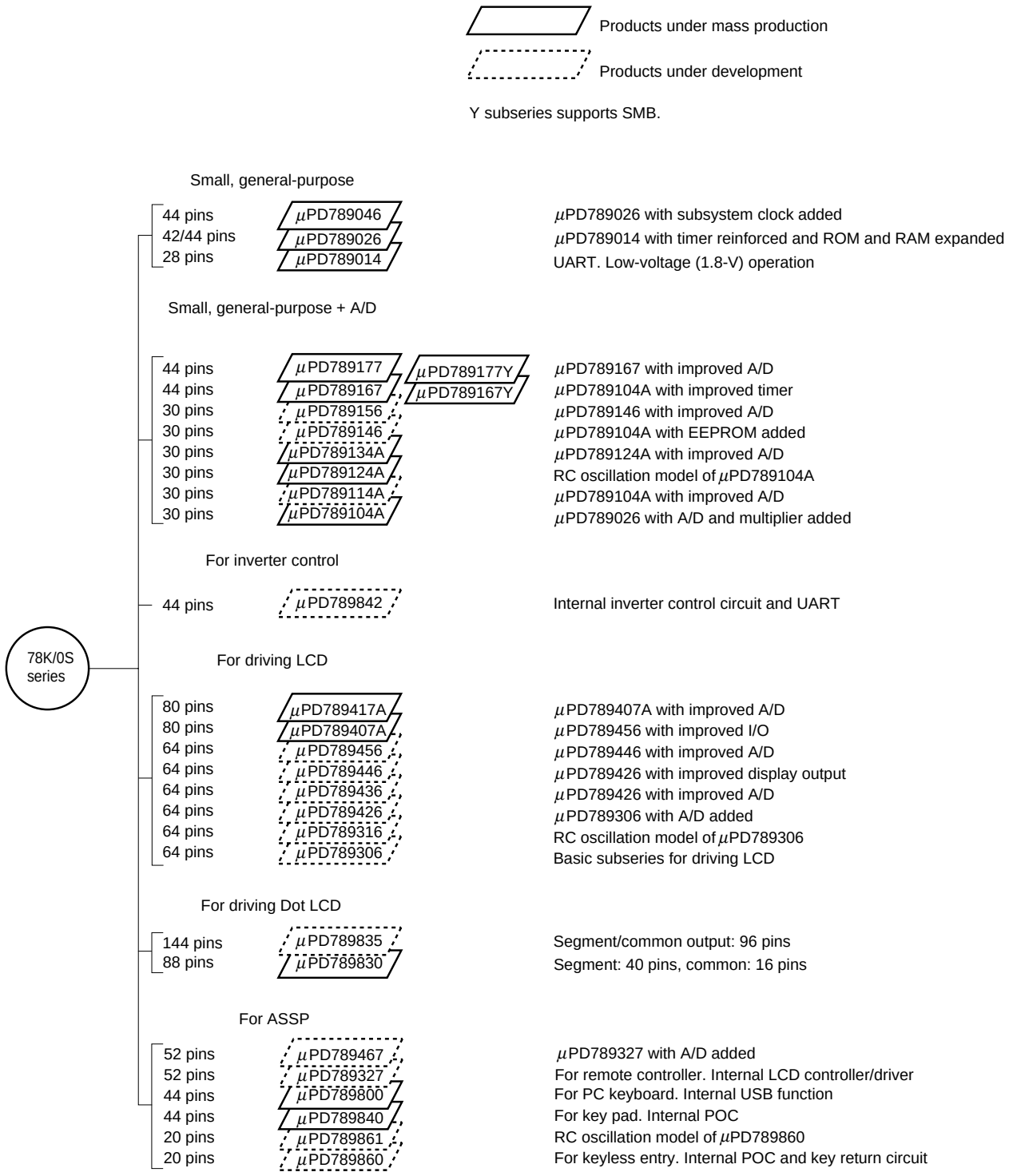
Part Number	Package
μPD78F9177GB-8ES	44-pin plastic QFP (10 × 10)

★ **(2) μPD78F9177Y**

Part Number	Package
μPD78F9177YGB-8ES	44-pin plastic LQFP (10 X 10)
μPD78F9177YGA-9EU	48-pin plastic TQFP (fine pitch) (7 X 7)

★ 78K/0S SERIES DEVELOPMENT

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major differences between subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	Serial Interface	I/O	V_{DD} MIN Value	Remark
			8-bit	16-bit	Watch	WDT						
Small, general-purpose	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART:1 ch)	34 pins	1.8 V	–
	μPD789026	4 K-16 K			–							
	μPD789014	2 K-4 K	2 ch	–						22 pins		
Small, general-purpose + A/D	μPD789177	16 K-24 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31 pins	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 K-16 K	1 ch		–		–	4 ch		20 pins		Internal EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K-8 K						4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
For inverter control	μPD789842	8 K-16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30 pins	4.0 V	–
For LCD driving	μPD789417A	12 K-24 K	3 ch	1 ch	1 ch	1 ch		7 ch	1 ch (UART: 1 ch)	43 pins	1.8 V	–
	μPD789407A						7 ch	–				
	μPD789456	12 K-16 K	2 ch				–	6 ch		30 pins		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40 pins		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16K					–		2 ch (UART: 1 ch)	23 pins		RC oscillation version
	μPD789306											–
For Dot LCD driving	μPD789835	24 K-60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch	28 pins	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30 pins	2.7 V	
ASSP	μPD789467	4 K-24 K	2 ch	–	1 ch	1 ch	1 ch	–	–	18 pins	1.8 V	Internal LCD
	μPD789327						–		1 ch	21 pins		
	μPD789800	8 K	2 ch	1 ch	–	1 ch	–		2 ch (USB: 1 ch)	31 pins	4.0 V	–
	μPD789840						4 ch		1 ch	29 pins	2.8 V	
	μPD789861	4 K		–			–		–	14 pins	1.8 V	RC oscillation version, Internal EEPROM
	μPD789860											Internal EEPROM

Note 10-bit timer: 1 channel

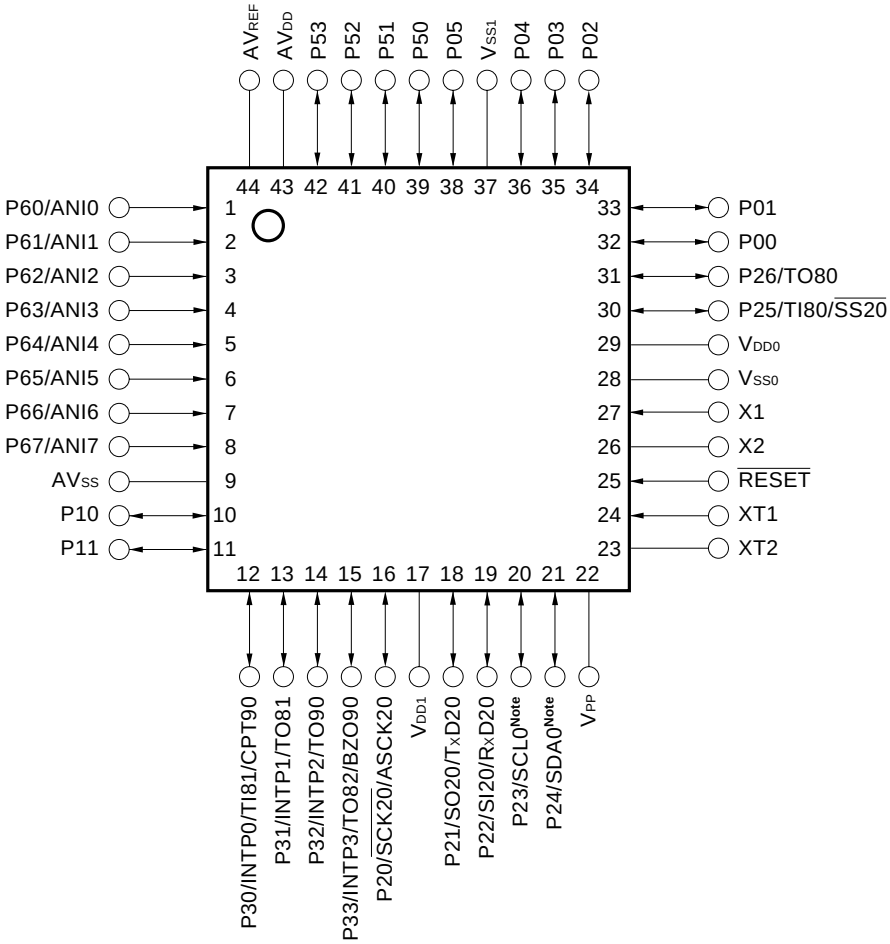
OVERVIEW OF FUNCTIONS

Item		μPD78F9177	μPD78F9177Y
Internal memory	Flash memory	24 Kbytes	
	High-speed RAM	512 bytes	
Minimum instruction execution time		• 0.4/1.6 μs (@5.0-MHz operation with main system clock) • 122 μs (@ 32.768-kHz operation with subsystem clock)	
General-purpose registers		8 bits × 8 registers	
Instruction set		• 16-bit operations • Bit manipulations (set, reset, test)	
Multiplier		8 bits × 8 bits = 16 bits	
I/O ports		Total: 31 • CMOS input: 8 • CMOS I/O: 17 • N-ch open drain: 6	
A/D converters		10-bit resolution × 8 channels	
★ Serial interfaces		3-wire serial I/O/UART : 1 channel	• 3-wire serial I/O / UART: 1 channel • SMB: 1 channel
Timers		• 16-bit timer:1 channel • 8-bit timer/event counter:2 channels • 8-bit timer:1 channel • Watch timer:1 channel • Watchdog timer:1 channel	
Timer output		4 output	
Buzzer output		1	
Vectored interrupt sources	Maskable	Internal: 10, External: 4 (μPD78F9177)	
		Internal: 12, External: 4 (μPD78F9177Y)	
	Non-maskable	Internal: 1	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40°C to +85°C	
★ Package		44-pin plastic LQFP (10 × 10)	• 44-pin plastic LQFP (10 X10) • 48-pin plastic TQFP (fine pitch) (7 x 7)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **44-pin plastic LQFP (10 × 10)**
  μPD78F9177GB-8ES
  μPD78F9177YGB-8ES



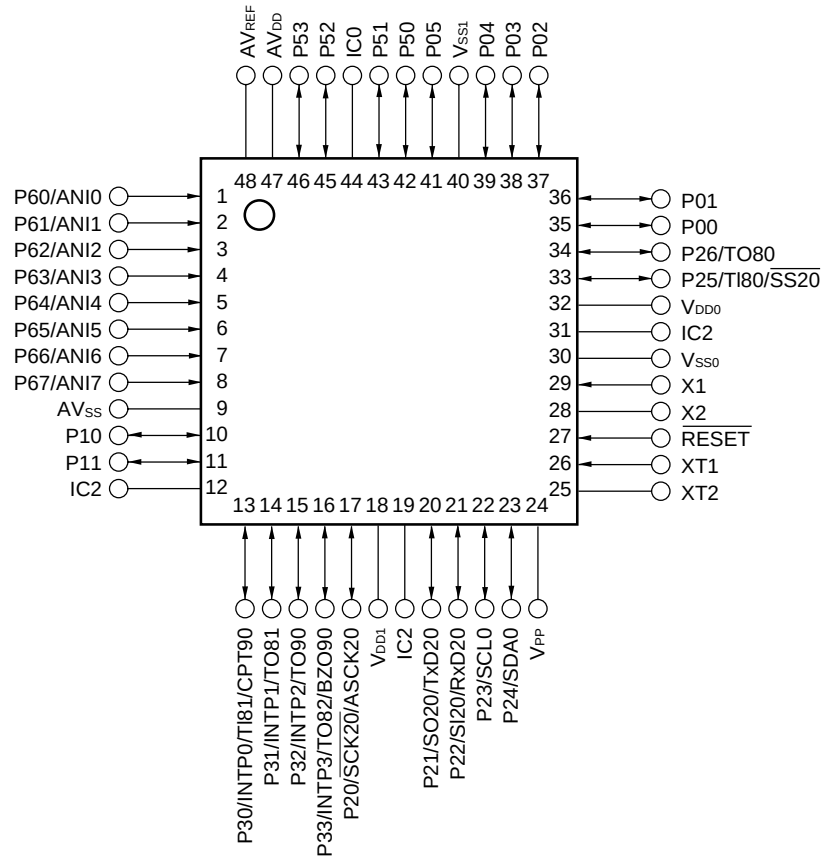
Note The SCL0 and SDA0 pins are available in μPD78F9177Y product only.

Cautions 1. Connect the V_{PP} pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{DD} pin to V_{DD0}.

3. Connect the AV_{SS} pin to V_{SS0}.

★ • **44-pin plastic QFP (fine pitch) (7 × 7)**
μPD78F9177YGA-9EU



Cautions 1. Connect the V_{PP} pin directly to the V_{SS0} or V_{SS1} pin in normal operation mode.

2. Connect the IC0 (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

3. Leave the IC2 pin open.

4. Connect the AV_{DD} pin to V_{DD0}.

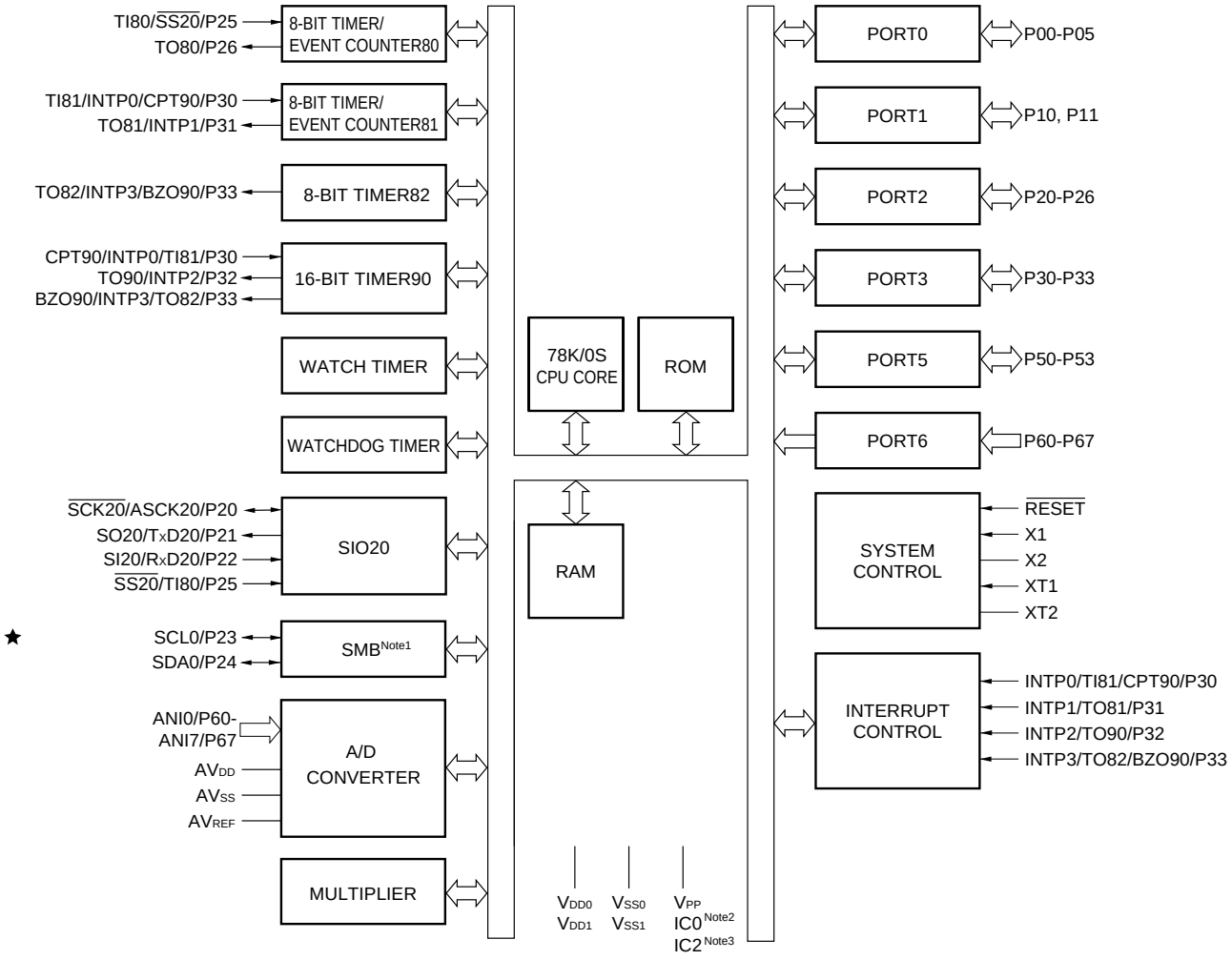
5. Connect the AV_{SS} pin to V_{SS0}.

ANI0 to ANI7:	Analog Input	$\overline{\text{RESET}}$:	Reset
ASCK20:	Asynchronous Serial Input	RxD20:	Receive Data
AV_{DD}:	Analog Power Supply	$\overline{\text{SCK20}}$:	Serial Clock (for SIO20)
AV_{REF}:	Analog Reference Voltage	SCL0 [Note2]:	Serial Clock (for SMB0)
AV_{SS}:	Analog Ground	SDA0 [Note2]:	Serial Data
BZO90:	Buzzer Output	SI20:	Serial Input
CPT90:	Capture Trigger Input	SO20:	Serial Output
IC0 [Note1],IC2 [Note2]:	Internally Connected	$\overline{\text{SS20}}$:	Chip Select Input
INTP0 to INTP3:	Interrupt from Peripherals	TI80, TI81:	Timer Input
P00 to P05:	Port 0	TO80 to TO82, TO90:	Timer Output
P10, P11:	Port 1	TxD20:	Transmit Data
P20 to P26:	Port 2	V_{DD0}, V_{DD1}:	Power Supply
P30 to P33:	Port 3	V_{PP}:	Programming Power Supply
P50 to P53:	Port 5	V_{SS0}, V_{SS1}:	Ground
P60 to P67:	Port 6	X1, X2:	Crystal (Main System Clock)
		XT1, XT2:	Crystal (Subsystem Clock)

Notes 1. The IC0 pin is available in 48-pin plastic TQFP (fine pitch) only.

2. The IC2, SCL0, and SDA0 pins are available in μPD78F9177Y product only.

2. BLOCK DIAGRAM



Notes 1. SMB is available in μPD78F9177Y product only.

2. The IC0 pin is available in 48-pin plastic TQFP (fine pitch) only.

3. The IC2 pin is available in μPD78F9177Y product only.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P05	I/O	Port 0 6-bit input/output port Input/output mode can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	–
P10, P11	I/O	Port 1 2-bit input/output port Input/output mode can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by software.	Input	–
P20	I/O	Port 2 7-bit input/output port Input/output mode can be specified in 1-bit units For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by software. Only P23 and P24 can be used as N-ch open-drain input/output port pins.	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
★ P23				SCL0 Note
★ P24				SDA0 Note
P25				TI80/$\overline{\text{SS20}}$
P26				TO80
P30	I/O	Port 3 4-bit input/output port Input/output mode can be specified in 1-bit units On-chip pull-up resistor can be specified by software.	Input	INTP0/TI81/CPT90
P31				INTP1/TO81
P32				INTP2/TO90
P33				INTP3/TO82/BZO90
P50 to P53	I/O	Port 5 4-bit N-ch open-drain input/output port Input/output mode can be specified in 1-bit units	Input	–
P60 to P67	Input	Port 6 8-bit input-only port	Input	ANI0 to ANI7

Note μPD78F9177Y only

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI81/CPT90
INTP1				P31/TO81
INTP2				P32/TO90
INTP3				P33/TO82/BZO90
SI20	Input	Serial data input to serial interface	Input	P22/RxD20
SO20	Output	Serial data output from serial interface	Input	P21/TxD20
$\overline{SCK20}$	I/O	Serial clock input/output for serial interface	Input	P20/ASCK20
$\overline{SS20}$	Input	Chip select input to serial interface	Input	P25/TI80
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{SCK20}$
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
★ SCL0 Note1	I/O	SMB0 clock input/output	Input	P23
★ SDA0 Note1	I/O	SMB0 data input/output	Input	P24
TI80	Input	External count clock input to 8-bit timer/event counter (TM80)	Input	P25/$\overline{SS20}$
TI81	Input	External count clock input to 8-bit timer/event counter (TM81)	Input	P30/INTP0/CPT90
TO80	Output	8-bit timer/event counter (TM80) output	Input	P26
TO81	Output	8-bit timer/event counter (TM81) output	Input	P31/INTP1
TO82	Output	8-bit timer (TM82) output	Input	P33/INTP3/BZO90
TO90	Output	16-bit timer (TM90) output	Input	P32/INTP2
BZO90	Output	16-bit timer (TM90) Buzzer output	Input	P33/INTP3/TO82
CPT90	Input	Capture edge input	Input	P30/INTP0/TI81
ANI0 to ANI7	Input	A/D converter analog input	Input	P60 to P67
AV_{REF}	–	A/D converter reference voltage	–	–
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}	–	A/D converter analog power supply	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
V_{DD0}	–	Positive power supply	–	–
V_{DD1}	–	Positive power supply (other than ports)	–	–
V_{SS0}	–	Ground potential	–	–
V_{SS1}	–	Ground potential (other than ports)	–	–
$\overline{RESET}$	Input	System reset input	Input	–
V_{PP}	–	Sets flash memory programming mode. Applies high voltage when a program is written or verified. Connect directly to V_{SS0} or V_{SS1} in normal operation mode.	–	–
IC0 Note2	–	Internally connected. Connect this pin directly to the V_{SS0} or V_{SS1} pin.	–	–
IC2 Note1	–	Internally connected. Leave this pin open.	–	–

Notes 1. μPD78F9177Y only.

2. 48-pin plastic TQFP (fine pitch) only.

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins is shown in Table 3-1. For the input/output circuit configuration of each type, refer to Figure 3-1.

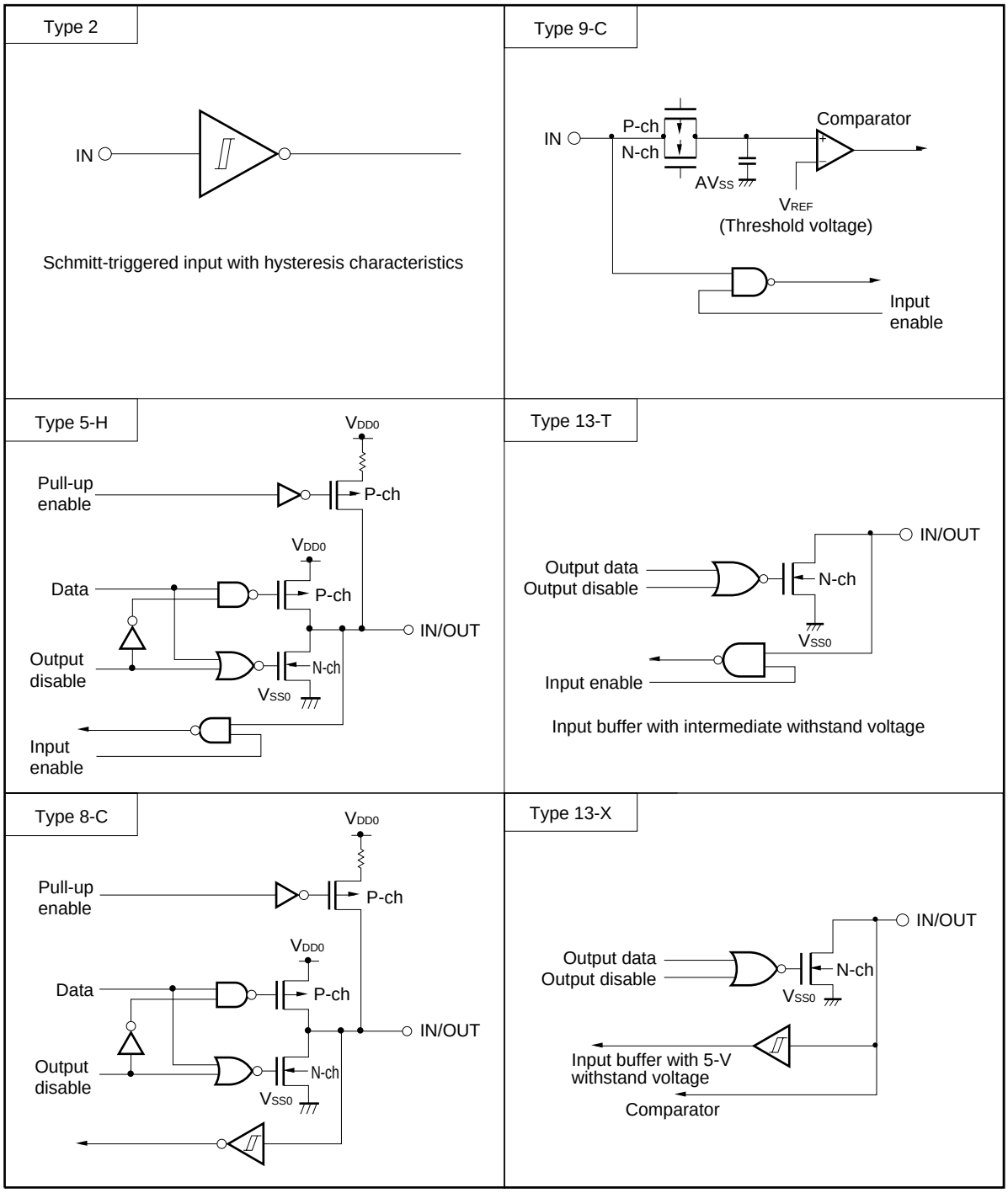
Table 3-1. Type of I/O Circuit for Each Pin and Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P05	5-H	I/O	Input: Independently connects to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1} via a resistor. Output: Leave open.
P10, P11			
P20/$\overline{SCK20}$/ASCK20	8-C		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23/SCL0[Note1]	13-X		Input: Independently connects to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P24/SDA0[Note1]			
P25/TI80/$\overline{SS20}$	8-C		Input: Independently connects to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1} via a resistor. Output: Leave open.
P26/TO80			
★ P30/INTP0/TI81/CPT90			Input: Independently connects to V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
★ P31/INTP1/TO81			
★ P32/INTP2/TO90			
★ P33/INTP3/TO82/BZO90			
P50 to P53	13-T		Input: Independently connects to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P60/ANI0 to P67/ANI7	9-C	Input	Connect directly to V_{DD0}, V_{DD1} or V_{SS0}, V_{SS1}.
XT1	–	Input	Connect to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
V_{PP}	–	–	Connect directly to V_{SS0} or V_{SS1}.
IC0 [Note2]			
IC2 [Note1]			Leave open.

Notes 1. The IC2, SCL0, and SDA0 pins are available in μPD78F9177Y product only.

2. 48-pin plastic TQFP (fine pitch) only.

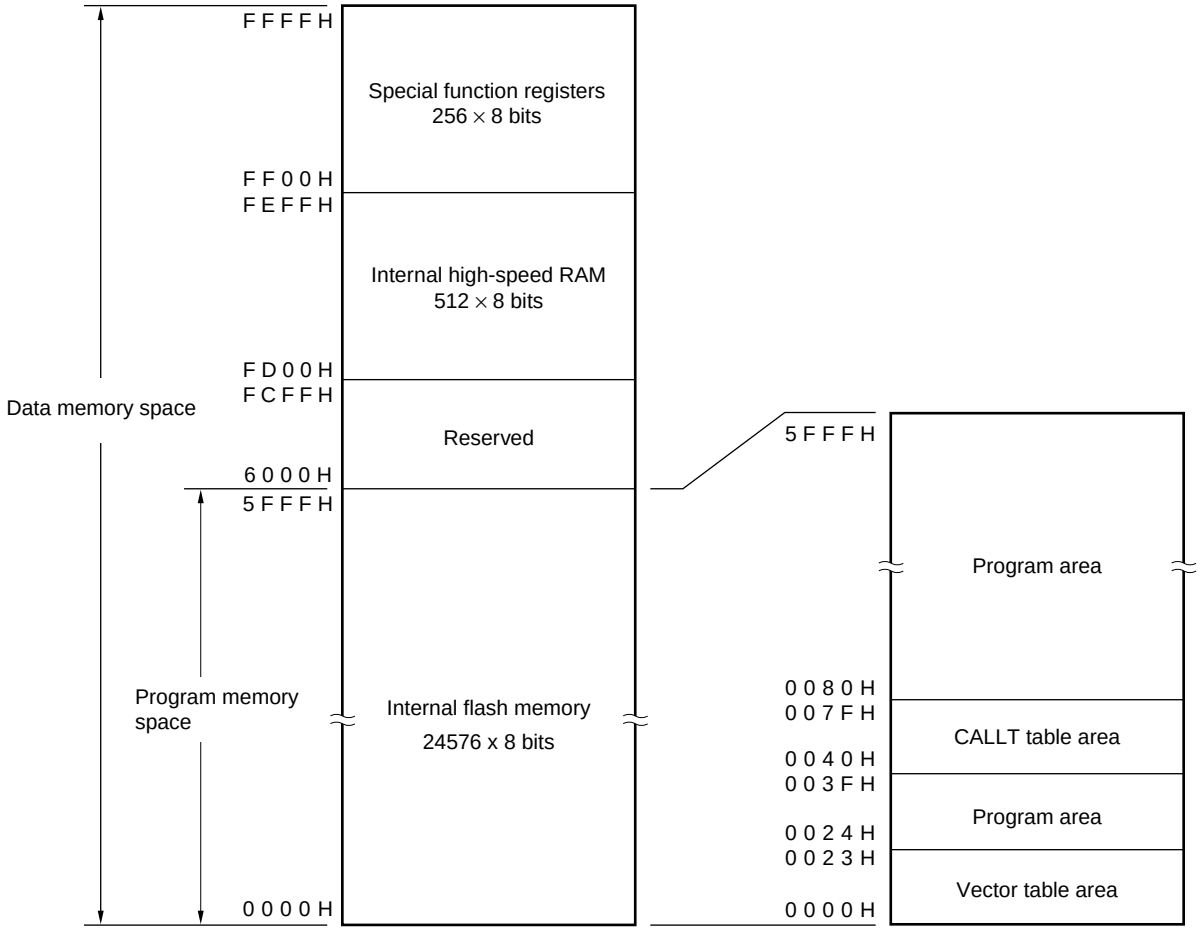
Figure 3-1. Pin Input/Output Circuits



4. CPU ARCHITECTURE

Products in the μPD78F9177 and μPD78F9177Y can access up to 64 Kbytes of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



5. FLASH MEMORY PROGRAMMING

The on-chip program memory in the μPD78F9177 and μPD78F9177Y is flash memory.

The flash memory can be written with the μPD78F9177 and μPD78F9177Y mounted on the target system (on-board). Connect the dedicated flash programmer (Flashpro III (part number: FL-PR3, PG-FP3)) to the host machine and target system to write the flash memory.

Remark FL-PR3 is made by Naito Densei Machida Mfg. Co., Ltd.

5.1 Selecting Communication Mode

The flash memory is written by using Flashpro III and by means of serial communication. Select a communication mode from those listed in Table 5-1. To select a communication mode, the format shown in Figure 5-1 is used. Each communication mode is selected by the number of V_{PP} pulses shown in Table 5-1.

Table 5-1. Communication Mode

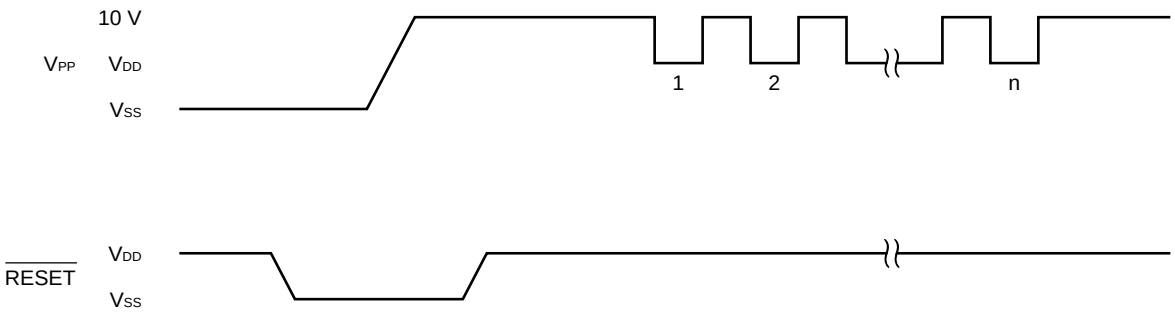
Communication Mode	Pins Used	Number of V_{PP} Pulses
3-wire serial I/O	$\overline{SCK20}$/ASCK20/P20 SO20/TxD20/P21 SI20/RxD20/P22	0
★ SMB Note1	SCL0/P23 SDA0/P24	4
UART	TxD20/SO20/P21 RxD20/SI20/P22	8
★ ★ Pseudo 3-wire mode Note2	P00 (Serial clock input) P01 (Serial data output) P02 (Serial data input)	12

Notes 1. μPD78F9177Y only

2. Serial transfer is performed by controlling a port by software.

Caution Be sure to select a communication mode based on the V_{PP} pulse number shown in Table 5-1.

Figure 5-1. Communication Mode Selection Format



5.2 Function of Flash Memory Programming

By transmitting/receiving commands and data in the selected communication mode, operations such as writing to the flash memory are performed. Table 5-2 shows the major functions of flash memory programming.

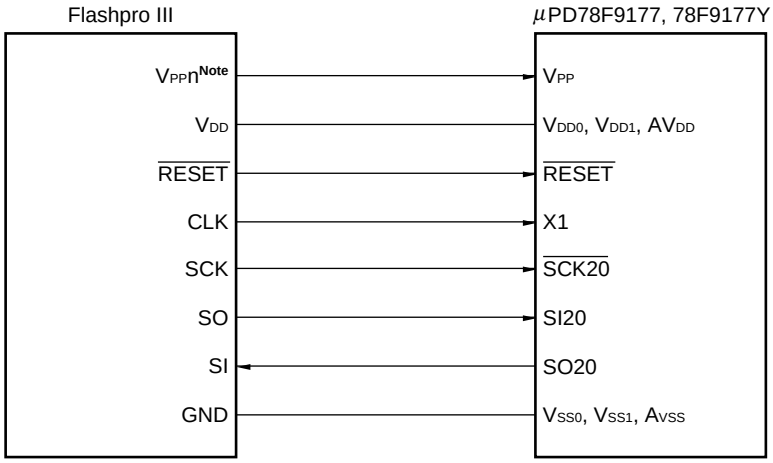
Table 5-2. Functions of Flash Memory Programming

Function	Description
Batch erase	Erases all contents of memory
Batch blank check	Checks erased state of entire memory
Data write	Write to flash memory based on write start address and number of data written (number of bytes)
Batch verify	Compares all contents of memory with input data

5.3 Flashpro III Connection Example

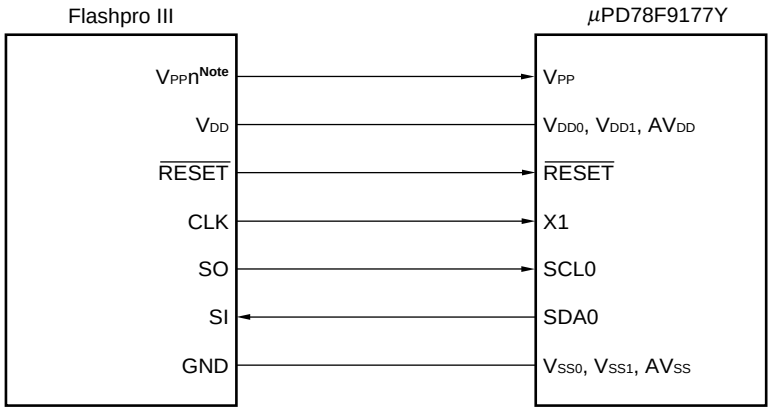
How the Flashpro III is connected to the μPD78F9177 and μPD78F9177Y differs depending on the communication mode (3-wired serial I/O, SMB, UART, or pseudo 3-wire mode). Figures 5-2 to 5-5 show the connection in the respective mode.

Figure 5-2. Flashpro III Connection in 3-wired Serial I/O Mode



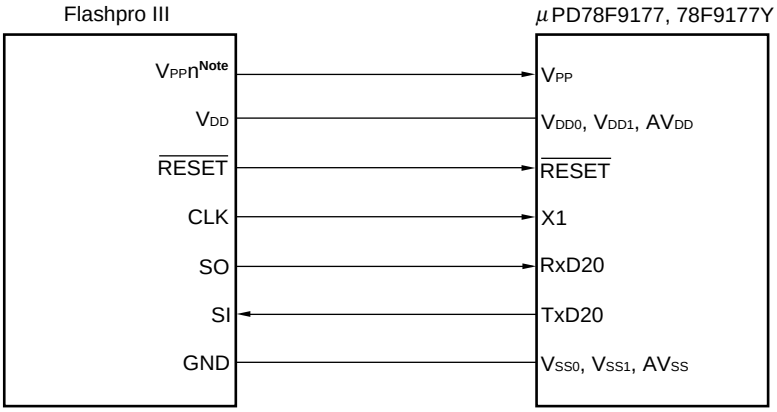
Note n = 1, 2

Figure 5-3. Flashpro III Connection in SMB Mode



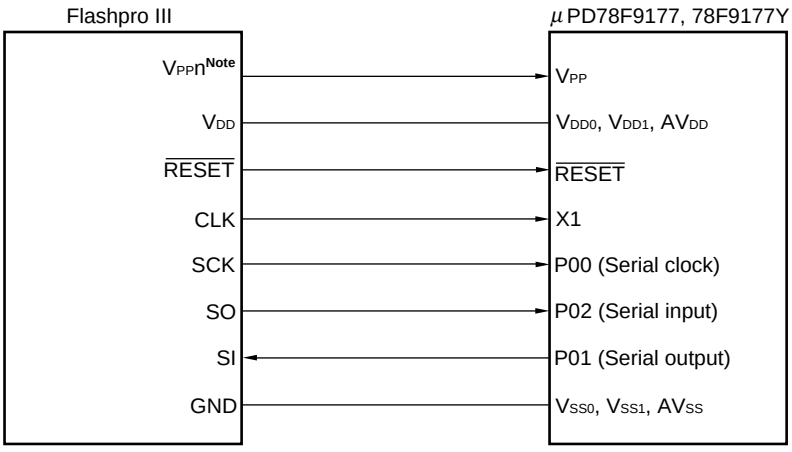
Note n = 1, 2

Figure 5-4. Flashpro III Connection in UART Mode



Note n = 1, 2

Figure 5-5. Flashpro III Connection in Pseudo Serial I/O Mode (When Port 0 is Used)



Note n = 1, 2

5.4 Example of Settings for Flashpro III (PG-FP3)

Set as follows when writing to flash memory using the Flashpro III (PG-FP3).

<1> Download the parameter file.

<2> Select the serial mode and the serial clock using the type command.

<3> The following is a setting example using the PG-FP3.

Table 5-3. Example Using PG-FP3

Communication mode	Setting example using PG-FP3		Number of V_{PP} pulses[Note1]
3-wired serial I/O mode	COMM PORT	SIO ch-0	0
	CPU CLK	On target board	
		In Flashpro	
	On target board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
SMB[Note2]	COMM PORT	IIC-ch0	4
	SLAVE ADDRESS	10H	
	IIC CLOCK	100 kHz	
	CPU CLOCK	In Flashpro	
	Flashpro Clock	4.0 MHz[Note3]	
	Multiple Rate	01.00	
UART	COMM PORT	UART-ch0	8
	CPU CLK	On target board	
	On target board	4.1943 MHz	
	UART BPS	9600 bps[Note4]	
Pseudo 3-wire mode	COMM PORT	Port A	12
	CPU CLK	On target board	
		In Flashpro	
	On target board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	

Notes 1. The number of V_{PP} pulses supplied from the Flashpro III during serial communication initialization. The pins to be used in communication are determined by this number of pulses.

2. μPD78F9177Y only.

3. Select one of 4.0 MHz or 3.125 MHz.

4. Select one of 9600 bps, 19200 bps, 38400 bps, or 76800 bps.

Remark COMM PORT : Selection of serial port
SIO CLK : Selection of serial clock frequency
CPU CLK : Selection of CPU clock source to be input

6. INSTRUCTION SET OVERVIEW

This section lists the μPD78F9177 and μPD78F9177Y instruction set.

6.1 Conventions

6.1.1 Operand identifiers and description methods

Operands are described in the "Operand" column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, $, and [ ], are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #,!, $, or [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 6-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7), AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH immediate data or label FE20H to FF1FH immediate data or label (even address only)
addr16 addr5	0000H to FFFFH immediate data or label (Only even addresses for 16-bit data transfer instructions) 0040H to 007FH immediate data or label (even address only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

6.1.2 Descriptions of the operation field

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Non-maskable interrupt servicing flag
( ): Memory contents indicated by address or register contents in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
∀: Exclusive OR
$\overline{\quad}$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

6.1.3 Description of the flag operation field

(Blank): Not affected
0: Cleared to 0
1: Set to 1
×: Set/cleared according to the result
R: Previously saved value is restored

6.2 Operations

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
MOV	r. #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r[Note 1]	2	4	A ← r			
	r, A[Note 1]	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ←→ X			
	A, r[Note 2]	2	6	A ←→ r			
	A, saddr	2	6	A ←→ (saddr)			
	A, sfr	2	6	A ←→ (sfr)			
	A, [DE]	1	8	A ←→ (DE)			
	A, [HL]	1	8	A ←→ (HL)			
	A, [HL + byte]	2	8	A ←→ (HL+byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp[Note 3]	1	4	AX ← rp			
	rp, AX[Note 3]	1	4	rp ← AX			

Notes 1. Except r = A

2. Except r = A, X

3. Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
XCHW	AX, rp[Note]	1	8	AX ←→ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A+ (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A+ (addr16) +CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A+ (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×

Note Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r– 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ←SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC_H ← (00000000, addr5 + 1) PC_L ← (00000000, addr5) SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP –– 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags
					Z AC CY
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	PC_H ← A, PC_L ← X	
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr.bit, $saddr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A.bit, $saddr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW.bit $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set Stop Mode	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

7. ELECTRICAL SPECIFICATIONS

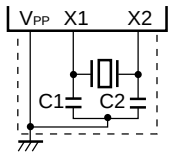
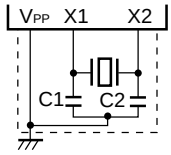
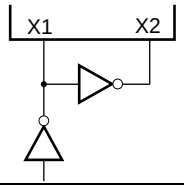
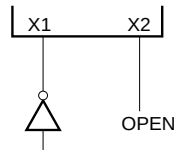
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$AV_{DD} - 0.3\ V \le V_{DD} \le AV_{DD} + 0.3\ V$	–0.3 to +6.5	V
	AV_{DD}	$AV_{REF} \le AV_{DD} + 0.3\ V$		V
	AV_{REF}	$AV_{REF} \le V_{DD} + 0.3\ V$		V
	V_{PP}		–0.3 to +10.5	V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24	–0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24	–0.3 to +5.5	V
	V_{I3}	P50 to P53	–0.3 to +13	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–10	mA
		Total for all pins	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	160	mA
Operating ambient temperature	T_A	In normal operation mode	–40 to +85	°C
★		During flash memory programming	+10 to +40	°C
Storage temperature	T_{stg}		–40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X) Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

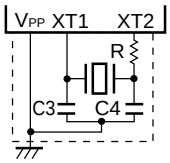
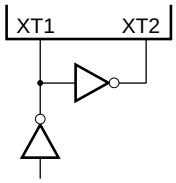
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) Note 1		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11,P60 to P67	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.9 V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		12	V
			V_{DD} = 1.8 to 5.5 V, T_A = 25 to +85°C	0.9 V_{DD}		12	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.9 V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$,P20 to P26, P30 to P33	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.4	V
				0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}	Pins other than P50 to P53 (N-ch open-drain) X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open-drain) X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3 Note	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	200	kΩ

Note A low-level input leakage current of -60 μA(MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 and P50 to P53 are set to input mode. At times other than this, -3 μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	5.0-MHz crystal oscillation operating mode (C1 = C2 = 22pF)	V_{DD} = 5.0 V ± 10% Note 4		5.0	15.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		2.0	5.0	mA
			V_{DD} = 2.0 V ± 10% Note 5		1.5	3.0	mA
	I_{DD2} Note 1	5.0-MHz crystal oscillation HALT mode (C1 = C2 = 22pF)	V_{DD} = 5.0 V ± 10% Note 4		2.0	6.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		1.0	2.5	mA
			V_{DD} = 2.0 V ± 10% Note 5		0.75	1.5	mA
	I_{DD3} Note 1	32.768-kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22pF, R = 220kΩ)	V_{DD} = 5.0 V ± 10%		250	750	μA
			V_{DD} = 3.0 V ± 10%		200	600	μA
			V_{DD} = 2.0 V ± 10%		150	450	μA
	I_{DD4} Note 1	32.768-kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22pF, R = 220kΩ)	V_{DD} = 5.0 V ± 10%		50	150	μA
			V_{DD} = 3.0 V ± 10%		30	90	μA
			V_{DD} = 2.0 V ± 10%		20	60	μA
	I_{DD5} Note 1	32.768-kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA
			V_{DD} = 2.0 V ± 10%		0.05	10	μA
	I_{DD6} Note 2	5.0-MHz crystal oscillation A/D operating mode (C1 = C2 = 22pF)	V_{DD} = 5.0 V ± 10% Note 4		6.0	17.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		3.0	7.0	mA
			V_{DD} = 2.0 V ± 10% Note 5		2.5	5.0	mA

Notes 1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and the port current (including the current flowing through the internal pull-up resistors) are not included.

2. The AV_{REF}On (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) are not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

5. During low-speed mode operation (when PCC is set to 02H)

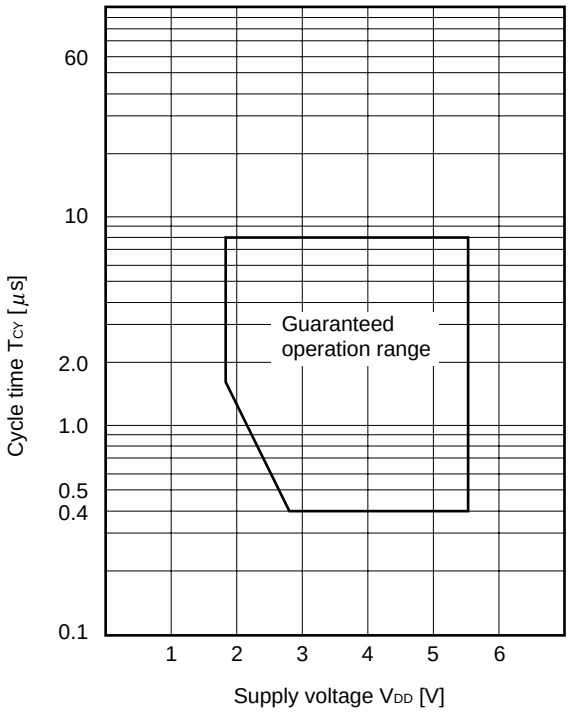
Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
				1.6		8	μs
		Operation based on the subsystem clock		114	122	125	μs
TI80 and TI81 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI80 and TI81 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			10			μs
CPT90 input high-/low-level width	t_{CPH}, t_{CPL}			10			μs

T_{CY} vs V_{DD} (main system clock)



(2) Serial interface (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
				3500			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns
SO20 setup time (when using $\overline{SS20}$, to $\overline{SS20}$ ↓)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
						400	ns
SO20 disable time (when using $\overline{SS20}$, from $\overline{SS20}$ ↑)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
						800	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
					19531	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
			3500			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
			1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
					9766	bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

★ **(3) Serial interface SMB0 (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V) (μPD78F9177Y only)**

(a) DC Characteristics

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	SCL0, SDA0 (at hysteresis)		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	SCL0, SDA0 (at hysteresis)		0		0.2 V_{DD}	V
Output voltage, high	V_{OL}	SCL0, SDA0	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
Input leakage current, high	I_{LIH}	SCL0, SDA0	$V_I = V_{DD}$			3	μA
Input leakage current, low	I_{LIL}	SCL0, SDA0	V_I = 0 V			–3	μA

(b) DC Characteristics (When using comparator)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input range	V_{SDA}, V_{SCL}	V_{DD} = 1.8 to 5.5 V	0		5.5	V
Transfer level	V_{ISDA}, V_{ISCL}	4.5 ≤ V_{DD} ≤ 5.5 V	0.72 V_{ISMB}	V_{ISMB}	1.28 V_{ISMB}	V
		3.3 ≤ V_{DD} < 4.5 V	0.78 V_{ISMB}	V_{ISMB}	1.22 V_{ISMB}	V
		2.7 ≤ V_{DD} < 3.3 V	0.75 V_{ISMB}	V_{ISMB}	1.25 V_{ISMB}	V
		1.8 ≤ V_{DD} < 2.7 V	0.90 V_{ISMB}	V_{ISMB}	1.45 V_{ISMB}	V
Input level threshold value	V_{ISMB}	LVL01, LVL00 = 0, 1		0.25 × V_{DD}		V
		LVL01, LVL00 = 1, 0		0.375 × V_{DD}		V
		LVL01, LVL00 = 1, 1		0.5 × V_{DD}		V

Note V_{ISMB} is an input level threshold value selected by bits LVL00 and LVL01 (bits 0 and 1 of SMB input level setting register 0 (SMBVI0)).

According to the SMB standard (V1.1), the maximum value of low-level input voltage is 0.8 V, and the minimum value of high-level input voltage, 2.1 V. To satisfy these conditions, set LVL01 and LVL00 as follows;

- When V_{DD} = 1.8 to 3.3 V: LVL01, LVL00 = 1, 1 (0.5 × V_{DD})
- When V_{DD} = 3.3 to 4.5 V: LVL01, LVL00 = 1, 0 (0.375 × V_{DD})
- When V_{DD} = 4.5 to 5.5 V: LVL01, LVL00 = 0, 1 (0.25 × V_{DD})

"LVL01, LVL00 = 0, 0" is not available since this setting does not satisfy the SMB standard (V1.1).

(c) AC Characteristics

Parameter		Symbol	SMB Mode		Standard Mode I^2C Bus		High-speed Mode I^2C Bus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	10	100	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	–	4.7	–	1.3	–	μs
Hold time Note1		$t_{HD:STA}$	4.0	–	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	4.7	–	0.6	–	μs
Stop condition setup time		$t_{SU:STO}$	4.0	–	4.0	–	0.6	–	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	–	–	5	–	–	–	μs
	When using SMB/IIC bus		300	–	–	–	0 Note2	900 Note3	ns
Data setup time		$t_{SU:DAT}$	250	–	250	–	100 Note4	–	ns
SCL0 clock low-level width		t_{LOW}	4.7	–	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	50	4.0	–	0.6	–	μs
SCL0 and SDA0 signal fall time		t_F	–	300	–	300	–	300	ns
SCL0 and SDA0 signal rise time		t_R	–	1000	–	1000	–	300	ns
Spike pulse width controlled by input filter		t_{SP}	–	–	–	–	0	50	ns
Timeout		$t_{TIMEOUT}$	25	35	–	–	–	–	ms
Total extended time of SCL0 clock low-level period (slave)		$t_{LOW:SEXT}$	–	25	–	–	–	–	ms
Total extended time of cumulative clock low-level period (master)		$t_{LOW:MEXT}$	–	10	–	–	–	–	ms
Capacitive load per each bus line		Cb	–	–	–	400	–	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

2. To fill in the underfined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I^2C bus is available in the SMB mode and the standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

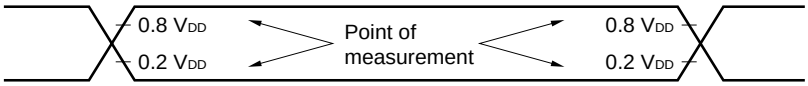
If the device extends the SCL0 signal low state hold time

$t_{SU:DAT} \geq 250$ ns

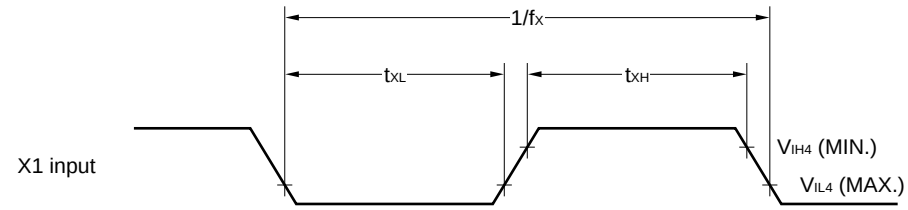
If the device extends the SCL0 signal low state hold time

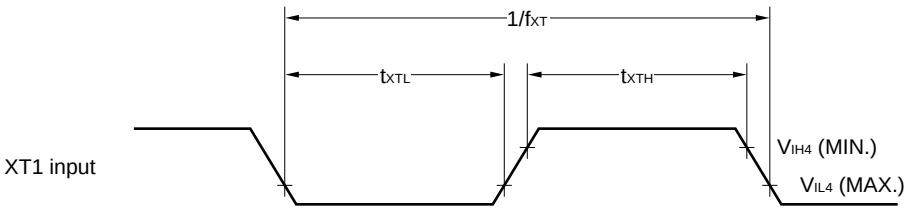
Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.}$+ $t_{SU:DAT}$ = 1000 + 250 = 1250 ns by the SMB mode or the standard mode I^2C bus specification).

AC Timing Measurement Points (excluding the X1 and XT1 inputs)

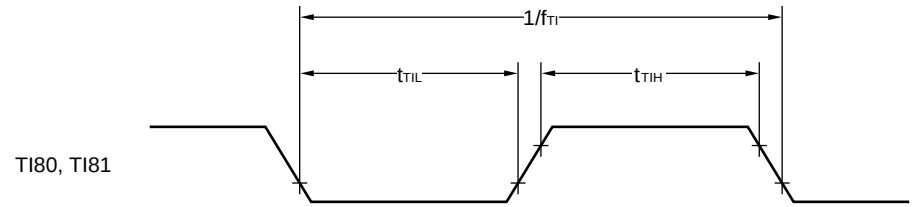


Clock Timing

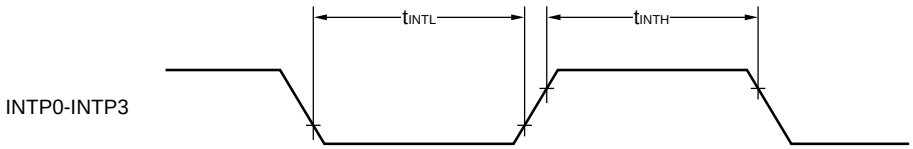




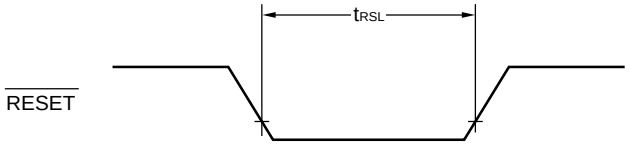
TI Timing



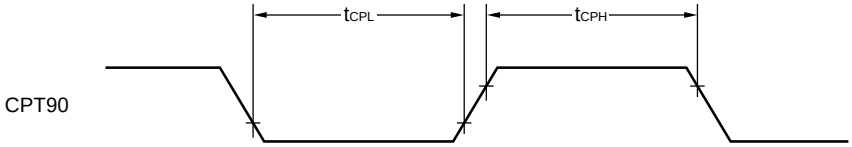
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

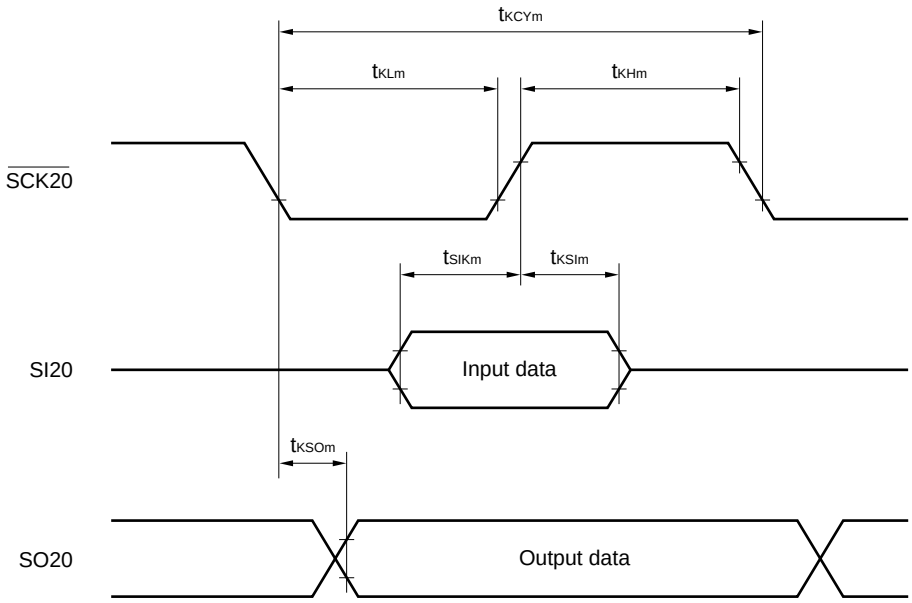


CPT90 Input Timing



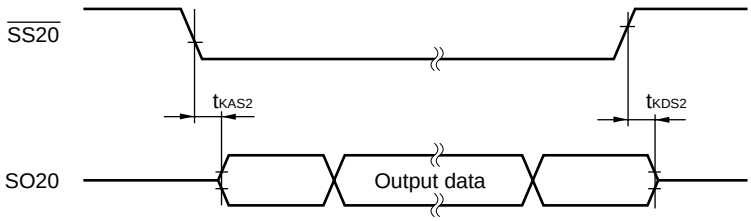
Serial Transfer Timing

3-wire serial I/O mode:

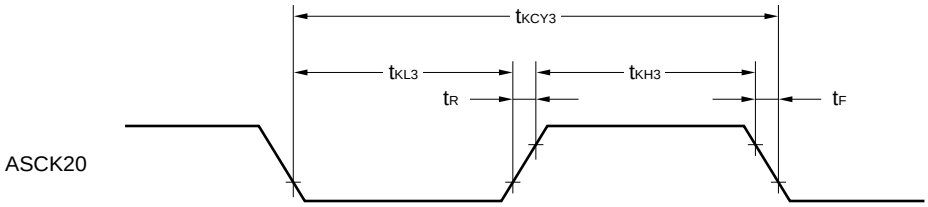


Remark m = 1, 2

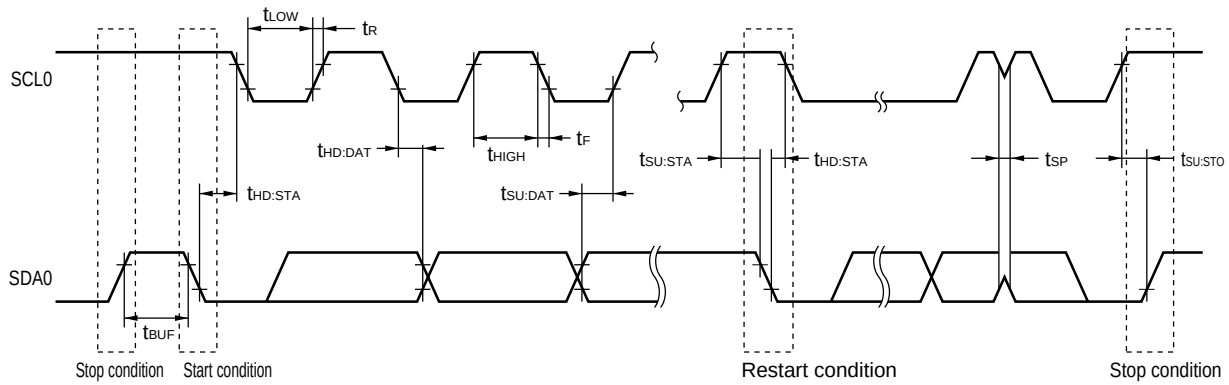
3-wire serial I/O mode (when using $\overline{SS20}$):



UART mode (external clock input):



SMB mode:


tLOW
tR
SCL0
tHD:DAT
tHIGH
tF
tSU:STA
tHD:STA
tSP
tSU:STO
tHD:STA
tSU:DAT
SDA0
tBUF
Stop condition
Start condition
Restart condition
Stop condition

10-Bit A/D Converter Characteristics (T_A = –40 to +85 °C, 1.8 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
Zero-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Full-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Integral linearity error[Note]	INL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±4.5	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±8.5	LSB
Differential linearity error[Note]	DNL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{AIREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

FLASH MEMORY WRITE/DELETE CHARACTERISTICS (T_A = 10 to 40 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current (V_{DD} pin) Note	I_{DDW}	When V_{PP} supply voltage = V_{PP1} (5.0-MHz crystal oscillation operation mode)			18	mA
Write current (V_{PP} pin) Note	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			7.5	mA
Delete current (V_{DD} pin) Note	I_{DDE}	When V_{PP} supply voltage = V_{PP1} (5.0-MHz crystal oscillation operation mode)			18	mA
Delete current (V_{PP} pin) Note	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			100	mA
Unit delete time	t_{er}		0.5	1	1	s
Total delete time	t_{era}				20	s
Write count		Delete/write are regarded as 1 cycle			20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		$0.2V_{DD}$	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

Note The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) and AV_{DD} current are not included.

Data Memory Stop Mode Low Power Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

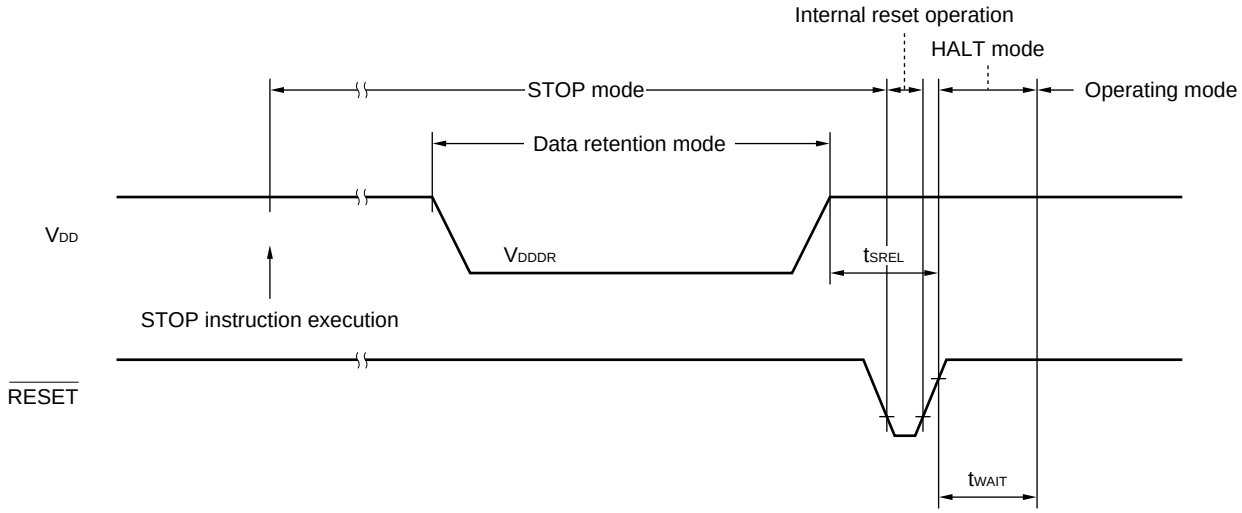
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 1	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

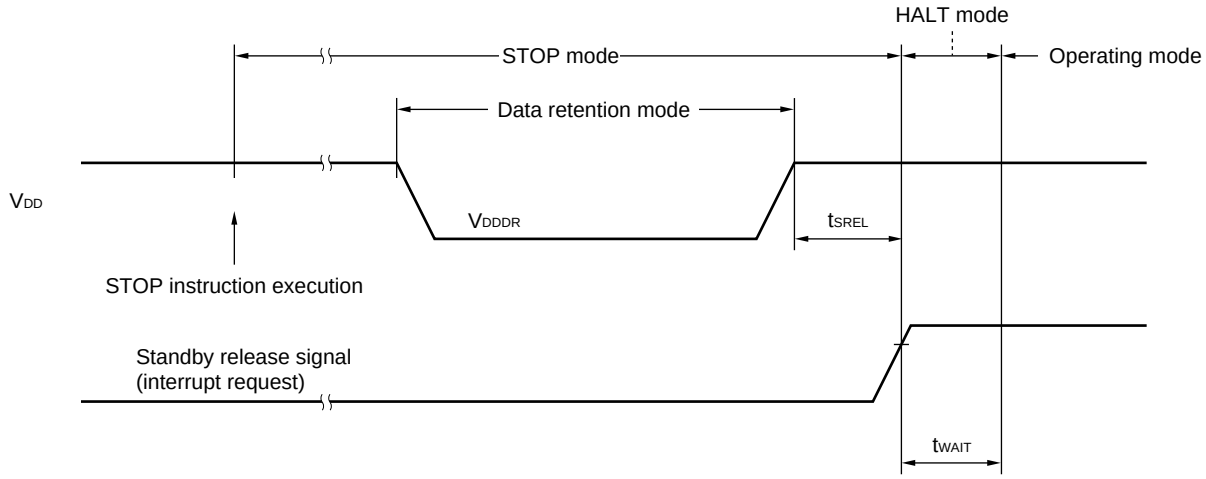
2. By using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS), $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected.

Remark f_X: Main system clock oscillation frequency

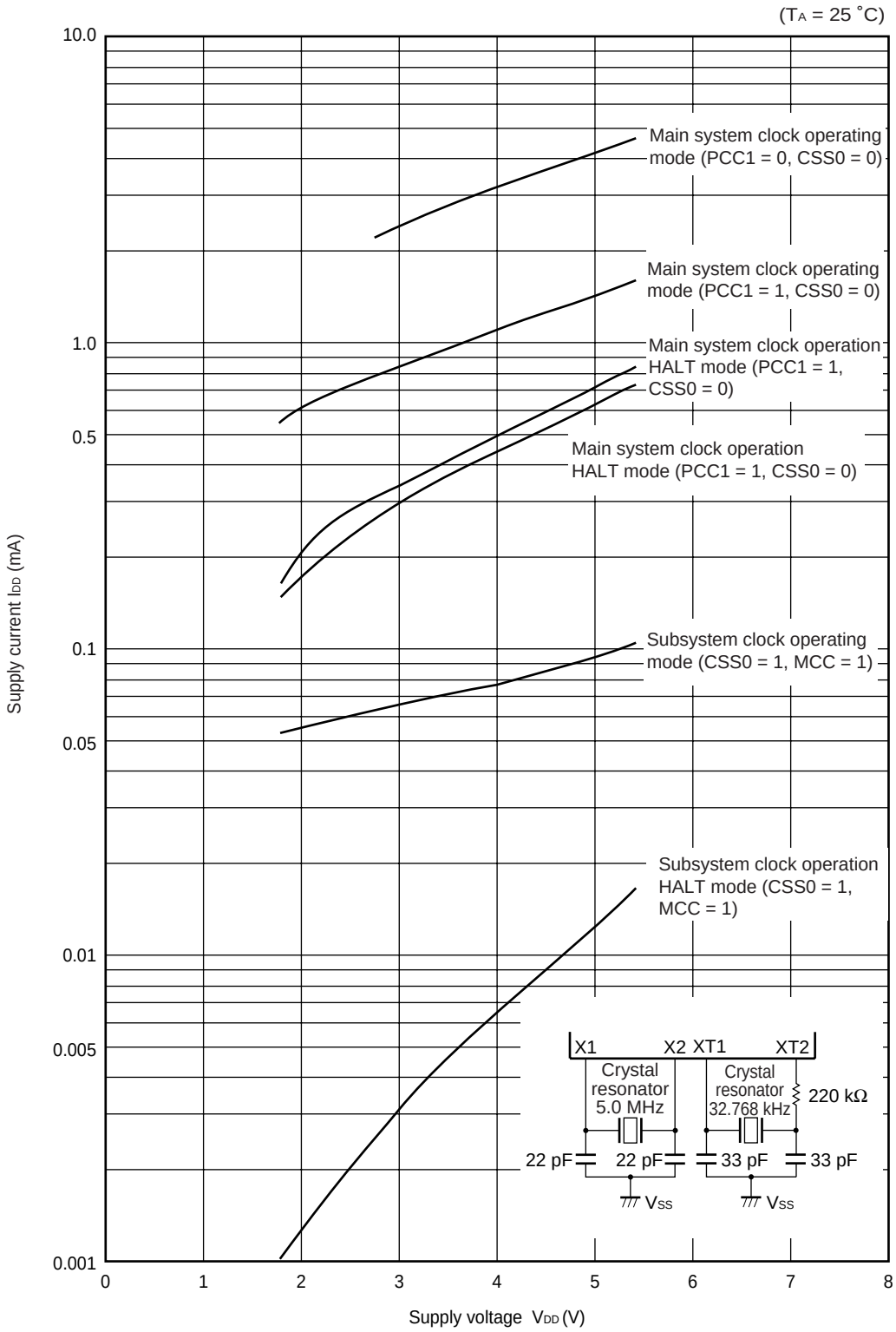
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

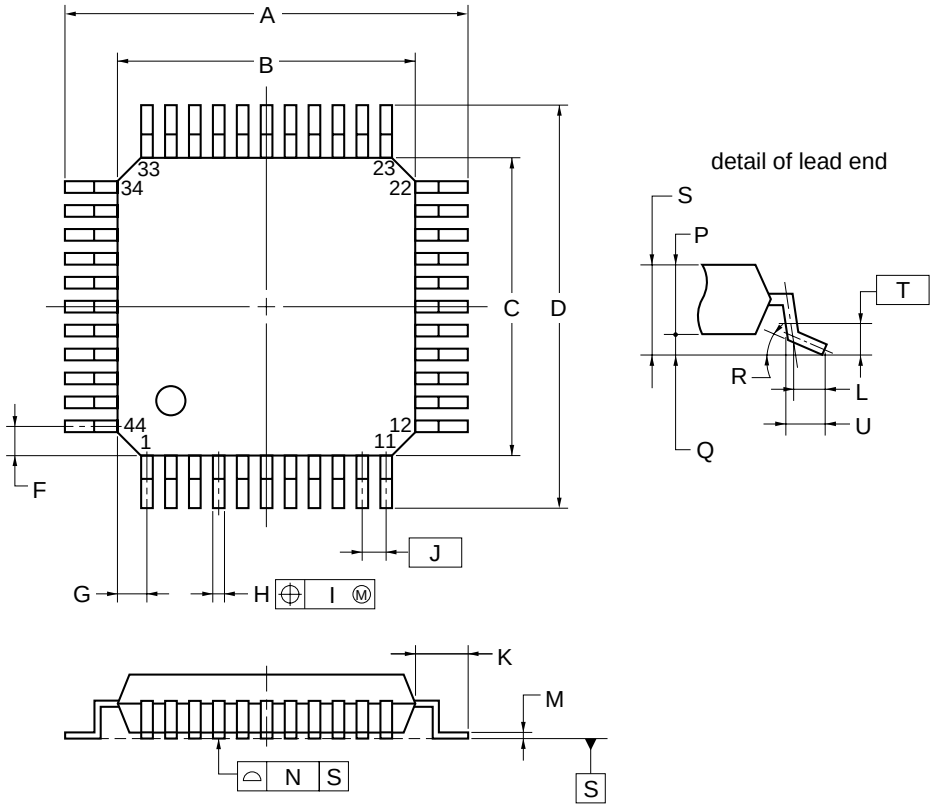


8. CHARACTERISTICS CURVES



9. PACKAGE DRAWING

44 PIN PLASTIC QFP (10x10)



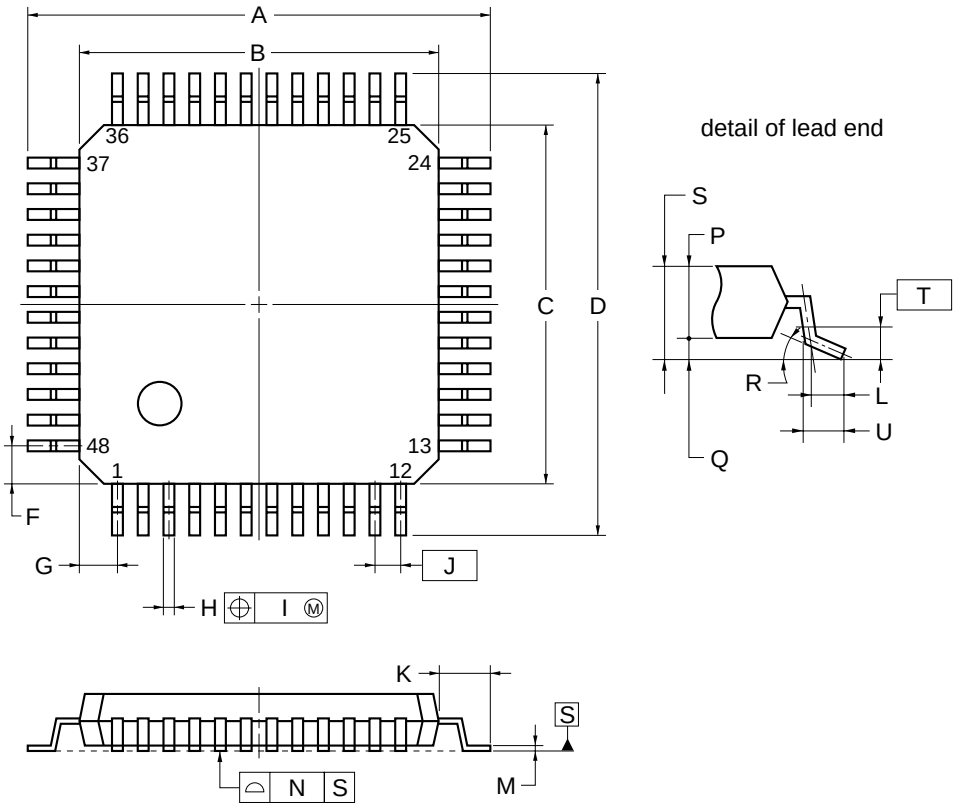
NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

48-PIN PLASTIC TQFP (FINE PITCH) (7x7)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.0±0.2
B	7.0±0.2
C	7.0±0.2
D	9.0±0.2
F	0.75
G	0.75
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.

P48GA-50-9EU

10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9177 and μPD789177Y should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E**).

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 10-1. Surface Mounting Type Soldering Conditions (1/2)

μPD78F9177GB-8ES: 44-pin plastic LQFP (10 × 10)
μPD78F9177YGB-8ES: 44-pin plastic LQFP (10 × 10)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (at 210 °C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (at 200 °C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

★ **Table 10-1. Surface Mounting Type Soldering Conditions (2/2)**

μPD78F9177YGA-9EU: 48-pin plastic TQFP (7 × 7)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (at 210 °C or higher), Count: Twice or less, Number of days:3[Note](After that, prebaking sis necessary at 125 °C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (at 200 °C or higher), Count: Twice or less, Number of days:3[Note](After that, prebaking sis necessary at 125 °C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds max. (per pin row)	–

Note The number of days for storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DIFFERENCES BETWEEN μPD78F9177, 78F9177Y, AND MASK ROM VERSIONS

The μPD78F9177 and μPD78F9177Y are flash memory version of the Mask ROM version. The differences between the μPD78F9177, 78F9177Y and the Mask ROM versions are shown in Table A-1.

Table A-1. Differences between μPD78F9177, 78F9177Y and Mask ROM Versions

Item \ Product Name		Flash Memory Version	Mask ROM Version	
		μPD78F9177, 78F9177Y	μPD789166, 789166Y 789176, 789176Y	μPD789167, 789167Y 789177, 789177Y
Internal memory	ROM	24 KB	16 KB	24 KB
	High-speed RAM	512 bytes		
V_{PP} pin		Provided	Not provided	
Pull-up resistor		17 (Software control)	21 (Software control: 17, mask option specification: 4)	
A/D resolution		10 bits	8 bits (μPD789166, 789167, 789166Y, 789167Y) 10 bits (μPD789176, 789177, 789176Y, 789177Y)	
Electrical specifications		See the relevant data sheet		

Cautions 1. There are differences in the amount of noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM versions, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering sample, ES) of the mask ROM version.

2. When the μPD78F9177, a flash memory counterpart of the μPD789166 or μPD789167, is used, however, ADCR0 can be manipulated with an 8-bit memory manipulation instruction. In this case, use an object file assembled with the μPD789166 or μPD789167. The same is also true for the μPD78F9177Y, a flash memory counterpart of the μPD789166Y or μPD789167Y. When the μPD78F9177Y is used, ADCR0 can be manipulated with an 8-bit memory manipulation instruction. In this case, use an object file assembled with the μPD789166Y or μPD789167Y.

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD78F9177 and μPD78F9177Y.

Language Processing Software

RA78K0S Notes 1, 2, 3	Assembler package common to 78K/0S Series
CC78K0S Notes 1, 2, 3	C compiler package common to 78K/0S Series
DF789177 Notes 1, 2, 3	Device file for μPD789167, 789177, 789167Y, and 789177Y Subseries
CC78K0S-L Notes 1, 2, 3	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part No. FL-PR3 Note 4, PG-FP3)	Flash programmer dedicated for on-chip flash memory microcontrollers
FA-44GB-8ES Note 4	Flash memory programming adapter for 44-pin plastic LQFP (GB-8ES type)
★ FA-48GA	Flash memory programming adapter for 48-pin plastic TQFP (fine pitch) (GA-9EU type)

Debugging Tools(1/2)

IE-78K0S-NS In-circuit emulator		In-circuit emulator used to debug hardware or software when application systems which use the 78K/0S Series are developed. The IE-78K0S-NS supports an integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-70000-MC-PS-B AC adapter		Adapter used to supply power from a 100- to 240-V AC outlet
IE-70000-98-IF-C Interface adapter		Adapter required when using the PC-9800 series (excluding notebook PCs) as the host machine for the IE-78K0S-NS (C bus supported)
IE-70000-CD-IF-A PC card/interface		PC card and interface cable required when using a notebook PC as the host machine for the IE-78K0S-NS (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter		Adapter required when using an IBM PC/AT™ or compatible as the host machine for the IE-78K0S-NS (ISA bus supported)
IE-70000-PCI-IF Interface adapter		Adapter required when using a PC equipped with a PCI bus as the host machine for the IE-78K0S-NS
IE-789177-NS-EM1 Emulation board		Emulation board used to emulate the peripheral hardware specific to the device. This is used in combination with the in-circuit emulator.
NP-44GB Note 4 Emulation probe		Board to connect an in-circuit emulator to the target system. This is used in combination with the EV-9200G-44
	EV-9200G-44 conversion socket	Conversion socket to connect the target system board on which a 44-pin plastic LQFP can be mounted and the NP-44GB
NP-44GB-TQ Note 4 Emulation probe		Board to connect an in-circuit emulator to the target system. This is used in combination with the TGB-044SAP.
	TGB-044SAP Note 5 conversion socket	Conversion socket to connect the target system board on which a 44-pin plastic LQFP can be mounted and the NP-44GB-TQ

Debugging Tools(2/2)

NP-48GA[Note 4] Emulation probe		Board to connect an in-circuit emulator to the target system. This is used in combination with the TGA-048SDP.
	TGA-048SDP[Note 5] conversion socket	Conversion socket to connect the target system board on which a 48-pin plastic TQFP (fine pitch) can be mounted and the NP-48GA
SM78K0S[Notes 1, 2]		System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]		Integrated debugger common to 78K/0S Series
DF789177[Notes 1, 2]		Device file for μPD789167, 789177, 789167, and 789177Y Subseries

Real-Time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. Based on the PC-9800 series (Japanese Windows™)

2. Based on IBM PC/AT and compatibles (Japanese Windows/English Windows)

3. Based on the HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Soraris™), and NEWS™ (NEWS-OS™)

4. Product made by and available from Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813).

5. Product made by TOKYO ELETECH CORPORATION.
Refer to: Daimaru Kogyo, Ltd.
Tokyo Electronic Division (+81-3-3820-7112)
Osaka Electronic Division (+81-6-6244-6672)

Remark The RA78K0S, CC78K0S, and SM78K0S can be used in combination with the DF789177.

APPENDIX C. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD789166, 167, 176, 177, 166Y, 167Y, 176Y, 177Y, 166(A), 167(A), 176(A), 177(A), 166Y(A), 167Y(A), 176Y(A), 177Y(A) Data Sheet	U14017J	U14017E
μPD78F9177, 78F9177Y Data Sheet	U14022J	This manual
μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual	U14186J	U14186E
78K/0S Series Instruction User's Manual	U11047J	U11047E

Document Related to Development Tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K0S Assembler Package	Operation	U11622J	U11622E
	Assembly Language	U11599J	U11599E
	Structured Assembly Language	U11623J	U11623E
CC78K0S C Compiler	Operation	U11816J	U11816E
	Language	U11817J	U11817E
SM78K0S System Simulator Windows based	Reference	U11489J	U11489E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092J	U10092E
ID78K0S-NS Windows based	Reference	U12901J	U12901E
IE-78K0S-NS In-circuit Emulator		U13549J	U13549E
IE-789177-NS-EM1 Emulation Board		U14621J	U14621E

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		Japanese	English
OS for 78K/0S Series MX78K0S	Fundamental	U12938J	U12938E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Documents

Document Name	Document No.	
	Japanese	English
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcomputer-Related Products by Third Party	U11416J	–

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The related document indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
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- Network requirements

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