

2-PHASE DD MOTOR DRIVER

The KA8310 is a monolithic integrated circuit for 2-phase full wave linear DD motor driving. This IC contains hall AMP, control circuit, CW/CCW circuit, thermal shutdown circuit and motor drivers.

FUNCTION

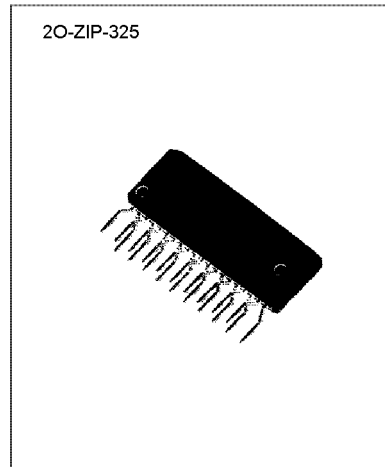
- TSD
- CTL/AMP
- CW/CCW
- HALL AMP
- Driver & AMP

FEATURES

- Incorporates rotation direction switching function.
- With regulated power supply for hall device feeding.
- High output current-control current ratio.
- High power dissipation.
- Built-in TSD (Thermal Shut Down) circuit.

APPLICATION

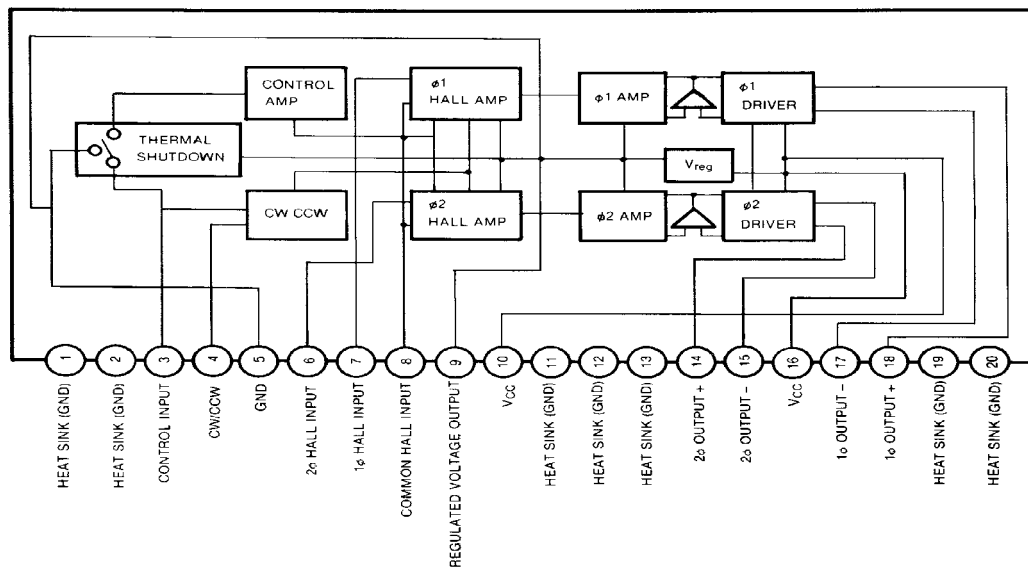
- VCRs, video disk players
- Compact disk players
- Tape recorders



ORDERING INFORMATION

Device	Package	Operating Temperature
KA8310	20-ZIP-325	-20°C ~ +75°C

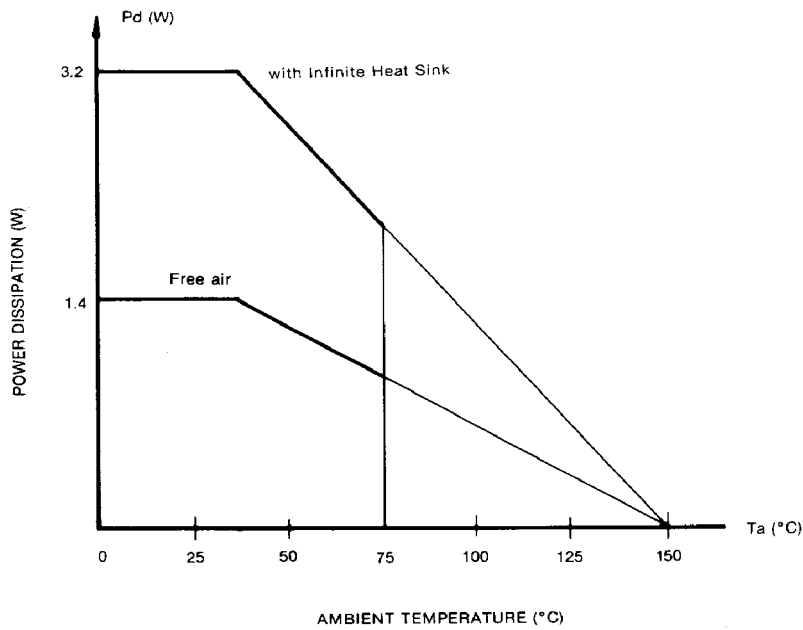
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit	Remark
Supply Voltage	V_{CC}	20	V	
Maximum Output Current (1)	I_{O1}	2.4	A	No Signal
Maximum Output Current (2)	I_{O2}	1.6		
Hall Input Voltage	V_H	6	V	DC
Pin 3 Current	I_3	1	mA	
Pin 4 Voltage	V_4	VREG	V	
Output Current	I_{REG}	40	mA	
Pin 16 Voltage	V_{16}	VCC	V	$V_{CC} \geq V_{16}$
AMP Common Input Voltage	V_{COM}	VREG-1.0	V	
Hall Device Frequency	f_{HALL}	1	KHz	
Operating Voltage Range	V_{OPR}	7.2~20	V	
Junction Temperature	T_J	150	°C	
Operating Temperature	T_{OPR}	-20~+75	°C	
Storage Temperature	T_{STG}	-40~+150	°C	

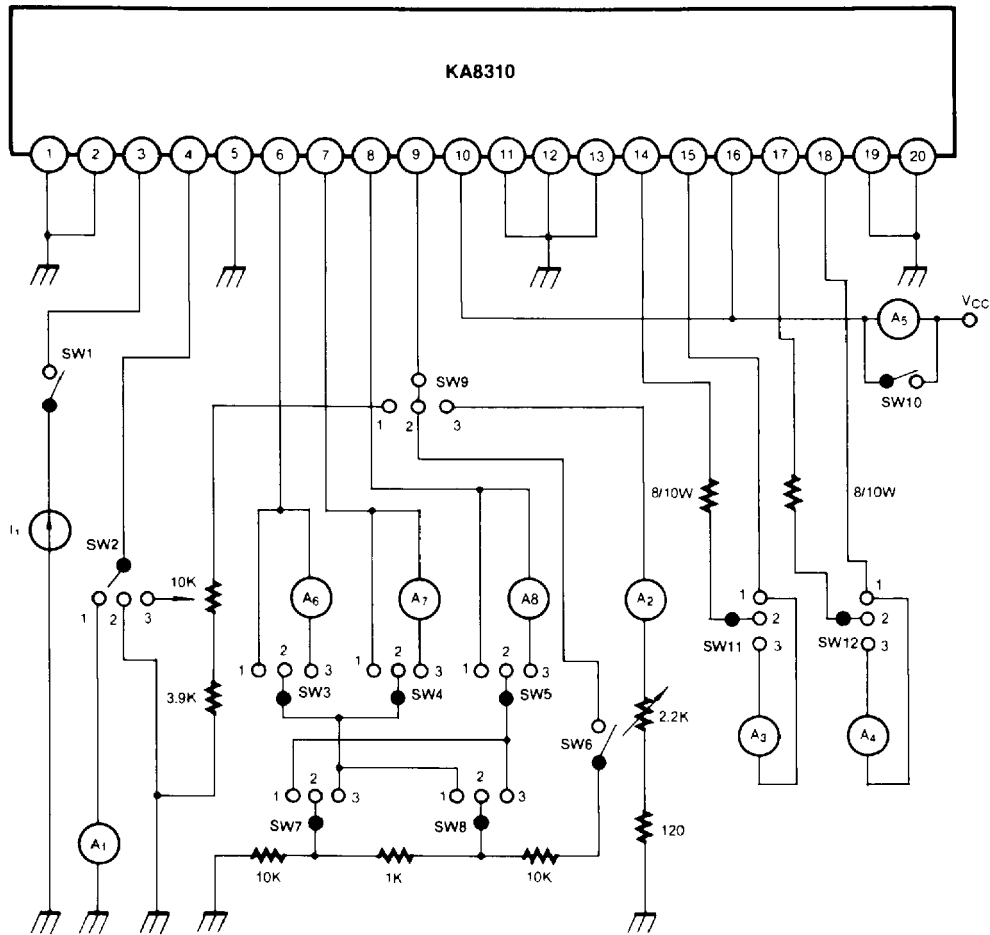
POWER DISSIPATION CURVE



ELECTRICAL CHARACTERISTICS ($V_{CC} = 12V$, $T_A = 25^\circ C$)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent Current	I_Q	$I_1 = Q \mu A$	4.5	6.5	8.5	mA
Regulated Voltage (1)	V_{REG1}	$I_1 = 0 \mu A$	6.0	6.7	7.4	V
Regulated Voltage (2)	V_{REG2}	$I_1 = Q \mu A$ $A_2 = 10mA$	6.0	6.7	7.4	V
Regulated Voltage (3)	V_{REG3}	$I_1 = Q \mu A$ $A_2 = 30mA$	6.0	6.7	7.4	V
Control Input Voltage	V_{CT1}	$I_1 = 10 \mu A$	1.2	1.35	1.5	V
CW/CCW Output Current	I_4	$I_1 = 0 \mu A$	200	410	600	μA
CW/CCW Threshold Voltage (1)	V_{T1}	$V_6 = V_7 = 3.1V$ $V_8 = 3.4V$ $I_1 = 50 \mu A$	2.5	—	—	V
CW/CCW Threshold Voltage (1)	V_{T2}	$V_6 = V_7 = 3.1V$ $V_8 = 3.4V$ $I_1 = 50 \mu A$	2.5	—	—	V
Current Gain (1)	G_1	$V_6 = 3.1V$ $V_8 = 3.4V$ $I_1 = 100 \mu A$ $G_1 = I_{OUT2} / I_1$	4000	4700	5500	.
Current Gain (2)	G_2	$V_6 = 3.4V$ $V_8 = 3.1V$ $I_1 = 100 \mu A$ $G_2 = I_{OUT2} / I_1$	4000	4700	5500	.
$\phi 1$, $\phi 2$ Current Ratio	R	$R = G_1 / G_2$	0.8	1	1.2	
Output Current (1)	I_{OUT1}	$V_6 = 3.4V$ $V_8 = 3.1V$ $I_1 = 180 \mu A$	750	890	1150	mA
Output Current (2)	I_{OUT2}	$V_7 = 3.4V$ $V_8 = 3.1V$ $I_1 = 180 \mu A$	750	890	1150	mA

TEST CIRCUIT

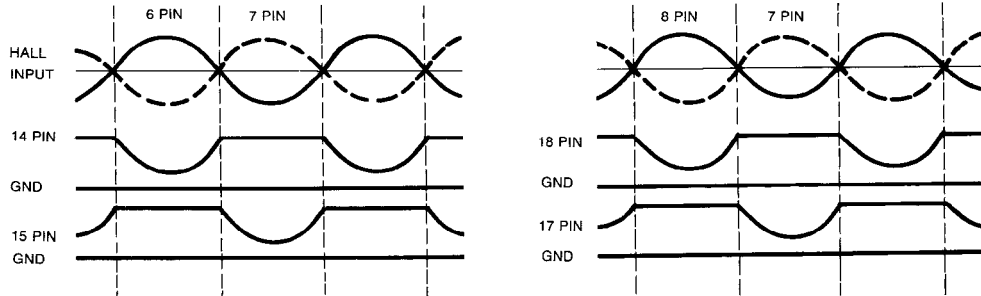


TEST METHOD ($V_{CC}=12V$)

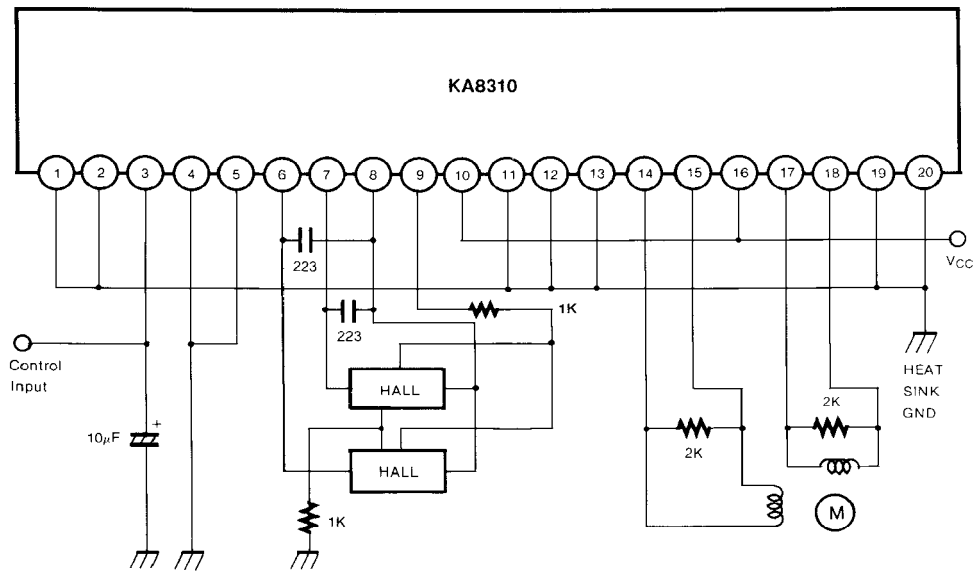
TEST Characteristic	Condition	Switch Condition												Test Point
		SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12	
Quiescent Current	$I_1=Q\mu A$	1	2	2	2	2	2	2	2	2	2	2	2	A5
Regulated Voltage (1)	$I_1=0\mu A$	1	2	2	2	2	2	2	2	2	1	2	2	Pin9
Regulated Voltage (2)	$I_1=Q\mu A$ $A_2=10mA$	1	2	2	2	2	2	2	2	3	1	2	2	Pin9
Regulated Voltage (3)	$I_1=Q\mu A$ $A_2=30mA$	1	2	2	2	2	2	2	2	3	1	2	2	Pin9
Control Input Voltage	$I_1=10\mu A$	1	2	2	2	2	2	2	2	2	1	2	2	Pin3
CW/CCW Output Current	$I_1=0\mu A$	1	1	2	2	2	2	2	2	2	1	2	2	A1
CW/CCW Threshold Voltage (1)	$V_6=V_7=3.1V$ $V_8=3.4V$ $I_1=50\mu V$	1	3	1	1	1	1	3	3	1	1	3	2	Pin4 (A3)
CW/CCW Threshold Voltage (2)	$V_6=V_7=3.1V$ $V_8=3.4V$ $I_1=50\mu A$	1	3	1	1	1	1	3	3	1	1	2	3	Pin4 (A4)
Current Gain (1)	$V_6=3.1V$ $V_8=3.4V$ $I_1=100\mu A$	1	2	1	2	1	1	3	3	2	1	3	2	A3/I1
Current Gain (2)	$V_6=3.4V$ $V_8=3.1V$ $I_1=100\mu A$	1	2	2	1	1	1	3	3	2	1	2	3	A4/I1
$\phi 1, \phi 2$ Current Ratio														
Output Current (1)	$V_6=3.4V$ $V_8=3.1V$ $I_1=180\mu A$	1	2	1	2	1	1	1	1	2	1	3	2	A3
Output Current (2)	$V_7=3.4V$ $V_8=3.1V$ $I_1=180\mu A$	1	2	2	1	1	1	1	1	2	1	2	3	A4

APPLICATION INFORMATION

OUTPUT WAVE FORM (4 PIN GND)



APPLICATION CIRCUIT



*The Application of HALL BIAS Pins must to follow above circuits.

Dimensions in Millimeters

