No.1190 A

LC7132

C MOS LSI

PLL FREQUENCY SYNTHSIZER LSI FOR 27MHz CB TRANSCEIVERS

Use

PLL frequency synthesizer LSI for 27MHz CB transceivers (U.S. standard).

Functions, features

1. Built-in high speed programmable divider for direct PLL system.
2. Doubled-frequency of VCO applicable as transmitting frequency carrier.
3. PLL out-of-lock output available to inhibit transmittion.
4. Instantaneous call capability of channel 9.
5. Built-in detecting circuit of mis-program.
6. Built-in amplifier for crystal oscillator.
7. Built-in amplifier for active low-pass filter.
8. 7-segment code channel selection. (allowable voltage 15V)

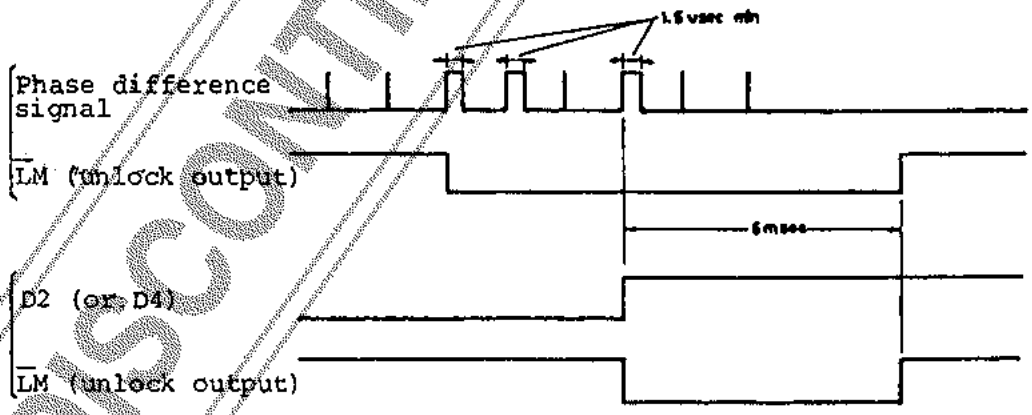
Description of functions

Digital Out-of-Lock Output

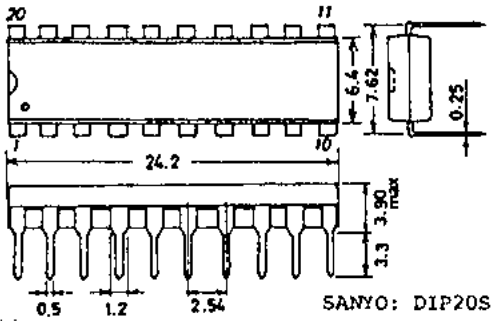
In direct PLL system, phase difference signal's pulse width at channel change is too narrow, so it is difficult to get out-of-lock signal from phase detector in the way of using C,R components externally.

LC7132 makes it possible to output the out-of-lock signal to have digital discriminate-expander of the pulse from phase detector internally (Detects the phase difference signal over 1.6us pulse width, and makes it expand to 6ms output pulse).

And also LC7132 outputs the out-of-lock signal when the phase difference signal is within 1.6us to have the detector of channel change input.



Case Outline
3021B-D20S1C
(unit:mm)



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Instantaneous call of channel 9 and recourse against miscode.

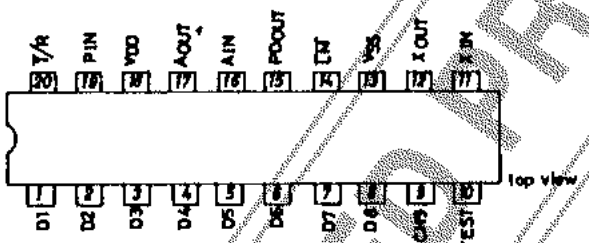
- .Setting CH9 at "H" level causes channel 9 to be selected.
- .Inputting miscode to D1 to D8 causes channel 19 to occur.
- .The following table shows the transmitting/receiving channel corresponding to the combination of D1 to D8 and CH9.

Input		Output
Data of D1 to D8	CH9	Channel
Normal code	0	Channel depending on D1 to D8
	1	Channel 9
Error program	0	Channel 19
	1	Chanel 9

1 : "H" level
0 : "L" level

Built-in amplifier for active low-pass filter
In direct PLL system, active low-pass filter is more available, as lock-up-time of PLL using active low-pass filter is shorter than the one using passive low-pass filter. The LC7132 contains an N channel open drain amplifier for active filter in order to make lockup time shorter.

Pin Assignment



Absolute Maximum Ratings at T_a=25°C

				unit
Maximum Supply Voltage	V_{DD}max		-0.3 to +9.0	V
Maximum Input Voltage	V_{IN}max(1)	D1 to D8,CH9	-0.3 to +17	V
	V_{IN}max(2)	Input pins other than above.	-0.3 to V_{DD}+0.3	V
Maximum Output Voltage	V_{OUT}(1)	LM, AOUT, output off	-0.3 to +10.0	
	V_{OUT}(2)	PDOUT, AOUT, output off	-0.3toV_{DD}+0.3	V
Maximum Output Current	I_{OUT}(1)	LM	0 to 15	mA
	I_{OUT}(2)	AOUT	0 to 2.5	mA
Allowable Power Dissipation	Pdmax	T_a=70°C	300	mW
Operating Temperature	Topg		-30 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at T_a=25°C

			min	typ	max	unit
Supply Voltage	V_{DD}	Ta=-30 to +70°C	5.0		8.0	V
Output Voltage	V_{OUT}	LM,AOUT,output off	0		9.0	V
Input Amplitude	V_{IN}(1)	XIN,*,f_{IN}(1)=10.25MHz	1.0		0.9V_{DD}	Vp-p
	V_{IN}(2)	PIN,*,f_{IN}(2)=20MHz	1.0		0.9V_{DD}	Vp-p
Input Frequency	f_{IN}(1)	XIN,*,V_{IN}(1)=1.0Vp-p	1.0		10.25	MHz
	f_{IN}(2)	PIN,*,V_{IN}(2)=1.0Vp-p	1.0		20	MHz
Input "H" Level Voltage	V_{IH}(1)	D1 to D8,CH9	0.8V_{DD}		15	V
	V_{IH}(2)	$\overline{T}$/R	0.7V_{DD}		V_{DD}	V
Input "L" Level Voltage	V_{IL}(1)	D1 to D8,CH9	0		0.4V_{DD}	V
	V_{IL}(2)	$\overline{T}$/R	0		0.3V_{DD}	V

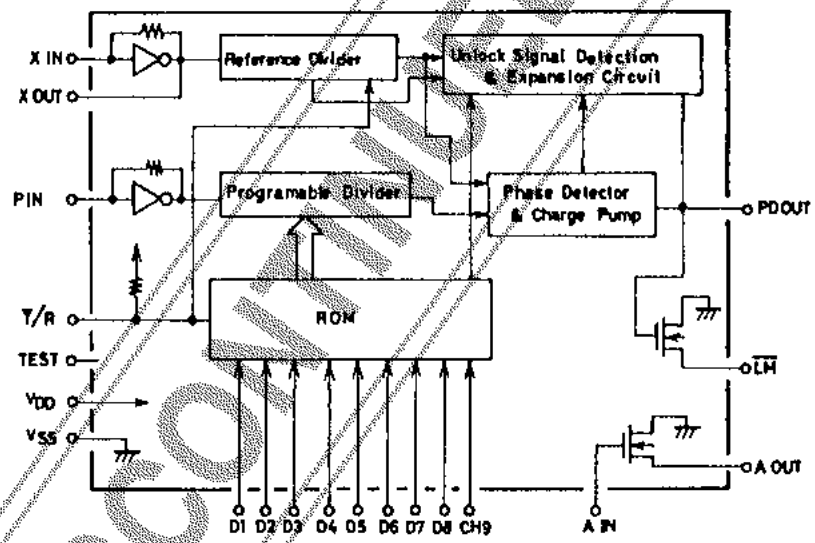
Note * : Sinusoidal wave, capacitive coupling, T_a=-30 to +70°C

Electrical Characteristics at T_a=25°C,V_{DD}=5 to 8V

				min	typ	max	unit
Input "H" Level Current	I_{IH}(1)	XIN,PIN	V_{IN}=V_{DD}			40	uA
Input "H" Level Current	I_{IH}(2)	D1 to D8,CH9	V_{IN}=15V			5.0	uA
Input "H" Level Current	I_{IH}(3)	AIN	V_{IN}=V_{DD}		0.01		nA
Input "L" Level Current	I_{IL}(1)	XIN,PIN	V_{IN}=V_{SS}			40	uA
	I_{IL}(2)	D1 to D8,CH9	V_{IN}=V_{SS}			5.0	uA

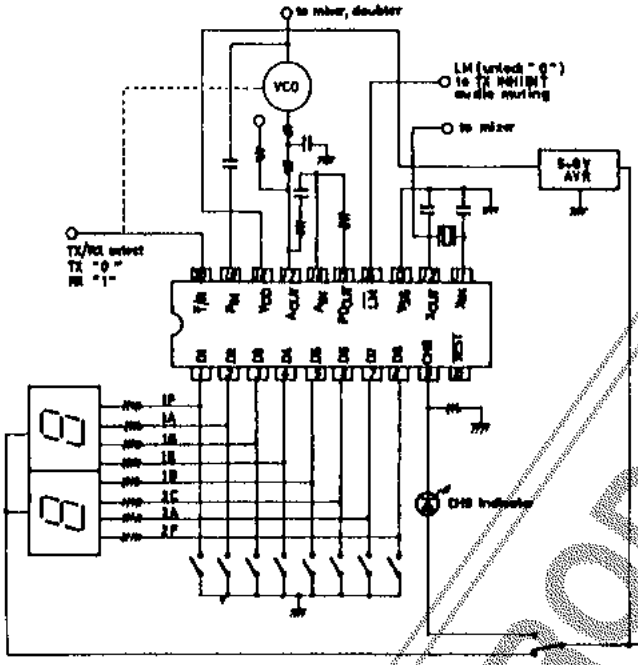
				min	typ	max	unit
Input "L" Level Current	$I_{IL}(3)$	$\overline{T}/R$	$V_{IN}=V_{SS}$	40	200	500	uA
	$I_{IL}(4)$	A_{IN}	$V_{IN}=V_{SS}$		0.01		nA
Output "H" Level Voltage	V_{OH}	PD_{OUT}	$I_{OUT}=0.3mA$	$V_{DD}-1.0$			V
Output "L" Level Voltage	$V_{OL}(1)$	PD_{OUT}	$I_{OUT}=0.3mA$			1.0	V
	$V_{OL}(2)$	A_{OUT}	$I_{OUT}=0.5mA$			0.3	V
	$V_{OL}(3)$	$\overline{LM}$	$I_{OUT}=15mA$			1.1	V
Feedback Resistance	$R_F(1)$	X_{IN}			1.0		Mohm
	$R_F(2)$	P_{IN}			0.5		Mohm
Input Threshold Voltage	V_{th}				$1/2V_{DD}$		V
"H"Level 3-State Leak Current	I_{OFFH}	PD_{OUT}	$V_{OUT}=V_{DD}$		0.01		nA
"L" Level 3-State Leak Current	I_{OFFL}	PD_{OUT}	$V_{OUT}=V_{SS}$		0.01		nA
Input Floating Voltage	$V_{IF}(1)$	$\overline{T}/R$	Input pins open	$V_{DD}-0.2$			V
Output Off Leak Current	$I_{OFF}(1)$	A_{OUT}	$V_{OUT}=9V$			3.0	uA
	$I_{OFF}(2)$	$\overline{LM}$	$V_{OUT}=9V$			5.0	uA
Current Dissipation	I_{DD}		$f_{IN}(1)=10.25MHz$, $f_{IN}(2)=20MHz$, $V_{IN}(1)=V_{IN}(2)=1.0Vp-p$ CH9=$A_{IN}=V_{SS}$, D1 to D4, D6 to D8=V_{DD}, D5=V_{SS}, Other pins open, Number of frequency divisions=3254		10	20	mA

Equivalent Circuit and Block Diagram



D1 to D8 : Program input (7-segment code)
X_{IN}, X_{OUT} : Amplifier for crystal oscillator
V_{DD}, V_{SS} : Power Supply
$\overline{LM}$: Lock monitor output Lock--open"1", unlock--"0"
PD_{OUT} : Charge pump output
A_{IN}, A_{OUT} : Amplifier for low-pass filter
P_{IN} : Programmable divider input
$\overline{T}/R$: Transmission/reception changeover input
$\overline{T}/R$="0"---Transmission $\overline{T}/R$="1"
$\overline{T}/R$="1"(or open)---reception
CH9 : Channel 9 select input
TEST : LSI test pin (TEST pin:Connected to V_{SS} or open)

Application Circuit



Program Data and Frequency Division

Channel No.	PROGRAM CODE								RX($\overline{T}$/R="1")		TX($\overline{T}$/R="0")	
	D1 (1F)	D2 (1A)	D3 (1G)	D4 (1E)	D5 (1B)	D6 (2C)	D7 (2A)	D8 (2F)	N	F_{VCO} (MHz)	N	F_{VCO} (MHz)
1	1	1	1	1	0	1	1	1	3254	16.27	5393	13.4825
2	1	0	0	0	0	1	1	1	3256	16.28	5395	13.4875
3	1	0	0	1	0	1	1	1	3258	16.29	5397	13.4925
4	0	1	0	1	0	1	1	1	3262	16.31	5401	13.5025
5	0	0	0	1	1	1	1	1	3264	16.32	5403	13.5075
6	0	0	0	0	1	1	1	1	3266	16.33	5405	13.5125
7	-	0	1	1	0	1	1	1	3268	16.34	5407	13.5175
8	0	0	0	0	0	1	1	1	3272	16.36	5411	13.5275
9	0	0	0	1	0	1	1	1	3274	16.37	5413	13.5325
10	0	0	1	0	0	0	1	1	3276	16.38	5415	13.5375
11	1	1	1	1	0	0	1	1	3278	16.39	5417	13.5425
12	1	0	0	0	0	0	1	1	3282	16.41	5421	13.5525
13	1	0	0	1	0	0	1	1	3284	16.42	5423	13.5575
14	0	1	0	1	0	0	1	1	3286	16.43	5425	13.5625
15	0	0	0	1	1	0	1	1	3288	16.44	5427	13.5675
16	0	0	0	0	1	0	1	1	3292	16.46	5431	13.5775
17	-	0	1	1	0	0	1	1	3294	16.47	5433	13.5825
18	0	0	0	0	0	0	1	1	3296	16.48	5435	13.5875
19	0	0	0	1	0	0	1	1	3298	16.49	5437	13.5925
20	0	0	1	0	0	1	0	1	3302	16.51	5441	13.6025
21	1	1	1	1	0	1	0	1	3304	16.52	5443	13.6075
22	1	0	0	0	0	1	0	1	3306	16.53	5445	13.6125
23	1	0	0	1	0	1	0	1	3312	16.56	5451	13.6275
24	0	1	0	1	0	1	0	1	3308	16.54	5447	13.6175
25	0	0	0	1	1	1	0	1	3310	16.55	5449	13.6225
26	0	0	0	0	1	1	0	1	3314	16.57	5453	13.6325
27	-	0	1	1	0	1	0	1	3316	16.58	5455	13.6375
28	0	0	0	0	0	1	0	1	3318	16.59	5457	13.6425
29	0	0	0	1	0	1	0	1	3320	16.60	5459	13.6475
30	0	0	1	0	0	0	0	1	3322	16.61	5461	13.6525
31	1	1	1	1	0	0	0	1	3324	16.62	5463	13.6575
32	1	0	0	0	0	0	0	1	3326	16.63	5465	13.6625
33	1	0	0	1	0	0	0	1	3328	16.64	5467	13.6675
34	0	1	0	1	0	0	0	1	3330	16.65	5469	13.6725
35	0	0	0	1	1	0	0	1	3332	16.66	5471	13.6775
36	0	0	0	0	1	0	0	1	3334	16.67	5473	13.6825
37	-	0	1	1	0	0	0	1	3336	16.68	5475	13.6875
38	0	0	0	0	0	0	0	1	3338	16.69	5477	13.6925
39	0	0	0	1	0	0	0	1	3340	16.70	5479	13.6975
40	0	0	1	0	0	0	1	0	3342	16.71	5481	13.7025

"1" : logical high level
"0" : logical low level
"-" : don't care