MAXIM

Direct-Conversion Tuner IC

General Description

The MAX2108 is a low-cost direct-conversion tuner IC designed for use in digital direct-broadcast satellite (DBS) television set-top box units and microwave links. Its direct-conversion architecture reduces system cost compared to devices with IF-based architectures.

The MAX2108 directly tunes L-band signals to baseband using a broadband I/Q downconverter. The operating frequency range spans from 950MHz to 2150MHz. The IC includes a low-noise amplifier (LNA) with gain control, two downconverter mixers with output buffers, a 90° quadrature generator, and a divide-by 32/33 prescaler.

Applications

DirecTV, PrimeStar, EchoStar DBS Tuners

DVB-Compliant DBS Tuners

Cellular Base Stations

Wireless Local Loop

Broadband Systems

LMDS

Microwave Links

Features

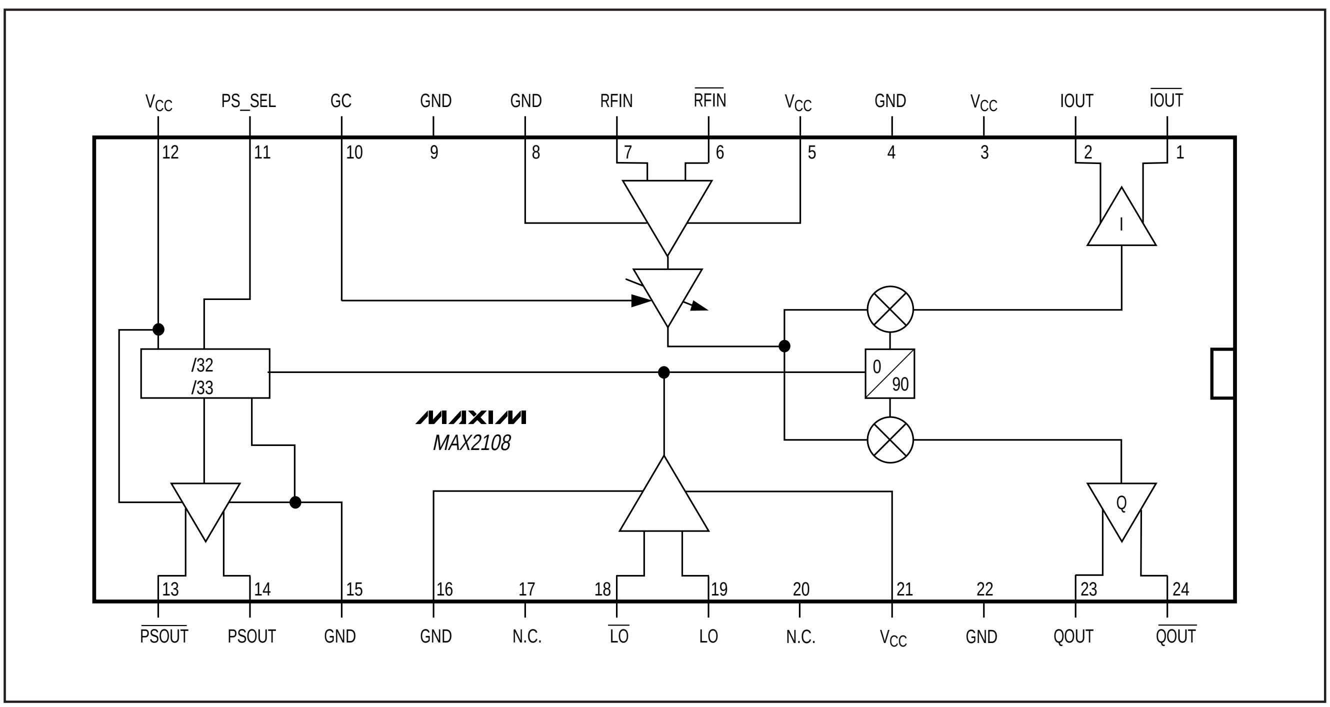
- ♦ **Low-Cost Architecture**
- ♦ **Operates from Single +5V Supply**
- ♦ **On-Chip Quadrature Generator, Dual-Modulus Prescaler (/32, /33)**
- ♦ **Input Levels: -20dBm to -70dBm per Carrier**
- ♦ **Over 50dB RF Gain-Control Range**
- ♦ **10dB Noise Figure at Maximum Gain**
- ♦ **+8dBm IIP3 at Minimum Gain**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2108CEG	0°C to +70°C	24 QSOP

Pin Configuration appears at end of data sheet.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +7V
V_{CC} to Any Other V_{CC} ....-0.3V to +0.3V
All Other Pins to GND................................-0.3V to (V_{CC} + 0.3V)
RFIN to $\overline{RFIN}$ ....±2V
LO to $\overline{LO}$ ....±2V
Short-Circuit Current
IOUT, $\overline{IOUT}$, QOUT, $\overline{QOUT}$ to GND 10mA
PSOUT, $\overline{PSOUT}$ to GND..40mA
Short-Circuit Duration IOUT to $\overline{IOUT}$, QOUT to $\overline{QOUT}$,
PSOUT to $\overline{PSOUT}$ 10sec
Continuous Power Dissipation (T_A = +70°C)
24 QSOP (derate 10mW/°C above T_A = +70°C) 800mW
Operating Temperature Range..............................0°C to +70°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V; V_{GC} = 1.3V; PS_SEL = 0.5V; IOUT, $\overline{IOUT}$, QOUT, $\overline{QOUT}$ = terminated with 2.5kΩ to GND; no input signal applied; T_A = 0°C to +70°C; unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			105	152	mA
PS_SEL Logic-High Threshold	V_{THH}		2.4			V
PS_SEL Logic-Low Threshold	V_{THL}				0.5	V
PS_SEL Input Bias Current	I_{PS_SEL}	0 < V_{PS_SEL} < V_{CC}	-30		+10	µA
GC Input Bias Current	I_{GC}	1V < V_{GC} < 4V	-80		+80	µA
IOUT, $\overline{IOUT}$, QOUT, $\overline{QOUT}$ Common-Mode Output Voltage	V_{CM}		2.9	3.35	3.8	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V; PS_SEL = 0.5V; P_{RFIN} = -20dBm; f_{LO} = f_{RFIN} +125kHz; GC set via servo loop for V_{IOUT} - $V_{\overline{IOUT}}$ = 200mVp-p (differential); T_A = +25°C; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RFIN Frequency Range (Note 1)	f_{RFIN}		950		2150	MHz
RFIN Maximum Input Power (Note 2)	$P_{RFINMAX}$	950MHz < f_{RFIN} < 2150MHz, P_{LO} = -5dBm	-20			dBm
RFIN Minimum Input Power (Note 2)	$P_{RFINMIN}$	950MHz < f_{RFIN} < 2150MHz, P_{LO} = -5dBm, V_{IOUT} - $V_{\overline{IOUT}}$ = 10mVp-p, T_A = 0°C +70°C			-70	dBm
External LO Drive Level (Note 2)				-5		dBm
Gain-Control Range (Note 2)		1V < V_{GC} < 4V, P_{LO} = -5dBm	50			dB
RFIN Input Third-Order Intercept Point (Note 3)	IIP_3			8		dBm
RFIN Input Second-Order Intercept Point (Note 4)	IIP_2			14		dBm
Noise Figure	NF	V_{GC} = 4V, f_{LO} = 1750MHz		10		dB

AC ELECTRICAL CHARACTERISTICS (continued)

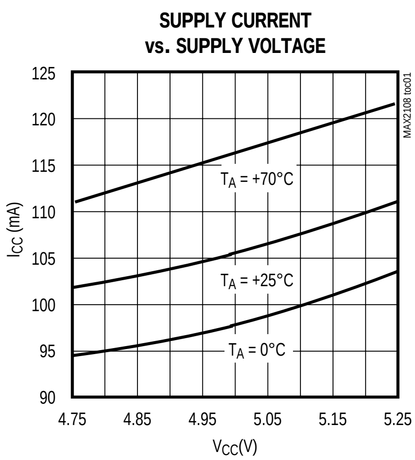
(V_{CC} = +5V; PS_SEL = 0.5V; P_{RFIN} = -20dBm; f_{LO} = f_{RFIN} +125kHz; GC set via servo loop for V_{IOUT} - $V_{\overline{IOUT}}$ = 200mVp-p (differential); T_A = +25°C; unless otherwise noted.)

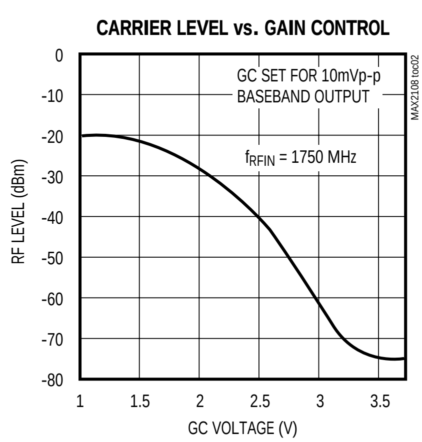
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prescaler Divide Ratio		V_{PS_SEL} > 2.4V	32		32	
		V_{PS_SEL} < 0.5V	33		33	
Differential Prescaler Output Swing	V_{PSOUT} - $V_{\overline{PSOUT}}$	C_{PSOUT} = $C_{\overline{PSOUT}}$ = 10pF to GND	1.0			Vp-p
I/Q Channel Quadrature Phase Error (Note 2)		f_{IOUT} = $f_{\overline{IOUT}}$ = f_{QOUT} = $f_{\overline{QOUT}}$ = 125kHz			3	degrees
I/Q Amplitude Mismatch (Note 2)		f_{IOUT} = $f_{\overline{IOUT}}$ = f_{QOUT} = $f_{\overline{QOUT}}$ = 125kHz			1	dB
I/Q Channel Clipping Level		f_{IOUT} = $f_{\overline{IOUT}}$ = f_{QOUT} = $f_{\overline{QOUT}}$ = 10MHz, no output load		1.4		Vp-p
Baseband Bandwidth		At -3dB attenuation		150		MHz
I/Q Channel Differential Output Impedance		f_{IOUT} = $f_{\overline{IOUT}}$ = f_{QOUT} = $f_{\overline{QOUT}}$ = 20MHz		33		Ω

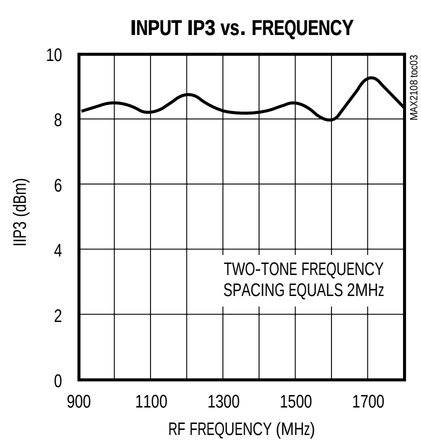
Note 1: AC specifications with minimum/maximum limits are met within this frequency range.
Note 2: LO and $\overline{LO}$ are differentially driven through an AC-coupled matching network.
Note 3: P_{RFIN} = -20dBm per tone, GC set via servo loop for V_{IOUT} - $V_{\overline{IOUT}}$ = 20mVp-p per tone. $f1_{RFIN}$ = 1749MHz, $f2_{RFIN}$ = 1751MHz, f_{LO} = 1740MHz.
Note 4: P_{RFIN} = -20dBm per tone, GC set via servo loop for V_{IOUT} - $V_{\overline{IOUT}}$ = 20mVp-p per tone. $f1_{RFIN}$ = 1200MHz, $f2_{RFIN}$ = 2150MHz, f_{LO} = 951MHz.

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)



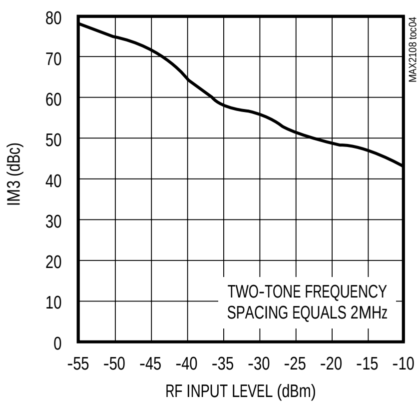




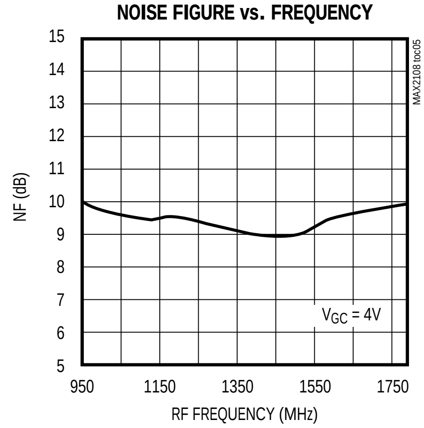
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

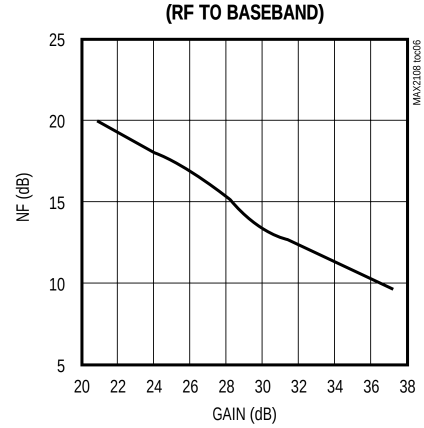
IM3 vs. CARRIER LEVEL



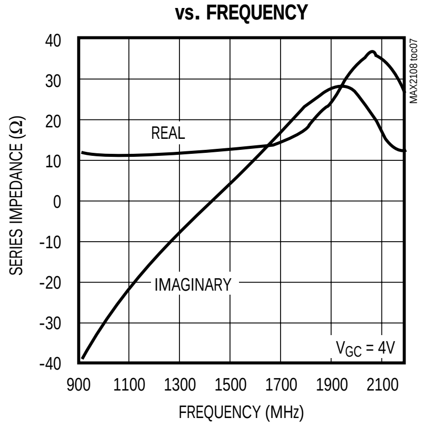
NOISE FIGURE vs. FREQUENCY



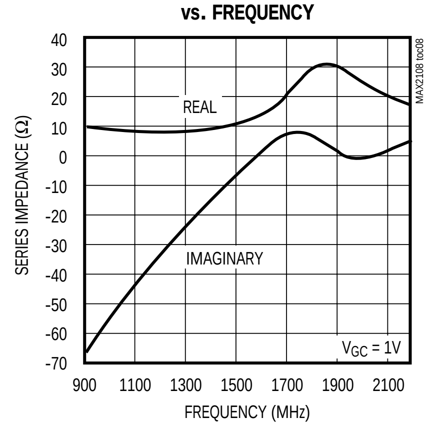
NOISE FIGURE vs. INSERTION GAIN (RF TO BASEBAND)



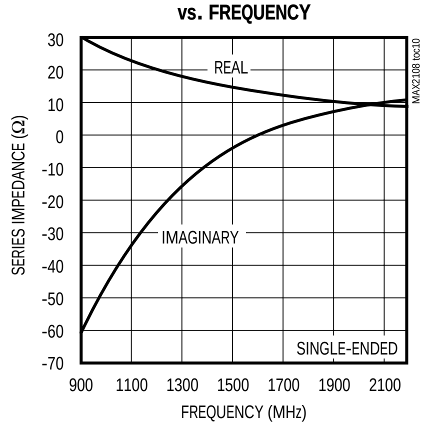
RF PORT SERIES IMPEDANCE vs. FREQUENCY



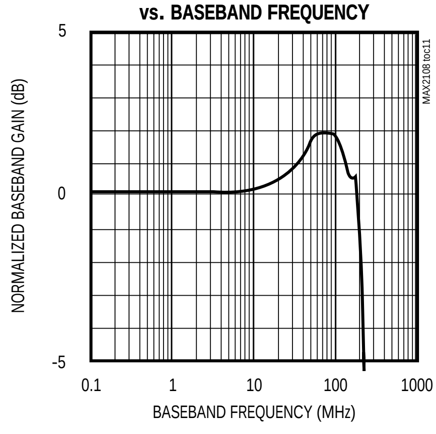
RF PORT SERIES IMPEDANCE vs. FREQUENCY



LO PORT SERIES IMPEDANCE vs. FREQUENCY



NORMALIZED BASEBAND GAIN vs. BASEBAND FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	$\overline{IOUT}$	Inverting I-Channel Baseband Output
2	IOUT	Noninverting I-Channel Baseband Output
3	V_{CC}	Downconverter +5V Supply. Bypass with a 10pF capacitor to GND as close to the IC as possible. Connect an additional 0.1µF capacitor in parallel with the 10pF capacitor.
4	GND	Ground. Connect to a low-inductance ground plane.
5	V_{CC}	RF +5V Supply. Bypass with a 22pF capacitor to GND as close to the IC as possible.
6	$\overline{RFIN}$	Inverting RF Input. Connect to a 22pF capacitor in series with a 75Ω resistor to GND.
7	RFIN	Noninverting RF Input. Connect via matching network to a 75Ω cable.
8, 9	GND	RF Ground. Connect to a low-inductance ground plane.
10	GC	Gain-Control Input. Apply a voltage between 1V and 4V to control the gain of the RF amplifier. Bypass with a 1000pF capacitor to minimize noise on the control line.
11	PS_SEL	Prescaler Modulus Control. Drive PS_SEL <0.5V to operate in divide-by-33 mode. Drive PS_SEL >2.4V to operate in divide-by-32 mode.
12	V_{CC}	Prescaler +5V Supply. Bypass with a 1000pF capacitor to GND.
13	$\overline{PSOUT}$	Inverting Prescaler Output
14	PSOUT	Noninverting Prescaler Output
15	GND	Prescaler Ground. Connect to a low-inductance ground plane.
16	GND	Local Oscillator Ground. Connect to a low-inductance ground plane.
17, 20	N.C.	No Connection. Do not make any connection to this pin.
18	$\overline{LO}$	Inverting LO Input
19	LO	Noninverting LO Input
21	V_{CC}	Local Oscillator +5V Supply. Bypass with a 22pF capacitor and a 0.1µF capacitor to pin 16.
22	GND	Downconverter Ground. Connect to a low-inductance ground plane.
23	QOUT	Noninverting Q-Channel Baseband Output
24	$\overline{QOUT}$	Inverting Q-Channel Baseband Output

Detailed Description

The MAX2108 downconverts signals in the 950MHz to 2150MHz range directly to baseband in-phase/quadrature-phase (I/Q) signals. It is designed for digital DBS tuner applications where a direct downconversion provides a cost savings over multiple-conversion approaches. However, the MAX2108 is applicable to any system requiring a broadband I/Q downconversion.

Internally, the MAX2108 consists of a broadband front-end variable gain stage, a quadrature downconverter, a 90° quadrature generator, a divide-by 32/33 prescaler, and high-linearity I and Q baseband buffers. The front-end gain-control range is over 50dB. Specifically, when the MAX2108 operates in an automatic gain control (AGC) loop, V_{GC} is adjusted by the loop so that a sine wave at RFIN ranging in power from -70dBm to -20dBm produces a sine wave across IOUT, $\overline{IOUT}$ and QOUT, $\overline{QOUT}$ at 10mVp-p differential. The noise figure is at its minimum when GC is at its maximum gain setting.

The quadrature downconverter follows the front-end variable-gain amplifier. The mixer LO ports are fed with the two LO signals, which are 90° apart in phase. These quadrature LO signals are generated internally using the signal from the LO and $\overline{LO}$ pins.

The resulting I/Q baseband signals are fed through separate I-channel and Q-channel baseband buffers. The outputs are capable of driving lowpass filters with 100Ω characteristic impedance (that is, the equivalent of an AC-coupled 100Ω load). The baseband -3dB output bandwidth is approximately 150MHz.

Applications Information

Front-End Tuner Circuitry for DBS Tuners

In a typical application, the signal path ahead of the tuner includes a discrete low-noise amplifier/buffer and a PIN-diode attenuator. Since the MAX2108 satisfies the noise and linearity requirements for DBS, this front-end circuitry is not required.

In some very high linearity applications, such as single channel-per-carrier (SCPC), a varactor-tuned preselection bandpass filter is added between a discrete LNA and the MAX2108. The filter provides a means of broadly filtering adjacent interference signals, thus improving the intermodulation performance of the tuner. Additionally, the filter removes RF interference at twice the LO frequency, which otherwise adds to the co-channel interference. The MAX2108 rejects this carrier to approximately 25dBc.

LO Port

The MAX2108 accepts either a single-ended or differential LO signal. For single-ended drive, AC-couple the LO signal into LO with a 47pF capacitor, and bypass $\overline{LO}$ to ground with a 47pF capacitor in series with a 25Ω resistor. Drive LO with a 50Ω source at -5dBm.

Prescaler

The prescaler requires a stable logic level at PS_SEL 4ns before the falling edge of PSOUT, $\overline{PSOUT}$ to assert the desired modulus. The logic level at PS_SEL must remain static until 2ns after this falling edge.

Baseband Buffers

The MAX2108 baseband buffers provide at least 10mVp-p differential swing across IOUT, $\overline{IOUT}$ and QOUT, $\overline{QOUT}$, and are capable of driving an AC-coupled 100Ω differential load. In a typical application, IOUT, $\overline{IOUT}$, QOUT, and $\overline{QOUT}$ drive a 5th- or 7th-order lowpass filter for ADC anti-aliasing purposes (see the *Filters in Direct-Conversion Tuners* section). In general, additional gain is required, after the filters. This is accomplished with a pair of video-speed op amps, such as the MAX4216 dual video op amp, or a simple transistor circuit. Contact Maxim for more information about the MAX4216.

Layout Considerations

Observe standard RF layout rules. A ground plane is essential; when connecting areas of ground plane between layers, use vias liberally. If a ground plane is used under the lowpass filters, note that the filter response may be slightly offset due to parasitic capacitance.

In a direct-conversion receiver, LO leakage to the RF input connector is a major issue, since filtering of the LO is impossible (the LO operates at the same frequency as the RF input). Observe the power-supply bypass capacitor connections in the *Pin Description* table, notably pins 3, 5, 12, and 21. Traces from these IC pins to the bypass capacitors must be kept on the top side of the board and as short as possible.

Power-Supply Sequencing

The MAX2108 has several +5V supply pins. Configure the supply layout in a star format, with a bypass capacitor that dominates the rise time of the supply at the center of the star to ensure that all pins see approximately the same voltage during power-up.

Filters in Direct-Conversion Tuners

Typically, a 5th- or 7th-order L-C lowpass filter is used for anti-aliasing the ADCs following the MAX2108. Table 1 offers suggested component values for these lowpass filters. Figures 1 and 2 describe typical filtering requirements.

Table 1. Suggested Component Values for Discrete Lowpass Filters

ADC SAMPLING RATE (Msps)	FILTER TYPE	R_S (Ω)	C1 (pF)	L1 (nH)	C2 (pF)	L2 (nH)	C3 (pF)	L3 (nH)	C4 (pF)	R_L (kΩ)
40	0.1dB Chebyshev, f_C = 20MHz	50	20	910	60	1500	75	1500	60	20
60	0.1dB Chebyshev, f_C = 30MHz	50	11	620	41	910	50	1000	41	20
90	0.1dB Chebyshev, f_C = 20MHz	50	15	680	39	820	33	Short	Open	20
	0.1dB Chebyshev, f_C = 45MHz	50	9	390	28	620	34	680	28	20

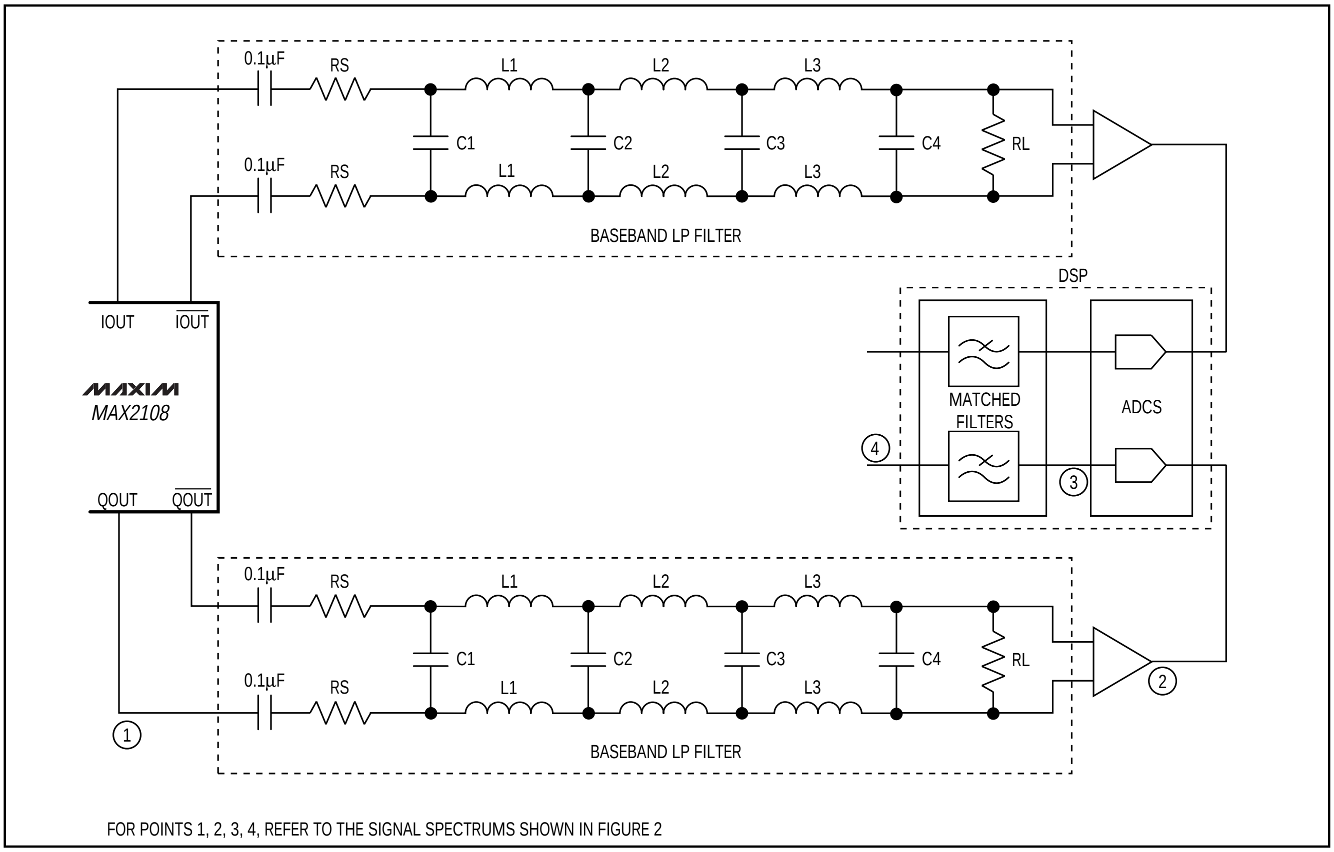


Figure 1. In-Phase and Quadrature-Phase Signal Paths

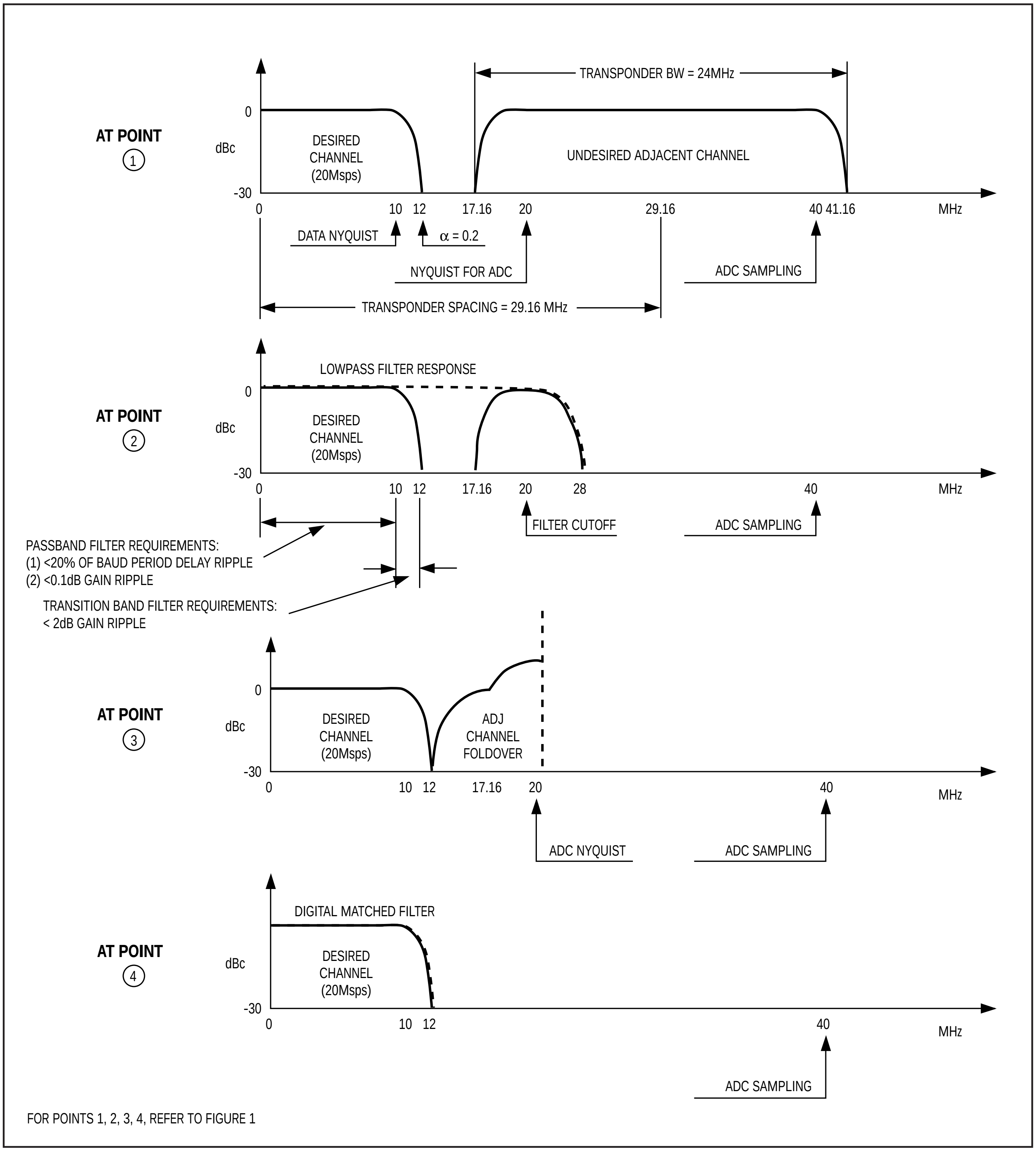
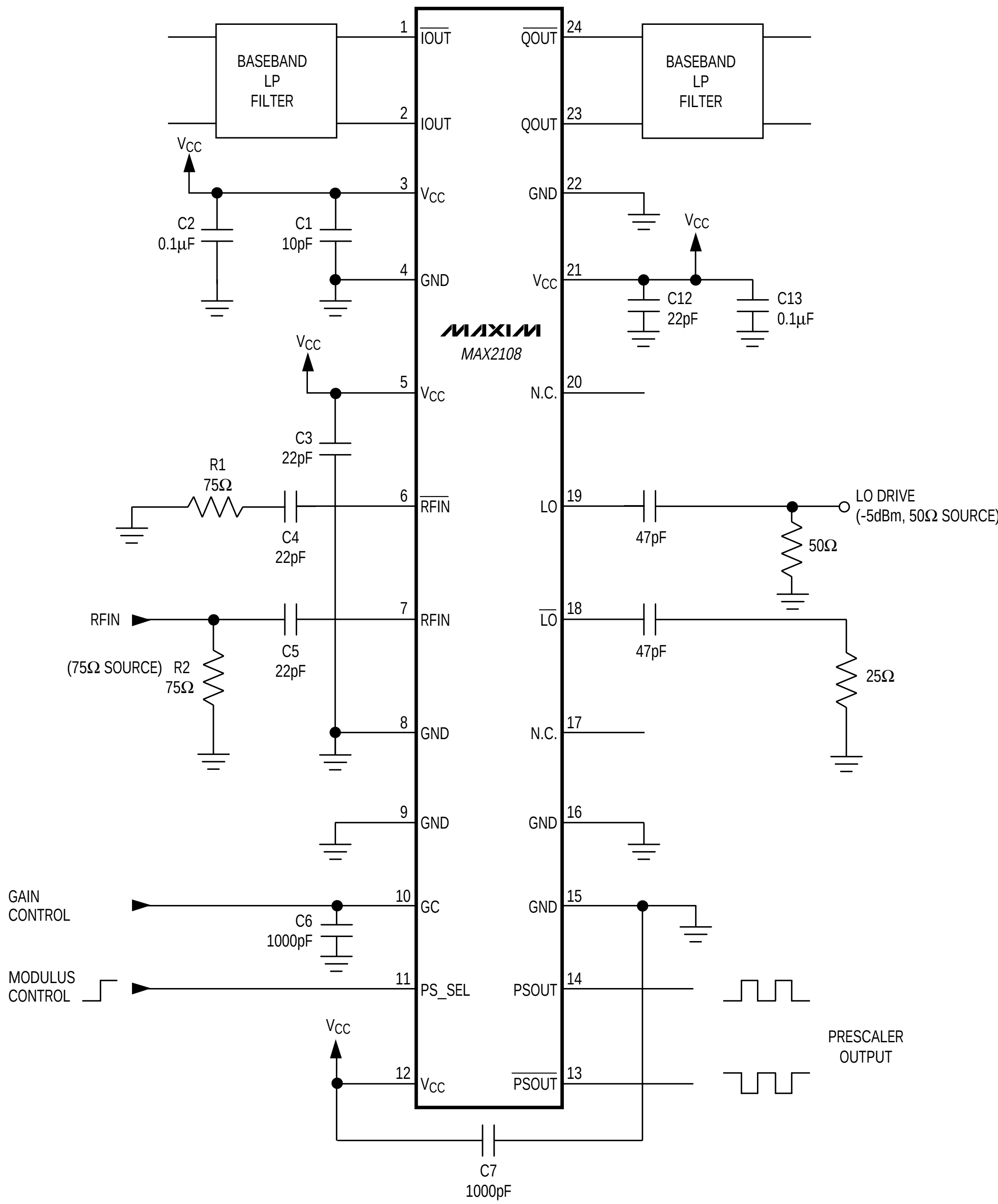
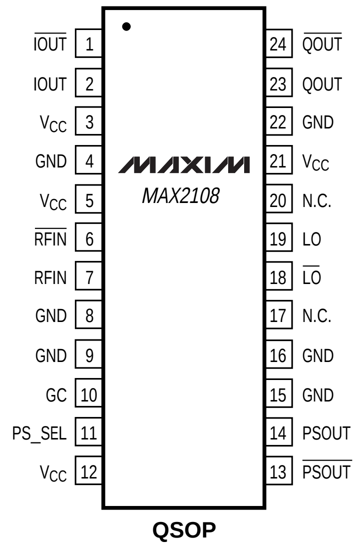


Figure 2. Lowpass Filtering Example

Typical Operating Circuit



Pin Configuration

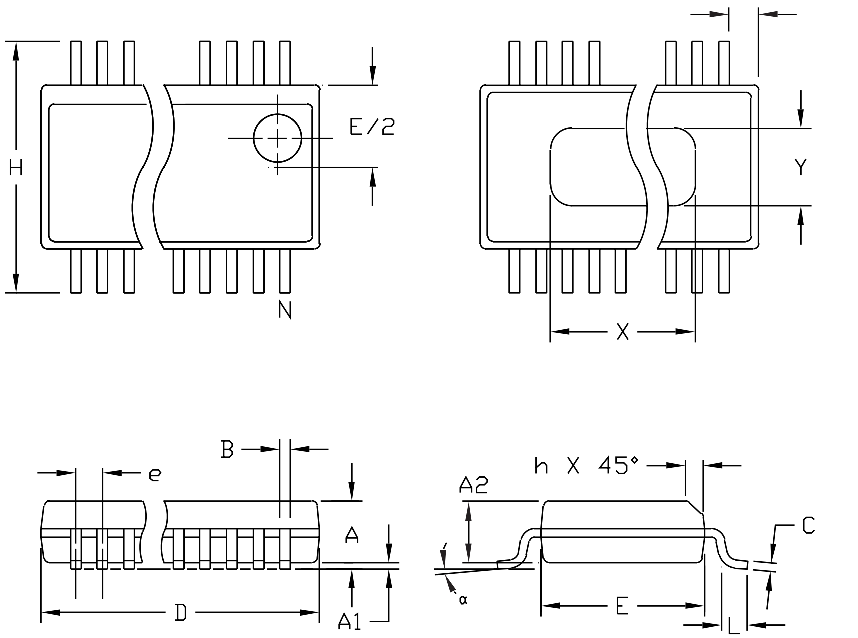


Chip Information

TRANSISTOR COUNT: 1484

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1