OVERVIEW

The SM5158A is a serial data programmable PLL Frequency Synthesizer LSI fabricated in NPC's proprietary Molybdenum-gate CMOS technology.

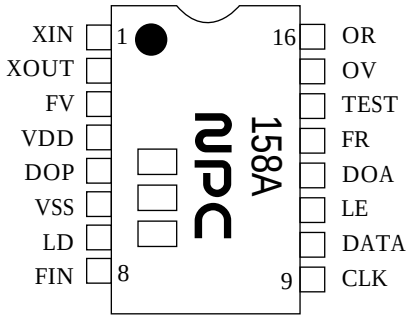
Ratios of reference frequency divider and input frequency divider can be independently set.

FEATURES

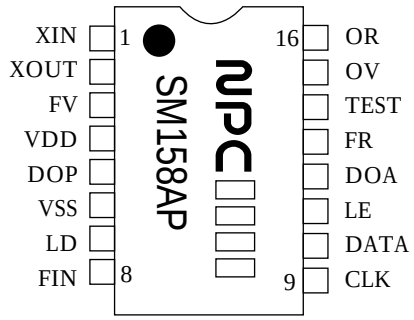
- Up to 200MHz input frequency (VDD=4.5V)
- Up to 35MHz reference frequency (VDD=4.5V)
- 5 to 65535 programmable reference frequency divider ratio
- 1056 to 65535 programmable input frequency divider ratio
- Lock detector
- Either Active or Passive filter can be externally used.
- 16-pin plastic DIP and 16-pin S-SOP
- Molybdenum gate CMOS structure

PIN OUT

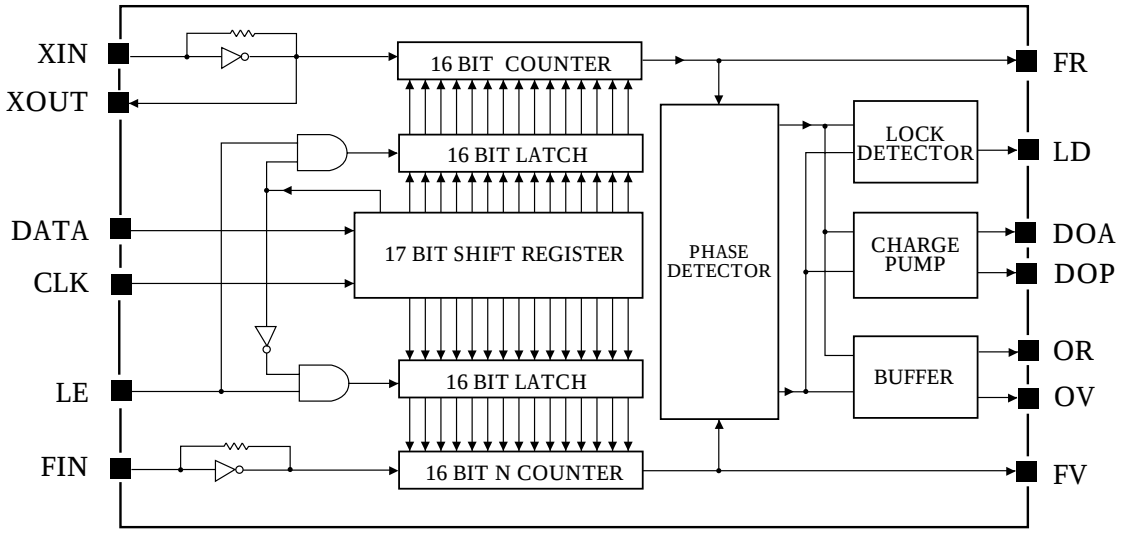
16-pin SSOP



16-pin DIP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	XIN	To connect external crystal and capacitor, or external clock input pin.
2	XOUT	To connect external crystal and capacitor,or oscilator output signal can be available at this pin.
3	FV	Buffered input frequency divider output.phase detector input
4	VDD	Positive supply pin. Apply +2.7 to 5.5 Volts.
5	DOP	Charge pump output for passive lowpass filter. Single ended tristate output.
6	VSS	Ground.
7	LD	Lock detector output. Logic Low when PLL is unlocked.
8	FIN	Comparison frequency input.Internal feedback resistor for AC coupling. Input frequency range 20MHz to 200MHz.
9	CLK	Shift register clock input.
10	DATA	Serial data input.
11	LE	Latch enable input.
12	DOA	Chrage pump output for active lowpass filter. Single ended tristate output.
13	FR	Buffered reference frequency devider output. Phase detector input.
14	TEST	Test pin. Left open.
15	OV	Buffered phase detector output to a differential lowpass filter.
16	OR	Buffered phase detector output to a differential lowpass filter.

SPECIFICATION

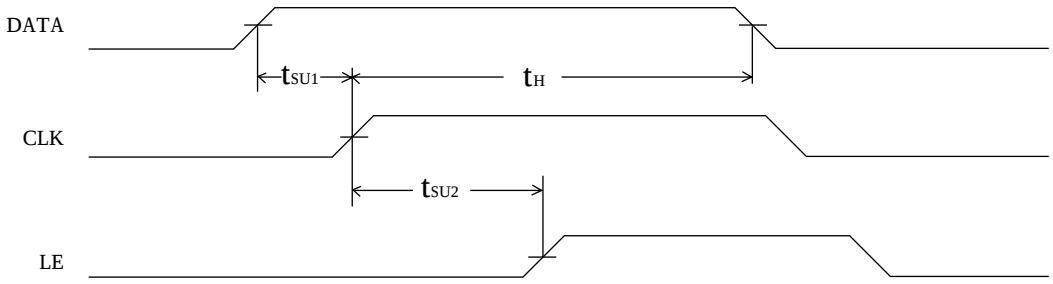
Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD} - V_{SS}	-0.3 to 7.0	V
Input voltage range	V_{IN}	V_{SS}-0.3 to V_{DD}+0.3	V
Operating temperature range	T_{OPR}	-30 to +85	deg.C
Storange temperature	Tstg	-40 to 125	deg.C
Solding temperature	Tsld	255	deg.C
Solding time	tsld	10	S

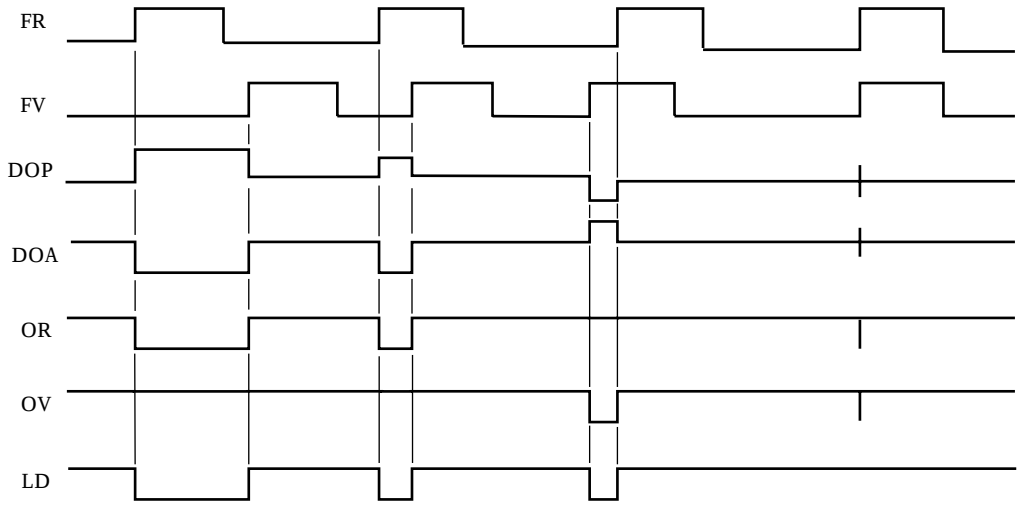
Electrical Characteristics

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply Voltage	V_{DD}		2.7		5.5	V
Supply current in operating mode	I_{DD}	F_{IN} 200MHz , V_{FIN}=0.5Vp-p sine wave X_{IN}=20MHz, V_{FIN}=0.5Vp-p sine wave		10	23.5	mA
Supply current in stanby mode	I_{DD2}	R/N latch's all bits="0"	-	-	10	uA
FIN maximum operating frequency	fmax1	F_{IN}=0.5Vp-p , sine wave (V_{DD}=2.7V)	100	120		MHz
		F_{IN}=0.5Vp-p , sine wave (V_{DD}=4.5V)	200	240		
XIN maximum operating frequency	fmax2	X_{IN}=0.5Vp-p , sine wave(V_{DD}=2.7V)	20			
		X_{IN}=0.5Vp-p , sine wave(V_{DD}=4.5V)	35			
FIN minimum operating frequency	fmin1	F_{IN}=0.5Vp-p , sine wave			20	
XIN minimum operating frequency	fmin2	F_{IN}=0.5Vp-p , sine wave			1	
FIN input voltage	V_{FIN}	f_{FIN} = 20 to 200MHz sine wave , AC coupling	0.5		V_{DD}-0.5	Vp-p
XIN input voltage	V_{XIN}	f_{XIN} = 1 to 35MHz sine wave , AC coupling	0.5		V_{DD}-0.5	Vp-p
CLK, DATA, LE HIGH-level input voltage	V_{IH}		V_{DD}-0.3			uA
CLK, DATA, LE LOW-level input voltage	V_{IL}				0.3	uA
FIN HIGH-level input current	I_{IH1}	V_{IH}=V_{DD}			100	uA
FIN LOW-level input current	I_{IL1}	V_{IL}=0V			100	uA
XIN HIGH-level input current	I_{IH2}	V_{IH}=V_{DD}			100	uA
XIN LOW-level input current	I_{IL2}	V_{IL}=0V			100	uA
FV, DOP, LD,DOA, FR, OV, OR, HIGH-level output current	I_{OH}	V_{OH}=V_{DD}-0.4V	0.4			mA
FV, DOP, LD,DOA, FR, OV, OR, LOW-level output current	I_{OL}	V_{OL}=0.4V	0.4			mA
DATA to CLK and CLK to LE setup time	tsu1		80			ns
	tsu2		80			ns
Hold time	tH		80			ns

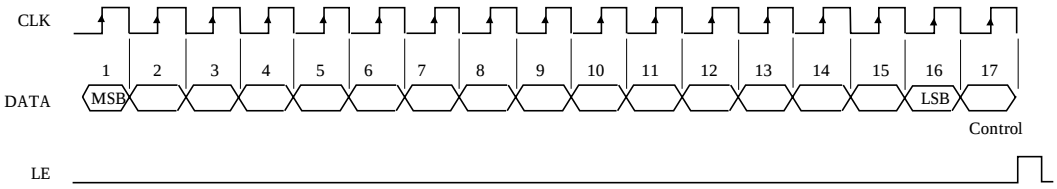
Serial data input timing



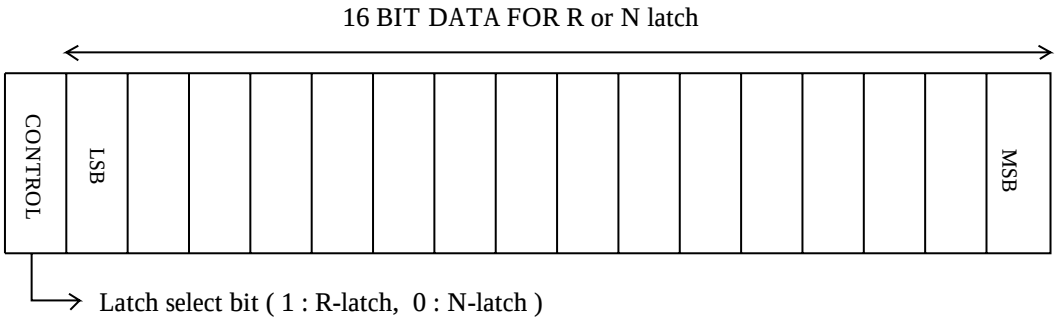
Phase detector timing



DIVIDER DATA SETTING PROCEDURE

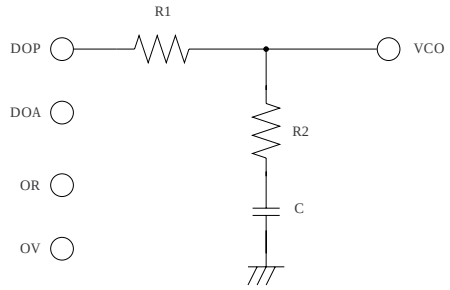


Input data must be MSB first. Final bit(17th bit) is assigned to the control bit.
Data are written into shift register at the rising edge of the CLK signal.
When LE is HIGH,data is transferred from the shift register to either the latch of reference divider or input divider. Thus data must be written on the shift register while LE is remaining LOW.
While all bits of the N latch to are "0", the N counter will be disabled, DOA, DOP are floating,and the supply current will be decreased.
While all bits of the R latch are "O", oscillator will be disabled.
While all bits of R and N latches are "0", supply current decreases to 10uA or less.

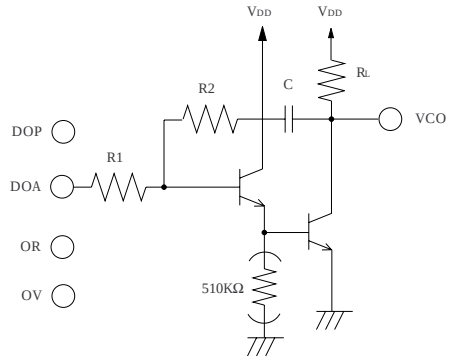


LOW PASS FILTERS

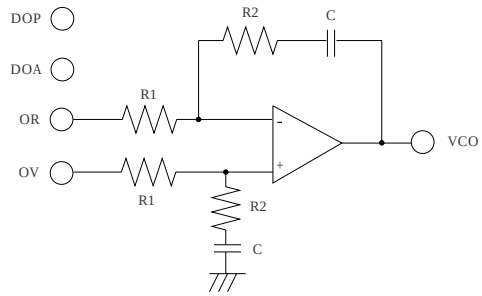
a. Passive filter



b. Active filter



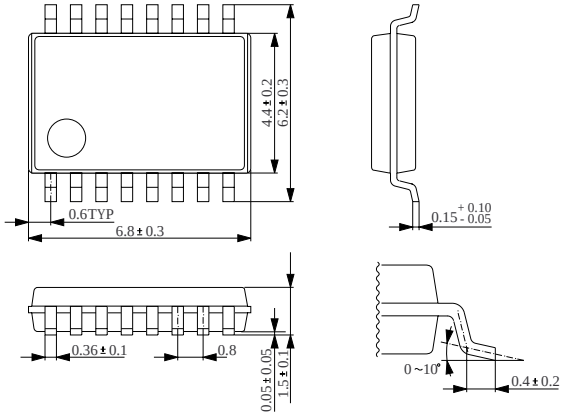
c. Differential filter



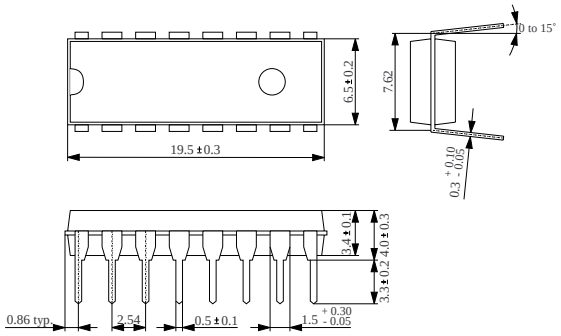
PACKAGE DIMENSIONS

UNIT:mm

16pin SSOP



16pin DIP



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