NEC

MOS INTEGRATED CIRCUIT

μPD75P0076

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD75P0076 replaces the μPD750068's internal mask ROM with a one-time PROM and features expanded ROM capacity.

Because the μPD75P0076 supports programming by users, it is suitable for use in prototype testing for system development using the μPD750064, 750066, and 750068 products, and for use in small-lot production.

Detailed information about function is provided in the following user's manual.
Be sure to read it before designing:
μPD750068 User's Manual: U10670E

FEATURES

- ○ Compatible with μPD750068
- ○ Memory capacity:
  - PROM : 16384 x 8 bits
  - RAM : 512 x 4 bits
- ○ Can operate with same power supply voltage as the mask ROM version μPD750068
  V_{DD} = 1.8 to 5.5 V
- ○ On-chip A/D converter capable of low-voltage operation (AV_{REF} = 1.8 to 5.5 V)
  8-bit resolution x 8 channels
- ○ Small shrink SOP package

ORDERING INFORMATION

Part Number	Package
μPD75P0076CU	42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)
μPD75P0076GT	42-pin plastic shrink SOP (375 mil, 0.8-mm pitch)

Caution On-chip pull-up resistors by mask option cannot be provided.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

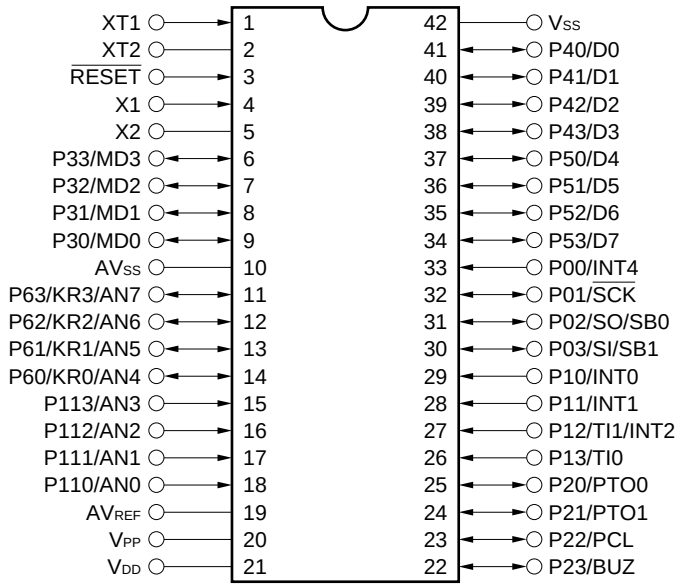
Functional Outline

Parameter		Function
Instruction execution time		• 0.95, 1.91, 3.81, 15.3 μs (@ 4.19 MHz with main system clock) • 0.67, 1.33, 2.67, 10.7 μs (@ 6.0 MHz with main system clock) • 122 μs (@ 32.768 kHz with subsystem clock)
On-chip memory	PROM	16384 x 8 bits
	RAM	512 x 4 bits
General-purpose register		• 4-bit operation: 8 x 4 banks • 8-bit operation: 4 x 4 banks
Input/output port	CMOS input	12 — Connections of on-chip pull-up resistors can be specified by software: 7 Also used for analog input pins: 4
	CMOS input/output	12 — Connections of on-chip pull-up resistors can be specified by software: 12 Also used for analog input pins: 4
★	N-ch open-drain input/output pins	8 — 13-V withstand voltage
	Total	32
Timer		4 channels • 8-bit timer/event counter: 2 channels (can be used as the 16-bit timer/event counter) • 8-bit basic interval timer/watchdog timer: 1 channel • Watch timer: 1 channel
Serial interface		• 3-wire serial I/O mode ··· MSB or LSB can be selected for transferring first bit • 2-wire serial I/O mode
A/D converter		8-bit resolution x 8 channels ($1.8\ V \leq AV_{REF} \leq V_{DD}$)
Bit sequential buffer		16 bits
★ Clock output (PCL)		• Φ, 1.05 MHz, 262 kHz, 65.5 kHz (@ 4.19 MHz with main system clock) • Φ, 1.5 MHz, 375 kHz, 93.8 kHz (@ 6.0 MHz with main system clock)
Buzzer output (BUZ)		• 2, 4, 32 kHz (@ 4.19 MHz with main system clock or @ 32.768 kHz with subsystem clock) • 2.93, 5.86, 46.9 kHz (@ 6.0 MHz with main system clock)
Vectored interrupts		External: 3, Internal: 4
Test input		External: 1, Internal: 1
System clock oscillator		• Ceramic or crystal oscillator for main system clock oscillation • Crystal oscillator for subsystem clock oscillation
Standby function		STOP/HALT mode
Operating ambient temperature		T_A = –40 to +85 ˚C
Power supply voltage		V_{DD} = 1.8 to 5.5 V
Package		• 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch) • 42-pin plastic shrink SOP (375 mil, 0.8-mm pitch)

CONTENTS

1. PIN CONFIGURATION (Top View)

- **42-pin plastic shrink DIP (600 mil, 1.778-mm pitch)**
  μPD75P0076CU
- **42-pin plastic shrink SOP (375 mil, 0.8-mm pitch)**
  μPD75P0076GT

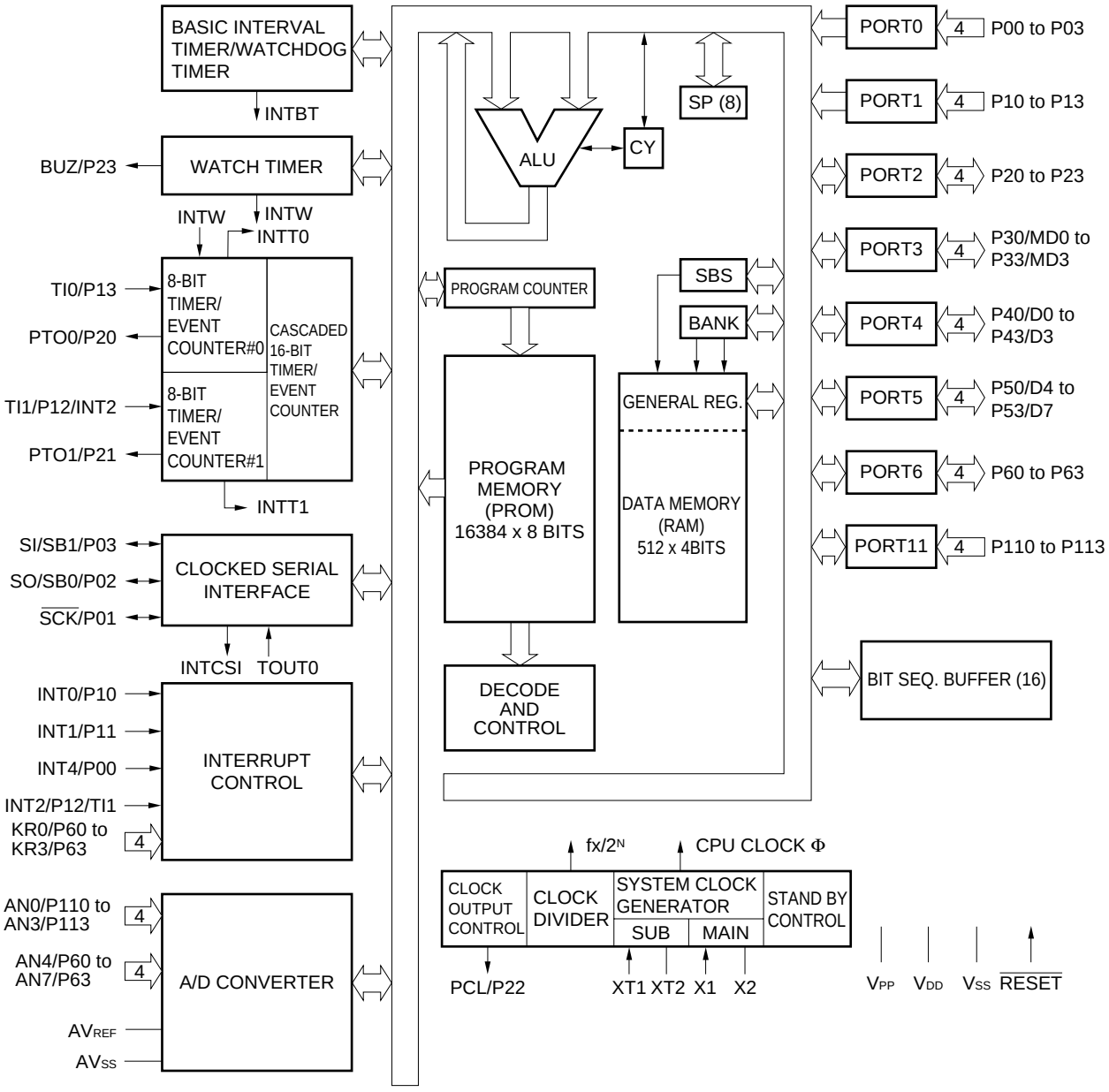


In normal operation mode, make sure to connect V_{PP} directly to V_{DD}.

Pin Identification

AN0 to AN7 : Analog Input 0 to 7
AV_{REF} : Analog Reference
AV_{SS} : Analog Ground
BUZ : Buzzer Clock
D0 to D7 : Data Bus 0 to 7
INT0, INT1, INT4 : External Vectored Interrupt 0, 1, 4
INT2 : External Test Input 2
KR0 to KR3 : Key Return
MD0 to MD3 : Mode Selection 0 to 3
P00 to P03 : Port 0
P10 to P13 : Port 1
P20 to P23 : Port 2
P30 to P33 : Port 3
P40 to P43 : Port 4
P50 to P53 : Port 5
P60 to P63 : Port 6
P110 to P113 : Port 11
PCL : Programmable Clock
PTO0, PTO1 : Programmable Timer Output 0, 1
$\overline{RESET}$: Reset Input
SB0, SB1 : Serial Data Bus 0, 1
$\overline{SCK}$: Serial Clock
SI : Serial Input
SO : Serial Output
TI0, TI1 : Timer Input 0, 1
V_{DD} : Positive Power Supply
V_{PP} : Programmable Power Supply
V_{SS} : Ground
X1, X2 : Main System Clock Oscillation 1, 2
XT1, XT2 : Subsystem Clock Oscillation 1, 2

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin name	I/O	Alternate function	Function	8-bit accessible	After reset	I/O circuit type[Note 1]
P00	I	INT4	This is a 4-bit input port (PORT0). For P01 to P03, on-chip pull-up resistors are software-specifiable in 3-bit units.	Not available	Input	<B>
P01	I/O	$\overline{SCK}$				<F>-A
P02	I/O	SO/SB0				<F>-B
P03	I/O	SI/SB1				<M>-C
P10	I	INT0	This is a 4-bit input port (PORT1). Connections of on-chip pull-up resistors are software-specifiable in 4-bit units. P10/INT0 can select a noise elimination circuit.	Not available	Input	<B>-C
P11		INT1				
P12		TI1/INT2				
P13		TI0				
P20	I/O	PTO0	This is a 4-bit I/O port (PORT2). Connections of on-chip pull-up resistors are software-specifiable in 4-bit units.	Not available	Input	E-B
P21		PTO1				
P22		PCL				
P23		BUZ				
P30	I/O	MD0	This is a programmable 4-bit I/O port (PORT3). Input and output can be specified in single-bit units. Connections of on-chip pull-up resistors are software-specifiable in 4-bit units.	Not available	Input	E-B
P31		MD1				
P32		MD2				
P33		MD3				
★ P40[Note 2]	I/O	D0	This is an N-ch open-drain 4-bit I/O port (PORT4). In the open-drain mode, withstands up to 13 V. Also used as data I/O pin (lower 4 bits) for program memory (PROM) write/verify.	Available	High impedance	M-E
P41[Note 2]		D1				
P42[Note 2]		D2				
P43[Note 2]		D3				
★ P50[Note 2]	I/O	D4	This is an N-ch open-drain 4-bit I/O port (PORT5). In the open-drain mode, withstands up to 13 V. Also used as data I/O pin (upper 4 bits) for program memory (PROM) write/verify.		High impedance	M-E
P51[Note 2]		D5				
P52[Note 2]		D6				
P53[Note 2]		D7				
P60	I/O	KR0/AN4	This is a programmable 4-bit I/O port (PORT6). Input and output can be specified in single-bit units. Connections of on-chip pull-up resistors are software-specifiable in 4-bit units.	Not available	Input	<Y>-D
P61		KR1/AN5				
P62		KR2/AN6				
P63		KR3/AN7				
P110	I	AN0	This is a 4-bit input port (PORT11).	Not available	Input	Y-A
P111		AN1				
P112		AN2				
P113		AN3				

Notes 1. Circuit types enclosed in brackets indicate Schmitt triggered inputs.

2. Low-level input current leakage increases when input instructions or bit manipulation instructions are executed.

3.2 Non-port Pins (1/2)

Pin name	I/O	Alternate function	Function		After reset	Circuit type[Note]
TI0	I	P13	Inputs external event pulses to the timer/event counter.		Input	<B>-C
TI1		P12/INT2				
PTO0	O	P20	Timer/event counter output		Input	E-B
PTO1		P21				
PCL		P22	Clock output			
BUZ		P23	Optional frequency output (for buzzer output or system clock trimming)			
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	<F>-A
SO/SB0		P02	Serial data output Serial data bus I/O			<F>-B
SI/SB1		P03	Serial data input Serial data bus I/O			<M>-C
INT4	I	P00	Edge detection vectored interrupt input (both rising edge and falling edge detection)			<B>
INT0	I	P10	Edge detection vectored interrupt input (detection edge can be selected). INT0/P10 can select a noise eliminator.	Noise eliminator/ asynchronous selection	Input	<B>-C
INT1		P11		Asynchronous		
INT2		P12/TI1	Rising edge detection testable input	Asynchronous		
KR0 to KR3	I	P60/AN4 to P63/AN7	Falling edge detection testable input		Input	<Y>-D
AN0 to AN3	I	P110 to P113	Analog signal input		Input	Y-A
AN4 to AN7		P60/KR0 to P63/KR3				<Y>-D
AV_{REF}	—	—	A/D converter reference voltage		—	Z-N
AV_{SS}	—	—	A/D converter reference GND potential		—	Z-N
X1	I	—	Crystal/ceramic connection pin for the main system clock oscillator. When inputting the external clock, input the external clock to pin X1, and the inverted phase of the external clock to pin X2.		—	—
X2	—					
XT1	I	—	Crystal connection pin for the subsystem clock oscillator. When the external clock is used, input the external clock to pin XT1, and the inverted phase of the external clock to pin XT2. Pin XT1 can be used as a 1-bit input (test) pin.		—	—
XT2	—					
$\overline{RESET}$	I	—	System reset input (low-level active)		—	<B>

★

Note Circuit types enclosed in brackets indicate Schmitt triggered inputs.

3.2 Non-port Pins (2/2)

Pin name	I/O	Alternate function	Function	After reset	Circuit type
MD0 to MD3	I	P30 to 33	Mode selection for program memory (PROM) write/verify.	Input	E-B
★ D0 to D3	I/O	P40 to 43	Data bus pin for program memory (PROM) write/verify.	Input	M-E
★ D4 to D7		P50 to 53			
V_{PP}[Note]	—	—	Programmable voltage supply in program memory (PROM) write/verify mode. In normal operation mode, connect directly to V_{DD}. Apply +12.5 V in PROM write/verify mode.	—	—
V_{DD}	—	—	Positive power supply	—	—
V_{SS}	—	—	Ground	—	—

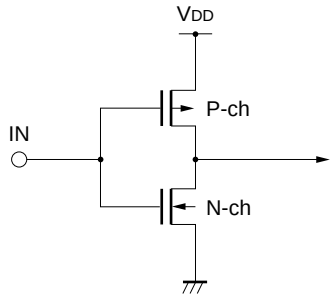
Note During normal operation, the V_{PP} pin will not operate normally unless connected to V_{DD} pin.

3.3 Equivalent Circuits for Pins

The equivalent circuits for the μPD75P0076's pin are shown in schematic diagrams below.

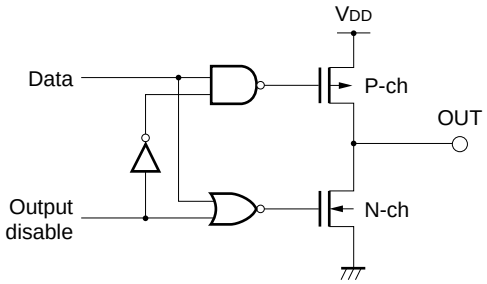
(1/3)

TYPE A



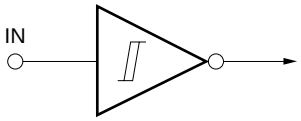
CMOS standard input buffer

TYPE D



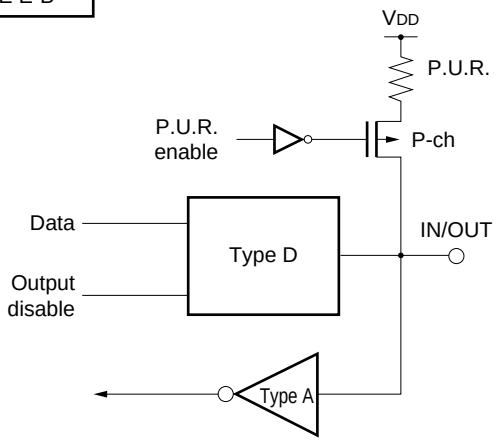
Push-pull output that can be set to high impedance output (with both P-ch and N-ch OFF).

TYPE B



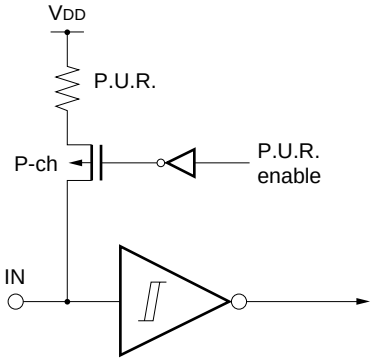
Schmitt trigger input with hysteresis characteristics.

TYPE E-B



P.U.R. : Pull-Up Resistor

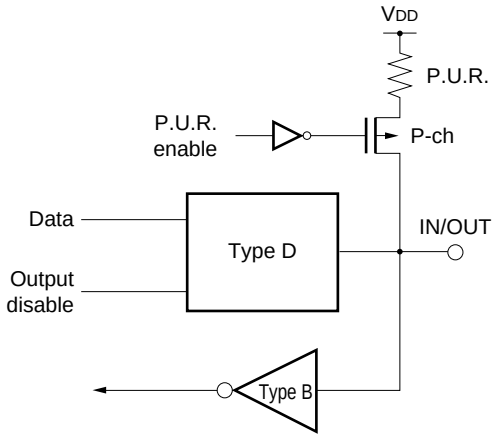
TYPE B-C



P.U.R. : Pull-Up Resistor

Schmitt trigger input with hysteresis characteristics.

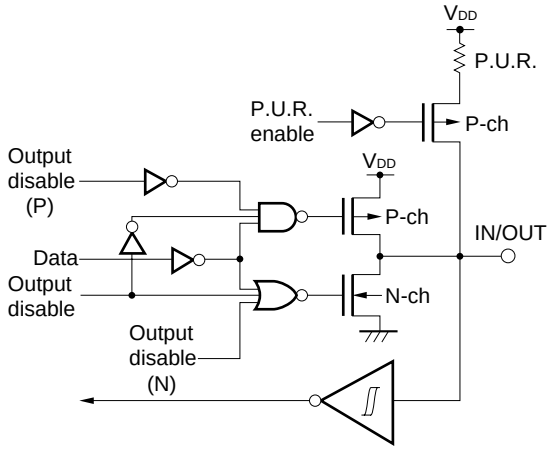
TYPE F-A



P.U.R. : Pull-Up Resistor

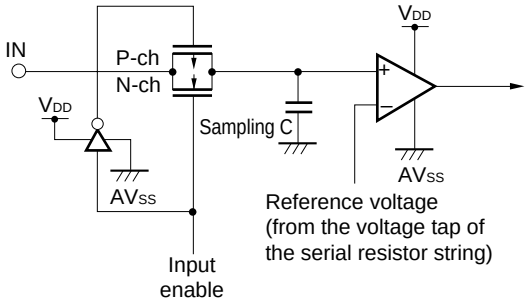
(2/3)

TYPE F-B

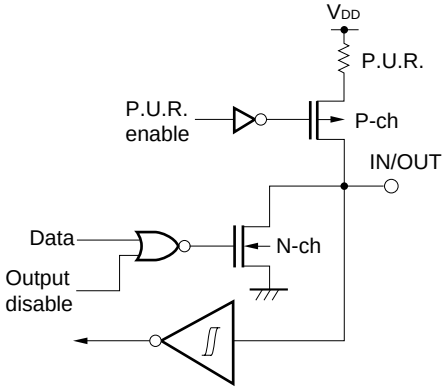


P.U.R. : Pull-Up Resistor

TYPE Y

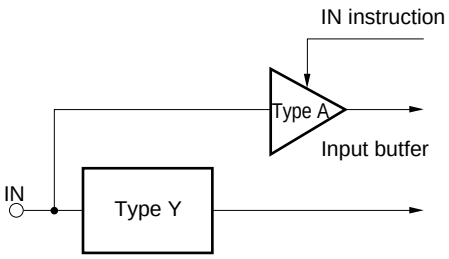


TYPE M-C

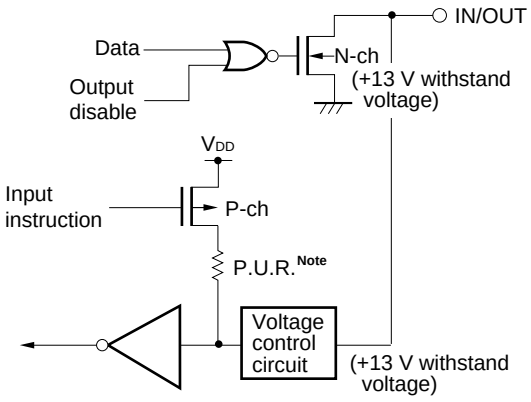


P.U.R. : Pull-Up Resistor

TYPE Y-A



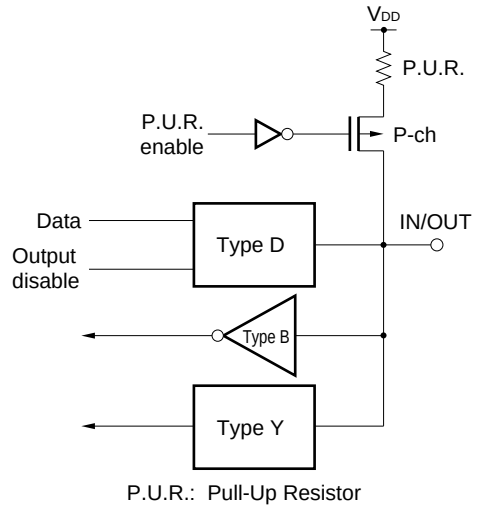
TYPE M-E*



Note This is a pull-up resistor which only operates when an input instruction is executed (when the pin is low a current flows from V_{DD} to the pin).

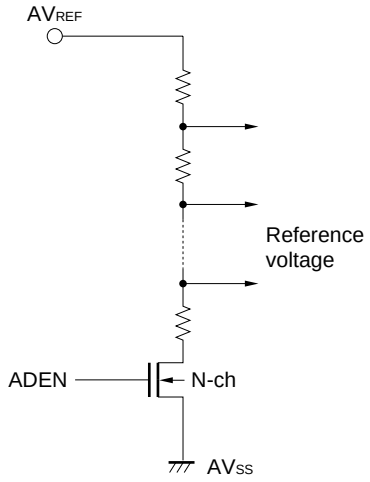
(3/3)

TYPE Y-D



P.U.R.: Pull-Up Resistor

TYPE Z-N



★ 3.4 Handling of Unused Pins

Pin	Recommended connection
P00/INT4	Connect to V_{SS} or V_{DD}
P01/$\overline{SCK}$	Independently connect to V_{SS} or V_{DD} through resistor
P02/SO/SB0	
P03/SI/SB1	Connected to V_{SS}
P10/INT0, P11/INT1	Connect to V_{SS} or V_{DD}
P12/TI1/INT2	
P13/TI0	
P20/PTO0	Input mode : independently connected to V_{SS} or V_{DD} through resistor Output mode : open
P21/PTO1	
P22/PCL	
P23/BUZ	
P30/MD0 to P33/MD3	
P40/D0 to P43/D3	Connected to V_{SS}
P50/D4 to P53/D7	
P60/KR0/AN4 to P63/KR3/AN7	Input mode : independently connected to V_{SS} or V_{DD} through resistor Output mode : open
P110/AN0 to P113/AN3	Connected to V_{SS} or V_{DD}
XT1[Note]	Connect to V_{SS} or V_{DD}
XT2[Note]	Open
V_{PP}	Make sure to connect directly to V_{DD}
AV_{REF}	Connect to V_{SS}
AV_{SS}	

Note When the subsystem clock is not used, set SOS.0 = 1 (on-chip feedback resistor is not used).

4. SWITCHING BETWEEN Mk I AND Mk II MODES

Setting a stack bank selection (SBS) register for the μPD75P0076 enables the program memory to be switched between the Mk I mode and the Mk II mode. This capability enables the evaluation of the μPD750064, 750066, and 750068 using the μPD75P0076.

When the SBS bit 3 is set to 1: sets Mk I mode (corresponds to Mk I mode of μPD750064, 750066, and 750068)
When the SBS bit 3 is set to 0: sets Mk II mode (corresponds to Mk II mode of μPD750064, 750066, and 750068)

4.1 Differences between Mk I Mode and Mk II Mode

Table 4-1 lists the differences between the Mk I mode and the Mk II mode of the μPD75P0076.

Table 4-1. Differences between Mk I Mode and Mk II Mode

Item		Mk I Mode	Mk II Mode
Program counter		$PC_{13 \text{ to } 0}$	
Program memory (bytes)		16384	
Data memory (bits)		512 x 4	
Stack	Stack bank	Selectable from memory banks 0 and 1	
	Stack bytes	2 bytes	3 bytes
Instruction	BRA !addr1 CALLA !addr1	Not provided	Provided
Instruction execution time	CALL !addr	3 machine cycles	4 machine cycles
	CALLF !faddr	2 machine cycles	3 machine cycles
Supported mask ROM versions and mode		Mk I mode of μPD750064, 750066, and 750068	Mk II mode of μPD750064, 750066, and 750068

★ **Caution The Mk II mode supports a program area which exceeds 16K bytes in the 75X and 75XL series. This mode enhances the software compatibility with products which have more than 16K bytes.**
When the Mk II mode is selected, the number of stack bytes used in execution of a subroutine call instruction increases by 1 per stack for the usable area compared to the Mk I mode. Furthermore, when a CALL !addr, or CALLF !faddr instruction is used, each instruction takes another machine cycle. Therefore, when more importance is attached to RAM utilization or throughput than software compatibility, use the Mk I mode.

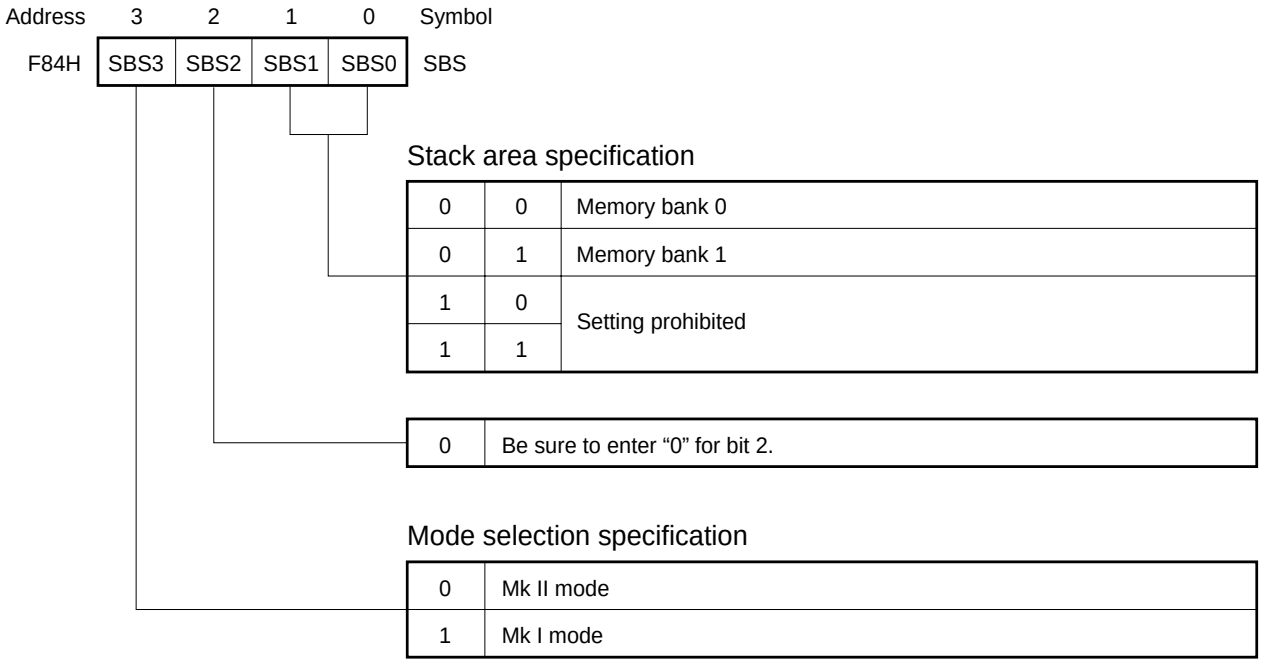
4.2 Setting of Stack Bank Selection (SBS) Register

Use the stack bank selection register to switch between the Mk I mode and the Mk II mode. Figure 4-1 shows the format for doing this.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 100xB[Note] at the beginning of the program. When using the Mk II mode, be sure to initialize it to 000xB[Note].

Note Set the desired value for x.

Figure 4-1. Format of Stack Bank Selection Register



Cautions 1. SBS3 is set to “1” after $\overline{\text{RESET}}$ input, and consequently the CPU operates in the Mk I mode. When using instructions for the Mk II mode, set SBS3 to “0” to enter the Mk II mode before using the instructions.

2. When using the Mk II mode, execute a subroutine call instruction and an interrupt instruction after $\overline{\text{RESET}}$ input and after setting the stack bank selection register.

5. DIFFERENCES BETWEEN μPD75P0076 AND μPD750064, 750066 AND 750068

The μPD75P0076 replaces the internal mask ROM in the μPD750064, 750066, and 750068 with a one-time PROM and features expanded ROM capacity. The μPD75P0076's Mk I mode supports the Mk I mode in the μPD750064, 750066, and 750068 and the μPD75P0076's Mk II mode supports the Mk II mode in the μPD750064, 750066, and 750068.
Table 5-1 lists differences among the μPD75P0076 and the μPD750064, 750066, 750068. Be sure to check the differences between corresponding versions beforehand, especially when a PROM version is used for debugging or prototype testing of application systems and later the corresponding mask ROM version is used for full-scale production.
For further description of CPU functions and internal hardware, see the **μPD750064 and 750068 Preliminary Product Information (U10165E)**.

★ **Table 5-1. Differences between μPD75P0076 and μPD750064, 750066, 750068**

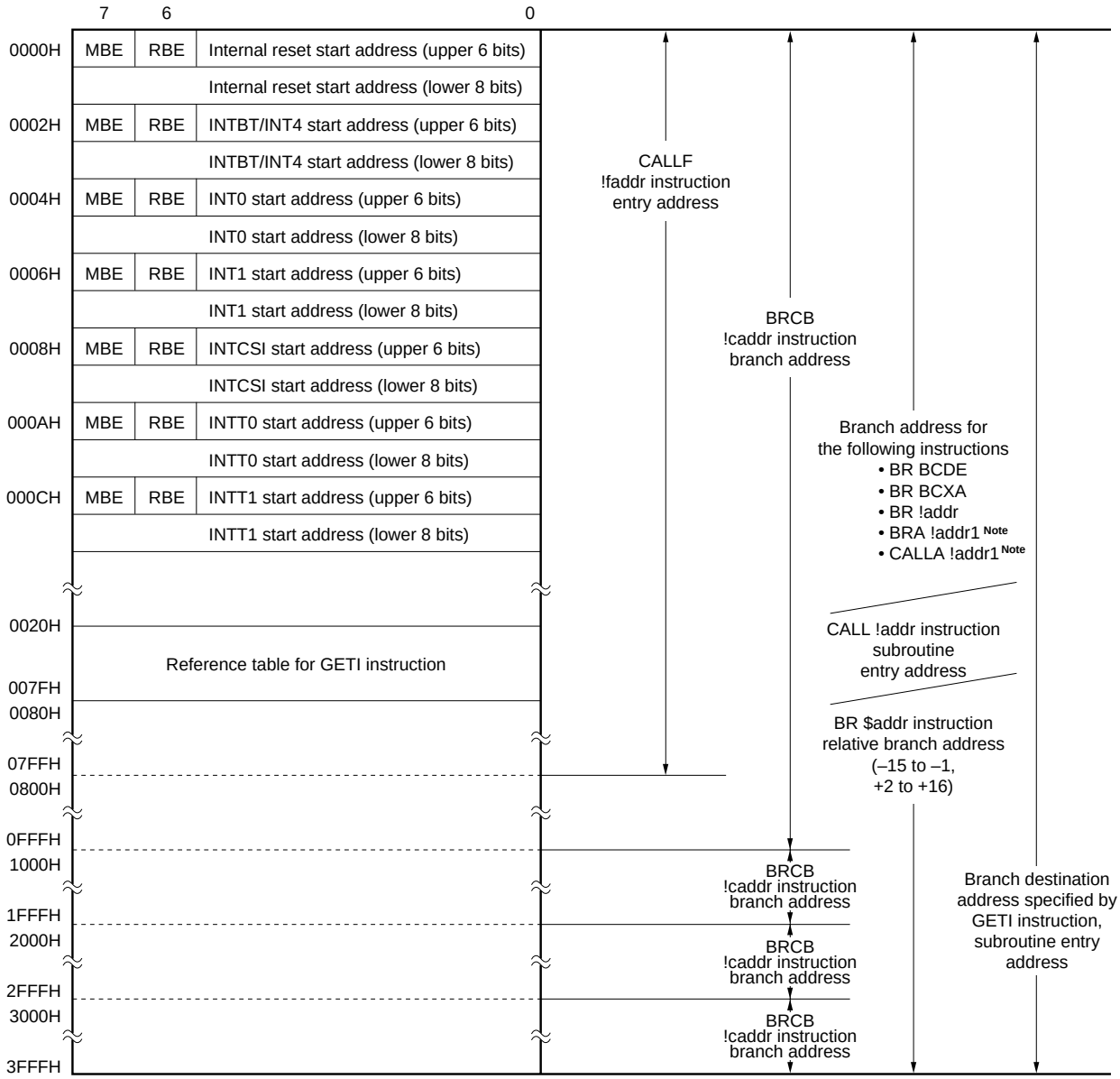
Item		μPD750064	μPD750066	μPD750068	μPD75P0076
Program counter		12-bit		13-bit	14-bit
Program memory (bytes)		Mask ROM 4096	Mask ROM 6144	Mask ROM 8192	One-time PROM 16384
Data memory (x 4 bits)		512			
Mask options	Pull-up resistor for ports 4 and 5	Yes (on-chip specifiable)			No (off chip)
	$\overline{\text{Wait}}$ time when $\overline{\text{RESET}}$	Yes ($2^{17}/f_X$, $2^{15}/f_X$ selectable)[Note]			No (fixed at $2^{15}/f_X$)[Note]
	Feedback resistor of subsystem clock	Yes (Use/not use selectable)			No (Use)
Pin configuration	Pins 6 to 9	P33 to P30			P33/MD3 to P30/MD0
	Pin 20	IC			V_{PP}
	Pins 34 to 37	P53 to P50			P53/D7 to P53/D4
	Pins 38 to 41	P43 to P40			P43/D3 to P40/D0
Other		Noise resistance and noise radiation may differ due to different circuit complexities and mask layouts.			

Note $2^{17}/f_X$ is 21.8 ms in 6.0 MHz operation and 31.3 ms in 4.19 MHz operation.
$2^{15}/f_X$ is 5.46 ms in 6.0 MHz operation and 7.81 ms in 4.19 MHz operation.

Caution Noise resistance and noise radiation are different in PROM version and mask ROM versions. If using a mask ROM version instead of the PROM version for processes between prototype development and full production, be sure to fully evaluate the CS of the mask ROM version (not ES).

6. MEMORY CONFIGURATION

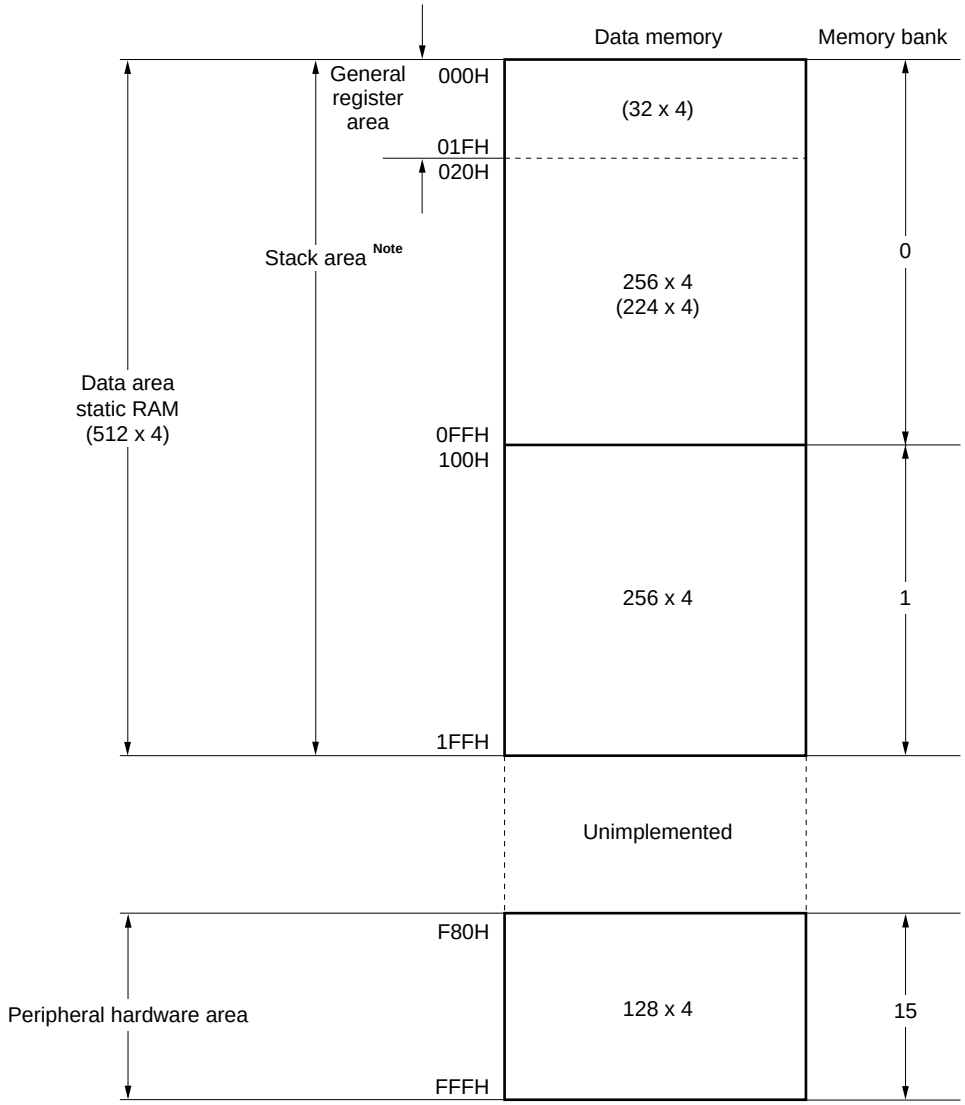
Figure 6-1. Program Memory Map



★ **Note** Can be used only in Mk II mode.

Remark For instructions other than those noted above, the “BR PCDE” and “BR PCXA” instructions can be used to branch to addresses with changes in the PC’s lower 8 bits only.

Figure 6-2. Data Memory Map



Note Either memory bank 0 or 1 can be selected as the stack area.

7. INSTRUCTION SET

(1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, see the **RA75X Assembler Package User's Manual–Language (EEU-1363)**). When there are several codes, select and use just one. Uppercase letters, and + and – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Instead of mem, fmem, pmem, bit, etc., a register flag symbol can be described as a label descriptor (for further description, see the **μPD750068 User's Manual (U10670E)**). Labels that can be entered for fmem and pmem are restricted.

Representation	Coding format
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL–, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label[Note]
bit	2-bit immediate data or label
fmem	FB0H to FBFH, FF0H to FFFH immediate data or label
pmem	FC0H to FFFH immediate data or label
addr	0000H to 3FFFH immediate data or label
addr1	000H to 3FFFH immediate data or label (in Mk II mode only)
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H to 7FH immediate data (however, bit0 = 0) or label
PORTn	PORT0 to PORT6, PORT11
IEXXX	IEBT, IECSI, IET0, IET1, IE0 to IE2, IE4, IEW
RBn	RB0 to RB3
MBn	MB0, MB1, MB15

Note When processing 8-bit data, only even addresses can be specified.

(2) Operation legend

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC)
DE	: Register pair (DE)
HL	: Register pair (HL)
XA'	: Expansion register pair (XA')
BC'	: Expansion register pair (BC')
DE'	: Expansion register pair (DE')
HL'	: Expansion register pair (HL')
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORTn	: Port n (n = 0 to 6, 11)
IME	: Interrupt master enable flag
IPS	: Interrupt priority select register
IExxx	: Interrupt enable flag
RBS	: Register bank select register
MBS	: Memory bank select register
PCC	: Processor clock control register
.	: Delimiter for address and bit
(xx)	: Contents of address xx
xxH	: Hexadecimal data

(3) Description of symbols used in addressing area

*1	MB = MBE • MBS MBS = 0, 1, 15	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H to 07FH) MB = 15 (F80H to FFFH) MBE = 1 : MB = MBS MBS = 0, 1, 15	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 0000H to 3FFFH	Program memory addressing
*7	addr, addr1 = (Current PC) –15 to (Current PC) –1 (Current PC) +2 to (Current PC) +16	
*8	caddr = 0000H to 0FFFH ($PC_{13, 12}$ = 00B) or 1000H to 1FFFH ($PC_{13, 12}$ = 01B) or 2000H to 2FFFH ($PC_{13, 12}$ = 10B) or 3000H to 3FFFH ($PC_{13, 12}$ = 11B)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	
*11	addr1 = 0000H to 3FFFH (Mk II mode only)	

Remarks 1. MB indicates access-enabled memory banks.

2. In area *2, MB = 0 for both MBE and MBS.

3. In areas *4 and *5, MB = 15 for both MBE and MBS.

4. Areas *6 to *11 indicate corresponding address-enabled areas.

(4) Description of machine cycles

S indicates the number of machine cycles required for skipping of skip-specified instructions. The value of S varies as shown below.

- No skip ..... S = 0
- Skipped instruction is 1-byte or 2-byte instruction ..... S = 1
- Skipped instruction is 3-byte instruction[Note] ..... S = 2

Note 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, CALLA !addr1

Caution The GETI instruction is skipped for one machine cycle.

One machine cycle equals one cycle (= t_{CY}) of the CPU clock Φ. Use the PCC setting to select among four cycle times.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A ← n4		String-effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String-effect A
		HL, #n8	2	2	HL ← n8		String-effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2 + S	A ← (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ← (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg1	2	2	A ← reg1		
		XA, rp’	2	2	XA ← rp’		
		reg1, A	2	2	reg1 ← A		
		rp’1, XA	2	2	rp’1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2 + S	A ↔ (HL), then L ← L + 1	*1	L = 0
		A, @HL–	1	2 + S	A ↔ (HL), then L ← L – 1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp’	2	2	XA ↔ rp’		
Table reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8} + XA)_{ROM}$		
		XA, @BCDE	1	3	XA ← $(BCDE)_{ROM}$ Note	*11	
		XA, @BCXA	1	3	XA ← $(BCXA)_{ROM}$ Note	*11	

Note As for the B register, only the lower 2 bits are valid.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← (H + mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H + mem.bit, CY	2	2	(H + mem_{3-0}.bit) ← CY	*1	
Operation	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		XA, #n8	2	2 + S	XA ← XA + n8		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
		XA, rp’	2	2 + S	XA ← XA + rp’		carry
		rp’1, XA	2	2 + S	rp’1 ← rp’1 + XA		carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
		XA, rp’	2	2	XA, CY ← XA + rp’ + CY		
		rp’1, XA	2	2	rp’1, CY ← rp’1 + XA + CY		
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
		XA, rp’	2	2 + S	XA ← XA – rp’		borrow
		rp’1, XA	2	2 + S	rp’1 ← rp’1 – XA		borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
		XA, rp’	2	2	XA, CY ← XA – rp’ – CY		
		rp’1, XA	2	2	rp’1, CY ← rp’1 – XA – CY		
	AND	A, #n4	2	2	A ← A∧n4		
		A, @HL	1	1	A ← A∧(HL)	*1	
		XA, rp’	2	2	XA ← XA∧rp’		
		rp’1, XA	2	2	rp’1 ← rp’1∧XA		
	OR	A, #n4	2	2	A ← A∨n4		
		A, @HL	1	1	A ← A∨(HL)	*1	
		XA, rp’	2	2	XA ← XA∨rp’		
		rp’1, XA	2	2	rp’1 ← rp’1∨XA		
	XOR	A, #n4	2	2	A ← A∀n4		
		A, @HL	1	1	A ← A∀(HL)	*1	
		XA, rp’	2	2	XA ← XA∀rp’		
		rp’1, XA	2	2	rp’1 ← rp’1∀XA		

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Accumulator manipulate	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/ decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		rp1	1	1 + S	rp1 ← rp1 + 1		rp1 = 00H
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
		rp’	2	2 + S	rp’ ← rp’ – 1		rp’ = FFH
Compare	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA, rp’	2	2 + S	Skip if XA = rp’		XA = rp’
Carry flag manipulate	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Memory bit manipulate	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 1	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) ← 0	*5	
		@H + mem.bit	2	2	(H + mem$_{3-0}$.bit) ← 0	*1	
	SKT	mem.bit	2	2 + S	Skip if(mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if(fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if(H + mem$_{3-0}$.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if(mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if(fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if(H + mem$_{3-0}$.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if(fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$)) = 1 and clear	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if(H + mem$_{3-0}$.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY, fmem.bit	2	2	CY ← CY∧(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY∧(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY∧(H + mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY∨(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY∨(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY∨(H + mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY∀(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY∀(pmem$_{7-2}$ + L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H + mem.bit	2	2	CY ← CY∀(H + mem$_{3-0}$.bit)	*1	

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Branch	BR[Note 1]	addr	—	—	$PC_{13-0} \leftarrow$ addr (Assembler selects the most appropriate instruction among the following: • BR !addr • BRCB !caddr • BR $addr)	*6	
		addr1	—	—	$PC_{13-0} \leftarrow$ addr1 (Assembler selects the most appropriate instruction among the following: • BRA !addr1 • BR !addr • BRCB !caddr • BR $addr1)	*11	
		!addr	3	3	$PC_{13-0} \leftarrow$ addr	*6	
		$addr	1	2	$PC_{13-0} \leftarrow$ addr	*7	
		$addr1	1	2	$PC_{13-0} \leftarrow$ addr1		
		PCDE	2	3	$PC_{13-0} \leftarrow PC_{13-8} + DE$		
		PCXA	2	3	$PC_{13-0} \leftarrow PC_{13-8} + XA$		
		BCDE	2	3	$PC_{13-0} \leftarrow$ BCDE[Note 2]	*6	
		BCXA	2	3	$PC_{13-0} \leftarrow$ BCXA[Note 2]	*6	
	BRA[Note 1]	!addr1	3	3	$PC_{13-0} \leftarrow$ addr1	*11	
	BRCB	!caddr	2	2	$PC_{13-0} \leftarrow PC_{13, 12} + caddr_{11-0}$	*8	

Notes 1. Double boxes indicate support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

2. As for the B register, only the lower 2 bits are valid.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALLA[Note]	!addr1	3	3	(SP – 6)(SP – 3)(SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, $PC_{13,12}$ (SP – 2) ← X, X, MBE, RBE PC_{13-0} ← addr1, SP ← SP – 6	*11	
	CALL[Note]	!addr	3	3	(SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, $PC_{13, 12}$ PC_{13-0} ← addr, SP ← SP – 4	*6	
				4	(SP – 6)(SP – 3)(SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, $PC_{13, 12}$ (SP – 2) ← X, X, MBE, RBE PC_{13-0} ← addr, SP ← SP – 6		
	CALLF[Note]	!faddr	2	2	(SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, $PC_{13, 12}$ PC_{13-0} ← 000 + faddr, SP ← SP – 4	*9	
				3	(SP – 6)(SP – 3)(SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, $PC_{13, 12}$ (SP – 2) ← X, X, MBE, RBE PC_{13-0} ← 000 + faddr, SP ← SP – 6		
	RET[Note]		1	3	MBE, RBE, $PC_{13, 12}$ ← (SP + 1) PC_{11-0} → (SP)(SP + 3)(SP + 2) SP ← SP + 4		
					X, X, MBE, RBE ← (SP + 4) PC_{11-0} ← (SP)(SP + 3)(SP + 2) 0, 0, $PC_{13, 12}$ ← (SP + 1) SP ← SP + 6		
	RETS[Note]		1	3 + S	MBE, RBE, $PC_{13, 12}$ ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4 then skip unconditionally		Unconditional
					X, X, MBE, RBE ← (SP + 4) PC_{11-0} ← (SP)(SP + 3)(SP + 2) 0, 0, $PC_{13, 12}$ ← (SP + 1) SP ← SP + 6 then skip unconditionally		
	RETI		1	3	MBE, RBE, $PC_{13, 12}$ ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6		
					0, 0, $PC_{13, 12}$ ← SP + 1 PC_{11-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6		

Note Double boxes indicate support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

Group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	PUSH	rp	1	1	(SP – 1)(SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← RBS, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1)(SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), RBS ← (SP), SP ← SP + 2		
Interrupt control	EI		2	2	IME(IPS.3) ← 1		
		IEXXX	2	2	IEXXX ← 1		
	DI		2	2	IME(IPS.3) ← 0		
		IEXXX	2	2	IEXXX ← 0		
I/O	IN[Note 1]	A, PORTn	2	2	A ← PORTn (n = 0 to 6, 11)		
		XA, PORTn	2	2	XA ← PORTn + 1, PORTn (n = 4)		
	OUT[Note 1]	PORTn, A	2	2	PORTn ← A (n = 2 to 6)		
		PORTn, XA	2	2	PORTn + 1, PORTn ← XA (n = 4)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS ← n (n = 0 to 3)		
		MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI[Note 2, 3]	taddr	1	3	• When using TBR instruction $PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr + 1)$	*10	
					• When using TCALL instruction (SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← MBE, RBE, $PC_{13, 12}$ $PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr + 1)$ SP ← SP – 4		
					• When using instruction other than TBR or TCALL Execute (taddr)(taddr + 1) instructions		Determined by referenced instruction
			1	3	• When using TBR instruction $PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr + 1)$	*10	
				4	• When using TCALL instruction (SP – 6)(SP – 3)(SP – 4) ← PC_{11-0} (SP – 5) ← 0, 0, $PC_{13, 12}$ (SP – 2) ← X, X, MBE, RBE $PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr + 1)$ SP ← SP – 6		
				3	• When using instruction other than TBR or TCALL Execute (taddr)(taddr + 1) instructions		Determined by referenced instruction

Notes 1. Before executing the IN or OUT instruction, set MBE to 0 or 1 and set MBS to 15.

2. TBR and TCALL instructions are assembler pseudo-instructions for the GETI instruction's table definitions.

3. Double box indicates support for the Mk II mode only. Other areas indicate support for the Mk I mode only.

8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory in the μPD75P0076 is a 16384 x 8-bit electronic write-enabled one-time PROM. The pins listed in the table below are used for this PROM's write/verify operations. Clock input from the X1 pins is used instead of address input as a method for updating addresses.

Pin name	Function
V_{PP}	Pin (usually V_{DD}) where programming voltage is applied during program memory write/verify
X1, X2	Clock input pin for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin.
MD0 to MD3	Operation mode selection pin for program memory write/verify
D0/P40 to D3/P43 (lower 4) D4/P50 to D7/P53 (upper 4)	8-bit data I/O pin for program memory write/verify
V_{DD}	Pin where power supply voltage is applied. Power voltage range for normal operation is 1.8 to 5.5 V. Apply 6 V for program memory write/verify.

Caution Pins not used for program memory write/verify should be handled as follows.

- **All unused pins except XT2 ..... Connect to Vss via a pull-down resistor**
- **XT2 pin ..... Leave open**

8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the μPD75P0076's V_{DD} pin and +12.5 V is applied to its V_{PP} pin, program memory write/verify modes are in effect. Furthermore, the following detailed operation modes can be specified by setting pins MD0 to MD3 as shown below.

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Zero-clear program memory address
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

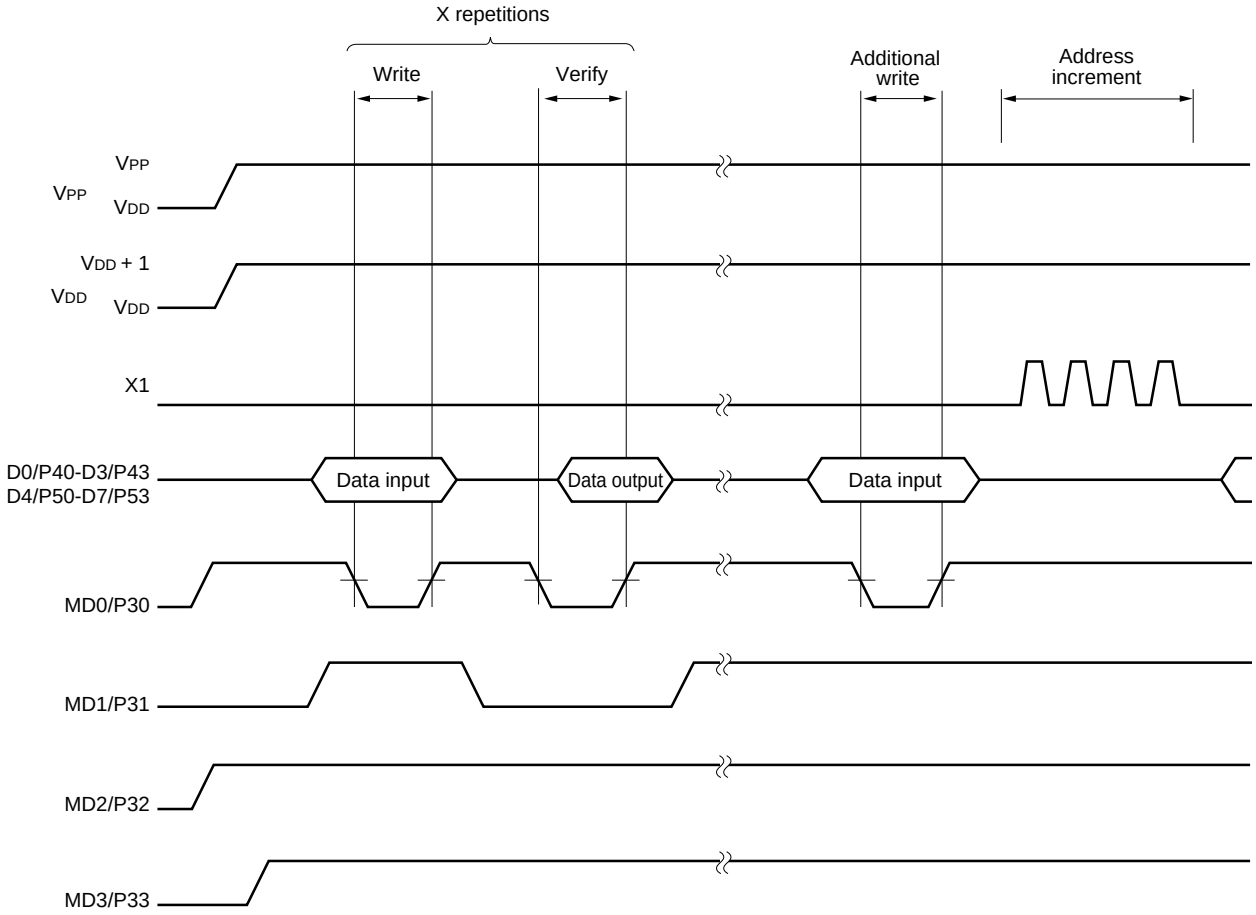
X: L or H

8.2 Steps in Program Memory Write Operation

High-speed program memory write can be executed via the following steps.

(1) Pull down unused pins to V_{SS} via resistors. Set the X1 pin to low.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Zero-clear mode for program memory addresses.
(5) Apply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Write data using 1-ms write mode.
(7) Verify mode. If write is verified, go to step (8) and if write is not verified, go back to steps (6) to (7).
(8) X [= number of write operations from steps (6) to (7)] x 1 ms additional write
(9) 4 pulse inputs to the X1 pin updates (increments +1) the program memory address.
(10) Repeat steps (6) to (9) until the last address is completed.
(11) Zero-clear mode for program memory addresses.
(12) Apply +5 V to the V_{DD} and V_{PP} pins.
(13) Power supply OFF

The following diagram illustrates steps (2) to (9).

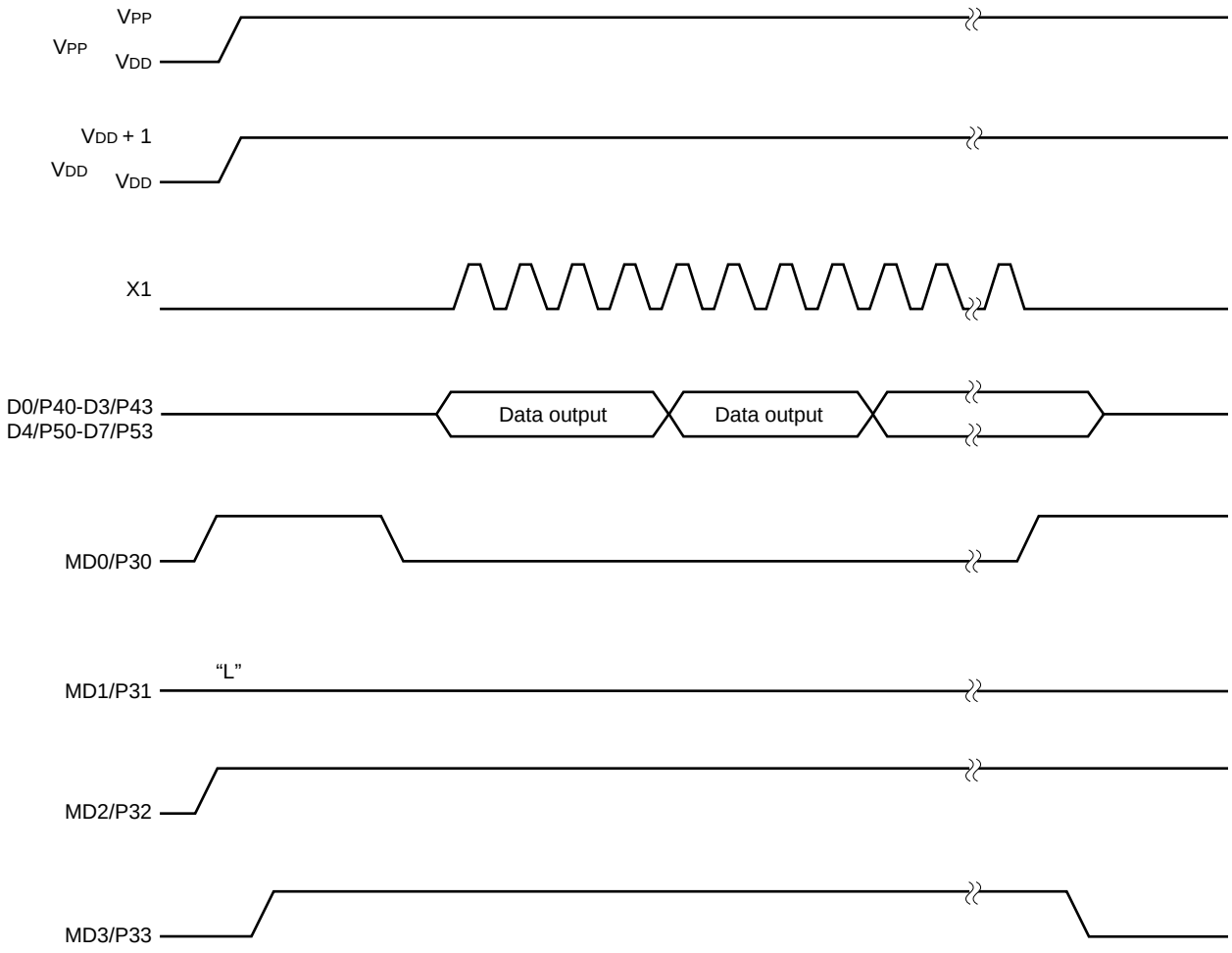


8.3 Steps in Program Memory Read Operation

The μPD75P0076 can read out the program memory contents via the following steps.

(1) Pull down unused pins to V_{SS} via resistors. Set the X1 pin to low.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Zero-clear mode for program memory addresses.
(5) Apply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Verify mode. When a clock pulse is input to the X1 pin, data is output sequentially to one address at a time based on a cycle of four pulse inputs.
(7) Zero-clear mode for program memory addresses.
(8) Apply +5 V to the V_{DD} and V_{PP} pins.
(9) Power supply OFF

The following diagram illustrates steps (2) to (7).



8.4 One-Time PROM Screening

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC. Therefore, NEC recommends the screening process, that is, after the required data is written to the PROM and the PROM is stored under the high-temperature conditions shown below, the PROM should be verified.

Storage temperature	Storage time
125 ˚C	24 hours

★ 9. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

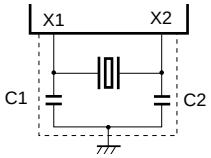
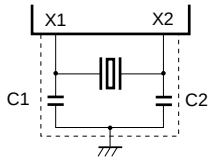
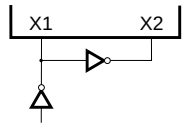
Parameter	Symbol	Test Conditions	Rating	Unit
Power supply voltage	V_{DD}		–0.3 to +7.0	V
PROM power supply voltage	V_{PP}		–0.3 to +13.5	V
Input voltage	V_{I1}	Except ports 4, 5	–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4, 5 (N-ch open drain)	–0.3 to +14	V
Output voltage	V_O		–0.3 to V_{DD} +0.3	V
Output current high	I_{OH}	Per pin	–10	mA
		Total of all pins	–30	mA
Output current low	I_{OL}	Per pin	30	mA
		Total of all pins	220	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the reliability of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

CAPACITANCE (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended constant	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (fx)Note 1		1.0		6.0Note 2	MHz
		Oscillation stabilization timeNote 3	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (fx) Note 1		1.0		6.0Note 2	MHz
		Oscillation stabilization timeNote 3	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx)Note 1		1.0		6.0Note 2	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		83.3		500	ns

Notes 1. The oscillation frequency and X1 input frequency indicate characteristics of the oscillator only. For the instruction execution time, refer to AC Characteristics.

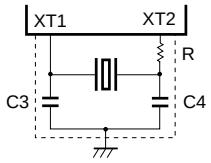
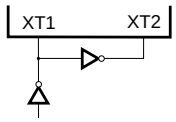
2. When the power supply voltage is 1.8 V ≤ V_{DD} < 2.7 V and the oscillation frequency is 4.19 MHz < fx ≤ 6.0 MHz, setting the processor clock control register (PCC) to 0011 results in 1 machine cycle being less than the required 0.95 μs. Therefore, set PCC to a value other than 0011.

3. The oscillation stabilization time is necessary for oscillation to stabilize after applying V_{DD} or releasing the STOP mode.

Caution When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended constant	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.0	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. The oscillation stabilization time is necessary for oscillation to stabilize after applying V_{DD}.

Caution When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

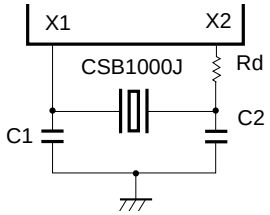
The subsystem clock oscillator is designed as a low amplification circuit to provide low consumption current, causing misoperation by noise more frequently than the main system clock oscillation circuit. Special care should therefore be taken for wiring method when the subsystem clock is used.

RECOMMENDED OSCILLATION CIRCUIT CONSTANTS

CERAMIC RESONATOR (T_A = –20 to +80 °C)

Manufacturer	Product Name	Frequency (MHz)	Oscillation Circuit Constants (pF)		Oscillation Voltage Range (V_{DD})		Remarks
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSB1000J[Note]	1.0	100	100	2.2	5.5	Rd = 5.6 KΩ
	CSA2.00MG040	2.0	100	100	2.0		—
	CST2.00MG040		—	—			With on-chip capacitor
	CSA4.00MG	4.0	30	30	1.8		—
	CST4.00MGW		—	—			With on-chip capacitor
	CSA4.19MG	4.19	30	30			—
	CST4.19MGW		—	—			With on-chip capacitor
	CSA6.00MG	6.0	30	30	2.6		—
	CST6.00MGW		—	—			With on-chip capacitor
	CSA6.00MGU		30	30	1.8		—
	CST6.00MGWU		—	—			With on-chip capacitor

Note When the CSB1000J (1.0 MHz) manufactured by Murata Mfg. is used as a ceramic resonator, a limiting resistor (Rd = 5.6 kΩ) is required (see the figure below). Other recommended resonators do not require such a limiting resistor.



Caution The oscillation circuit constants and oscillation voltage range only indicate the conditions under which the circuit can oscillate stably, and do not guarantee the oscillation frequency accuracy. If oscillation frequency accuracy is required in the actual circuit, it is necessary to adjust oscillation frequencies in the actual circuit, and you should consult directly with the manufacturer of the resonator used.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Output current low	I_{OL}	Per pin				15	mA
		Total of all pins				150	mA
Input voltage high	V_{IH1}	Ports 2, 3, and 11	2.7 ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, $\overline{\text{RESET}}$	2.7 ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5	2.7 ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		13	V
		(N-ch open-drain)	1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		13	V
	V_{IH4}	X1, XT1		V_{DD} – 0.1		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2-5, 11	2.7 ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, $\overline{\text{RESET}}$	2.7 ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL3}	X1, XT1		0		0.1	V
Output voltage high	V_{OH}	$\overline{\text{SCK}}$, SO, Ports 2, 3, 6 I_{OH} = –1.0 mA		V_{DD} – 0.5			V
Output voltage low	V_{OL1}	$\overline{\text{SCK}}$, SO, Ports 2-6	I_{OL} = 15 mA, V_{DD} = 4.5 to 5.5 V		0.2	2.0	V
			I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1	When N-ch open-drain pull-up resistor ≥ 1 kΩ			0.2V_{DD}	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1, XT1			3	μA
	I_{LIH2}		X1, XT1			20	μA
	I_{LIH3}	V_{IN} = 13 V	Ports 4, 5 (N-ch open-drain)			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Ports 4, 5, pins other than X1, XT1			–3	μA
	I_{LIL2}		X1, XT1			–20	μA
	I_{LIL3}		Ports 4, 5 (N-ch open-drain) When input instruction is not executed			–3	μA
			Ports 4, 5 (N-ch open-drain) When input instruction is executed			–30	μA
				V_{DD} = 5.0 V		–10	–27	μA
				V_{DD} = 3.0 V		–3	–8	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	$\overline{\text{SCK}}$, SO/SB0, SB1, Ports 2, 3, 6			3	μA
	I_{LOH2}	V_{OUT} = 13 V	Ports 4, 5 (N-ch open-drain)			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
On-chip pull-up resistor	R_L	V_{IN} = 0 V	Ports 0-3, 6 (Excluding P00 pin)	50	100	200	kΩ

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions			MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	6.0 MHz Note 2 Crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ± 10% Note 3			3.4	10.2	mA
			V_{DD} = 3.0 V ± 10% Note 4			0.8	2.4	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10%		0.9	2.7	mA
				V_{DD} = 3.0 V ± 10%		0.5	1.5	mA
	I_{DD1}	4.19 MHz Note 2 Crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ± 10% Note 3			2.7	7.4	mA
			V_{DD} = 3.0 V ± 10% Note 4			0.6	1.8	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10%		0.8	2.4	mA
				V_{DD} = 3.0 V ± 10%		0.4	1.2	mA
	I_{DD3}	32.768 kHz Note 5 Crystal oscillation	Low-voltage mode Note 6	V_{DD} = 3.0 V ± 10%		42	126	μA
				V_{DD} = 2.0 V ± 10%		23	69	μA
				V_{DD} = 3.0 V, T_A = 25°C		42	84	μA
			Low current consumption mode Note 7	V_{DD} = 3.0 V ± 10%		40	120	μA
				V_{DD} = 3.0 V, T_A = 25°C		40	80	μA
	I_{DD4}		HALT mode	Low-voltage mode Note 6	V_{DD} = 3.0 V ± 10%	8	24	μA
					V_{DD} = 2.0 V ± 10%	4	12	μA
					V_{DD} = 3.0 V, T_A = 25°C	8	16	μA
				Low current consumption mode Note 7	V_{DD} = 3.0 V ± 10%	7	21	μA
					V_{DD} = 3.0 V, T_A = 25°C	7	14	μA
	I_{DD5}	XT1 = 0 V STOP mode Note 8	V_{DD} = 5.0 V ± 10%			0.05	10	μA
			V_{DD} = 3.0 V ± 10%			0.02	5.0	μA
				T_A = 25°C		0.02	3.0	μA

Notes 1. Not including currents flowing in on-chip pull-up resistors.

2. Including oscillation of the subsystem clock.

3. When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

4. When PCC is set to 0000 and the device is operated in the low-speed mode.

5. When the system clock control register (SCC) is set to 1001 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

6. When the sub-oscillation circuit control register (SOS) is set to 0000.

7. When SOS is set to 0010.

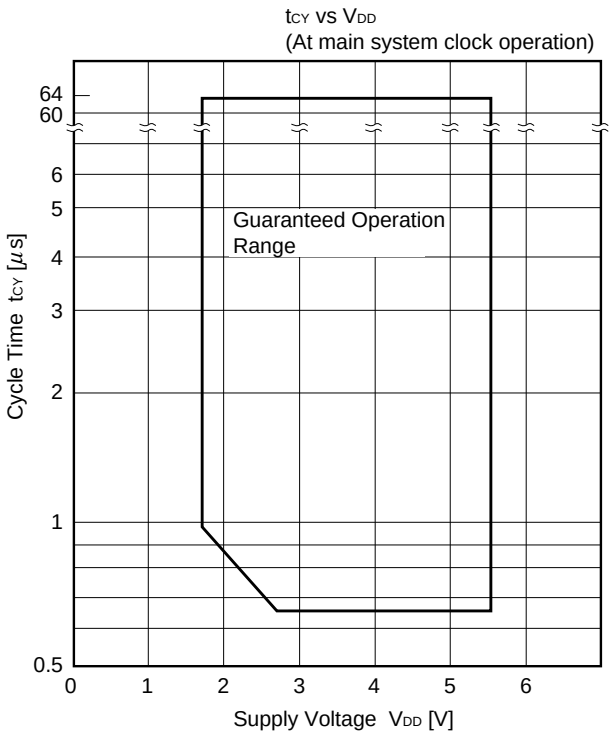
8. When SOS is set to 00×1, the feedback resistors of the sub-oscillation circuit is cutoff. (×: don't care)

AC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note 1 (Minimum instruction execution time = 1 machine cycle)	t_{CY}	Operating on main system clock	V_{DD} = 2.7 to 5.5 V	0.67		64	μs
				0.95		64	μs
		Operating on subsystem clock		114	122	125	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1.0	MHz
				0		275	kHz
TI0, TI1 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 2**			μs
			IM02 = 1	10			μs
		INT1, 2, 4		10			μs
		KR0 to KR3		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC) and the processor clock control register (PCC). The figure at the right indicates the cycle time t_{CY} versus supply voltage V_{DD} characteristic with the main system clock operating.

2. $2t_{CY}$ or 128/fx is set by setting the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...Internal clock output): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL1}, t_{KH1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI[Note 1] setup time (to $\overline{SCK}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI[Note 1] hold time (from $\overline{SCK}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$↓→SO[Note 1] output delay time	t_{KSO1}	R_L = 1 kΩ,	V_{DD} = 2.7 to 5.5 V	0		250	ns
		C_L = 100 pF[Note 2]		0		1000	ns

Notes 1. In 2-wire serial I/O mode, read SB0 or SB1 instead.

2. R_L and C_L are the load resistance and load capacitance of the SO output lines.

2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...External clock input): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL2}, t_{KH2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI[Note 1] setup time (to $\overline{SCK}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI[Note 1] hold time (from $\overline{SCK}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$↓→SO[Note 1] output delay time	t_{KSO2}	R_L = 1 kΩ,	V_{DD} = 2.7 to 5.5 V	0		300	ns
		C_L = 100 pF[Note 2]		0		1000	ns

Notes 1. In 2-wire serial I/O mode, read SB0 or SB1 instead.

2. R_L and C_L are the load resistance and load capacitance of the SO output lines.

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD})

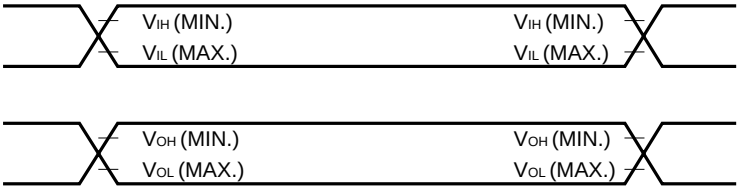
Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Absolute accuracy[Note 1]		V_{DD} = AV_{REF}	2.7 ≤ V_{DD}			1.5	LSB
			1.8 V ≤ V_{DD} < 2.7 V			3	LSB
		V_{DD} ≠ AV_{REF}				3	LSB
Conversion time[Note 2]	t_{CONV}					168/f_X	μs
Sampling time[Note 3]	t_{SAMP}					44/f_X	μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF}	V
Analog input impedance	R_{AN}				1000		MΩ
AV_{REF} current	I_{REF}				0.25	2.0	mA

Notes 1. Absolute accuracy excluding quantization error (±1/2 LSB).

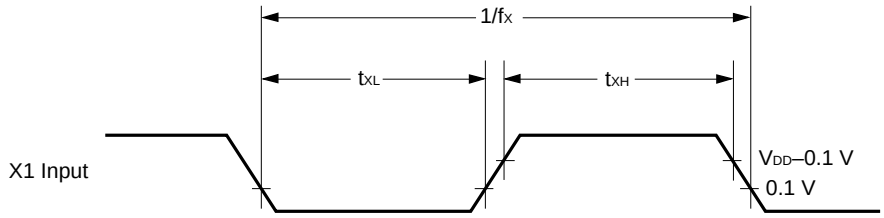
2. Time after execution of conversion start instruction until completion of conversion (EOC = 1) (40.1 μs: in f_X = 4.19 MHz operation)

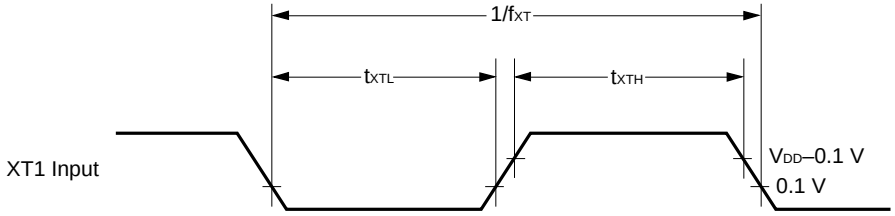
3. Time after conversion start instruction until completion of sampling (10.5 μs: in f_X = 4.19 MHz operation)

AC Timing Test Point (Excluding X1, XT1 Input)

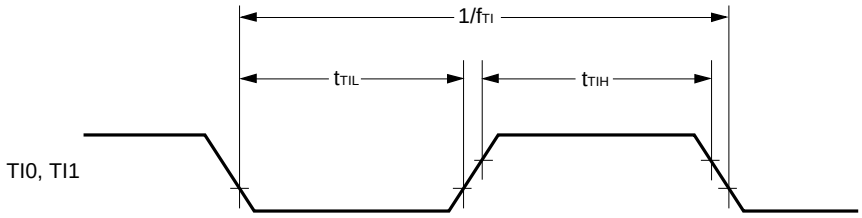


Clock Timing



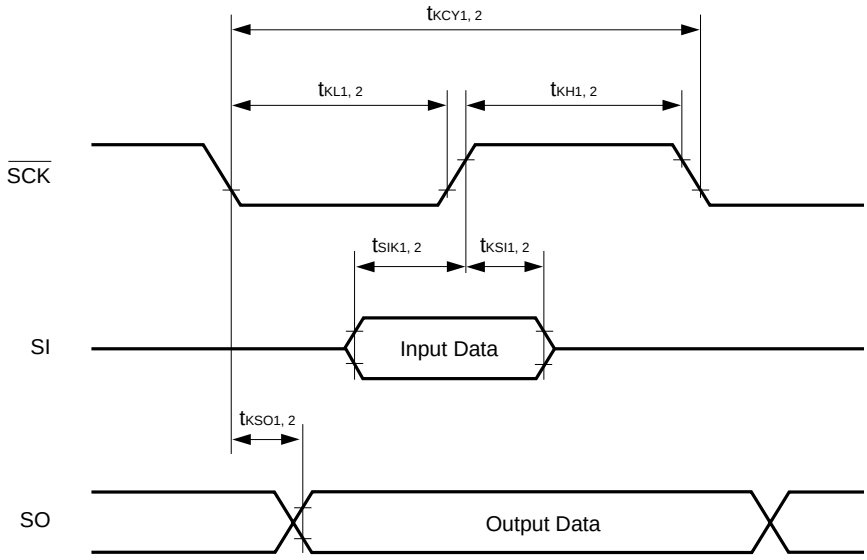


TI0, TI1 Timing

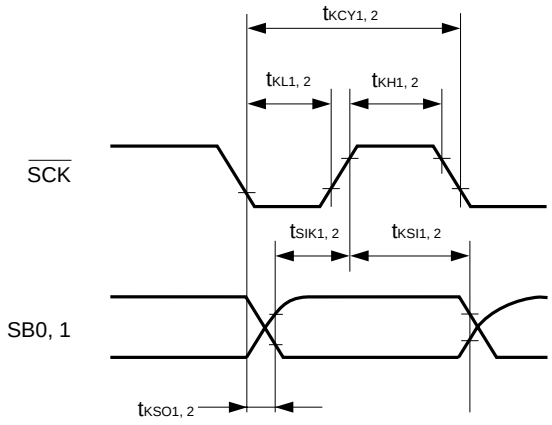


Serial Transfer Timing

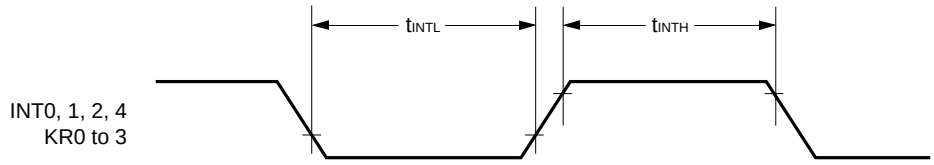
3-wire serial I/O mode



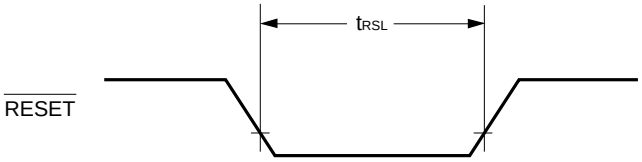
2-wire serial I/O mode



Interrupt input timing



$\overline{\text{RESET}}$ input timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

(T_A = –40 to +85°C)

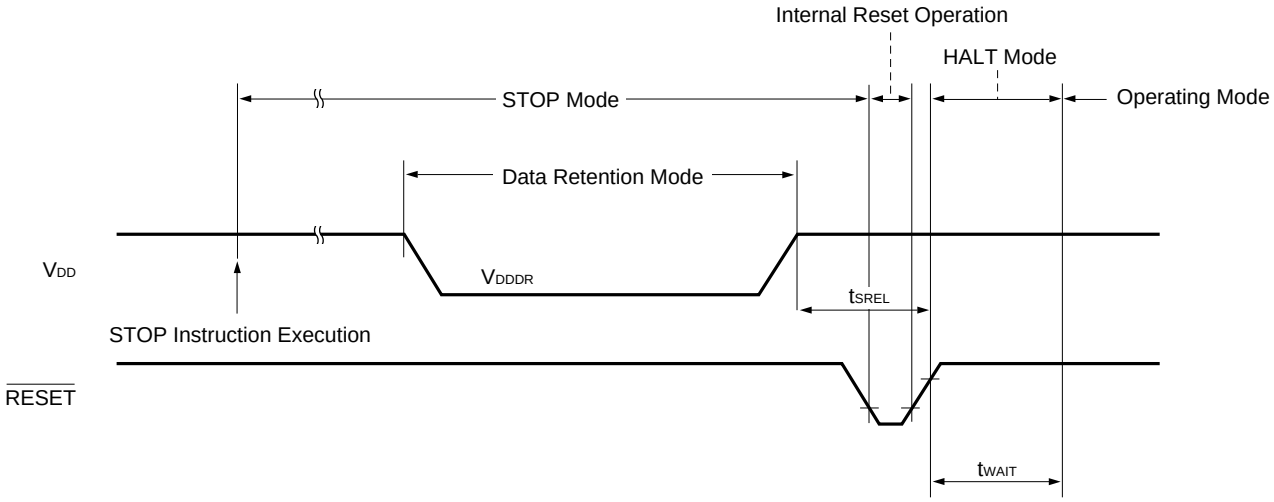
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Release by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

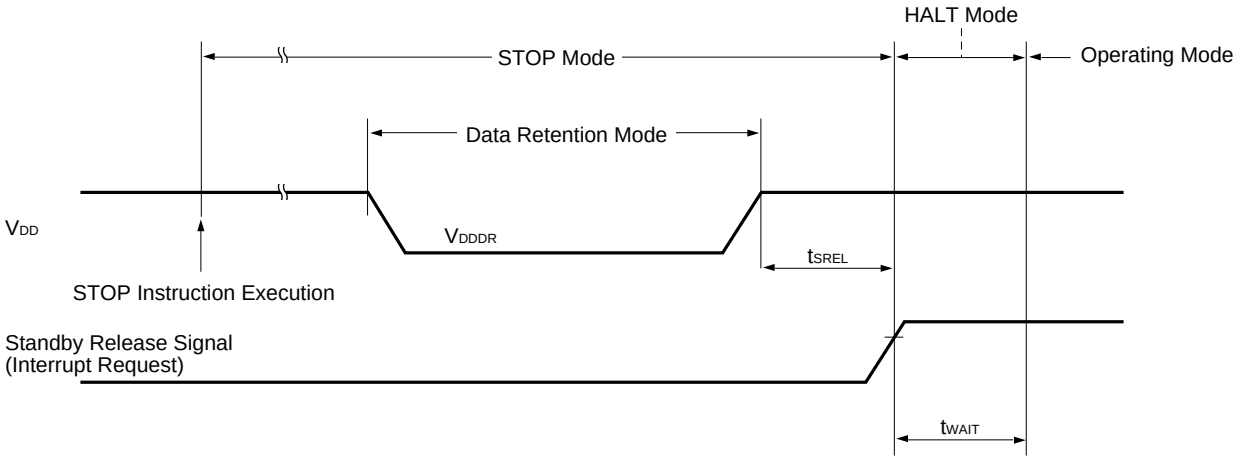
2. Depends on the basic interval timer mode register (BTM) settings (See the table below).

BTM3	BTM2	BTM1	BTM0	Wait time	
				fx = at 4.19 MHz	fx = at 6.0 MHz
—	0	0	0	2^{20}/fx (approx. 250 ms)	2^{20}/fx (approx. 175 ms)
—	0	1	1	2^{17}/fx (approx. 31.3 ms)	2^{17}/fx (approx. 21.8 ms)
—	1	0	1	2^{15}/fx (approx. 7.81 ms)	2^{15}/fx (approx. 5.46 ms)
—	1	1	1	2^{13}/fx (approx. 1.95 ms)	2^{13}/fx (approx. 1.37 ms)

Data Retention Timing (STOP Mode Release by RESET)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



DC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5°C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	Except X1, X2	0.7V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD}–0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except X1, X2	0		0.3V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD}–1.0			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Avoid exceeding +13.5 V for V_{PP} including the overshoot.

2. V_{DD} must be applied before V_{PP}, and cut after V_{PP}.

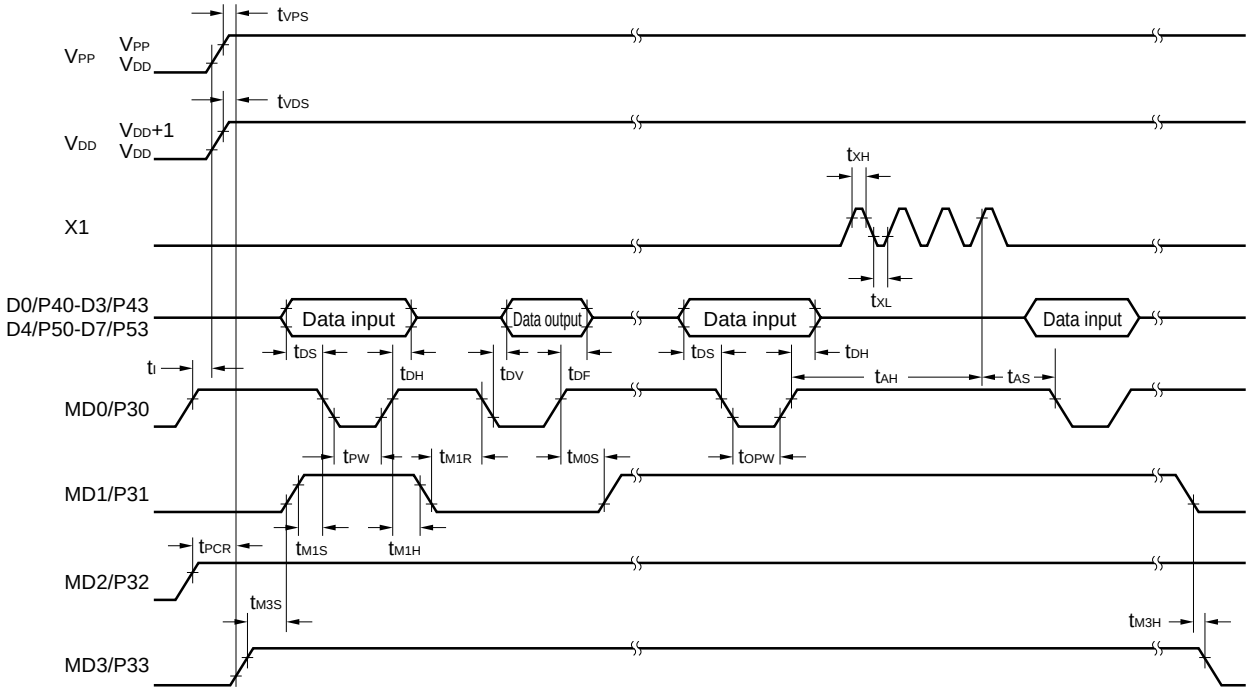
AC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5°C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	**Note 1**	Test conditions	MIN.	TYP.	MAX.	Unit
Address setup time Note 2 (to MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time Note 2 (from MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
MD0↑→data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{M0S}	t_{CES}		2			μs
MD0↓→data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (from MD0↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	–		10			μs
X1 input high-/low-level width	t_{XH}, t_{XL}	–		0.125			μs
X1 input frequency	f_X	–				4.19	MHz
Initial mode set time	t_I	–		2			μs
MD3 setup time (to MD1↑)	t_{M3S}	–		2			μs
MD3 hold time (from MD1↓)	t_{M3H}	–		2			μs
MD3 setup time (to MD0↓)	t_{M3SR}	–	During program memory read	2			μs
Address Note 2 →data output delay time	t_{DAD}	t_{ACC}	During program memory read			2	μs
Address Note 2 →data output hold time	t_{HAD}	t_{OH}	During program memory read	0		130	ns
MD3 hold time (from MD0↑)	t_{M3HR}	–	During program memory read	2			μs
MD3↓→data output float delay time	t_{DFR}	–	During program memory read			2	μs

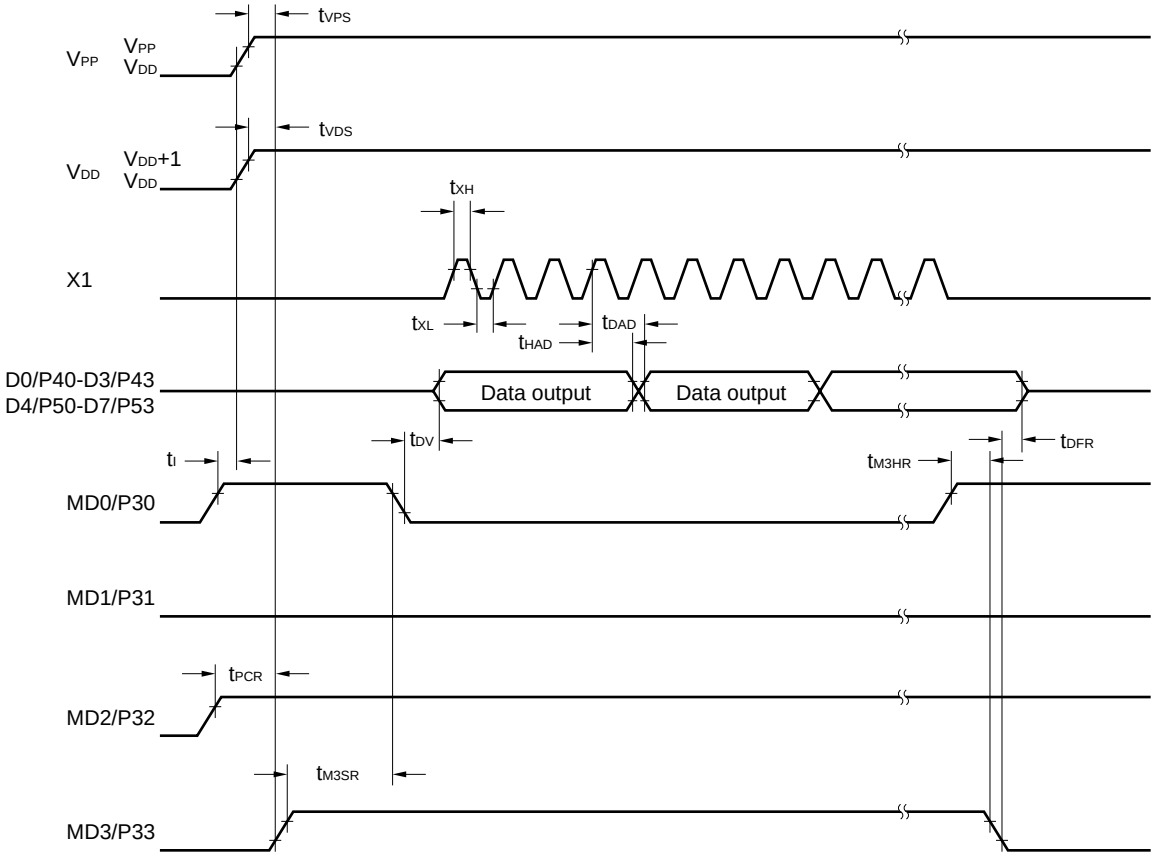
Notes1. Corresponding symbol of μPD27C256A

2. The internal address signal is incremented by 1 at the rising edge of the fourth X1 input and is not connected to the pin.

Program Memory Write Timing

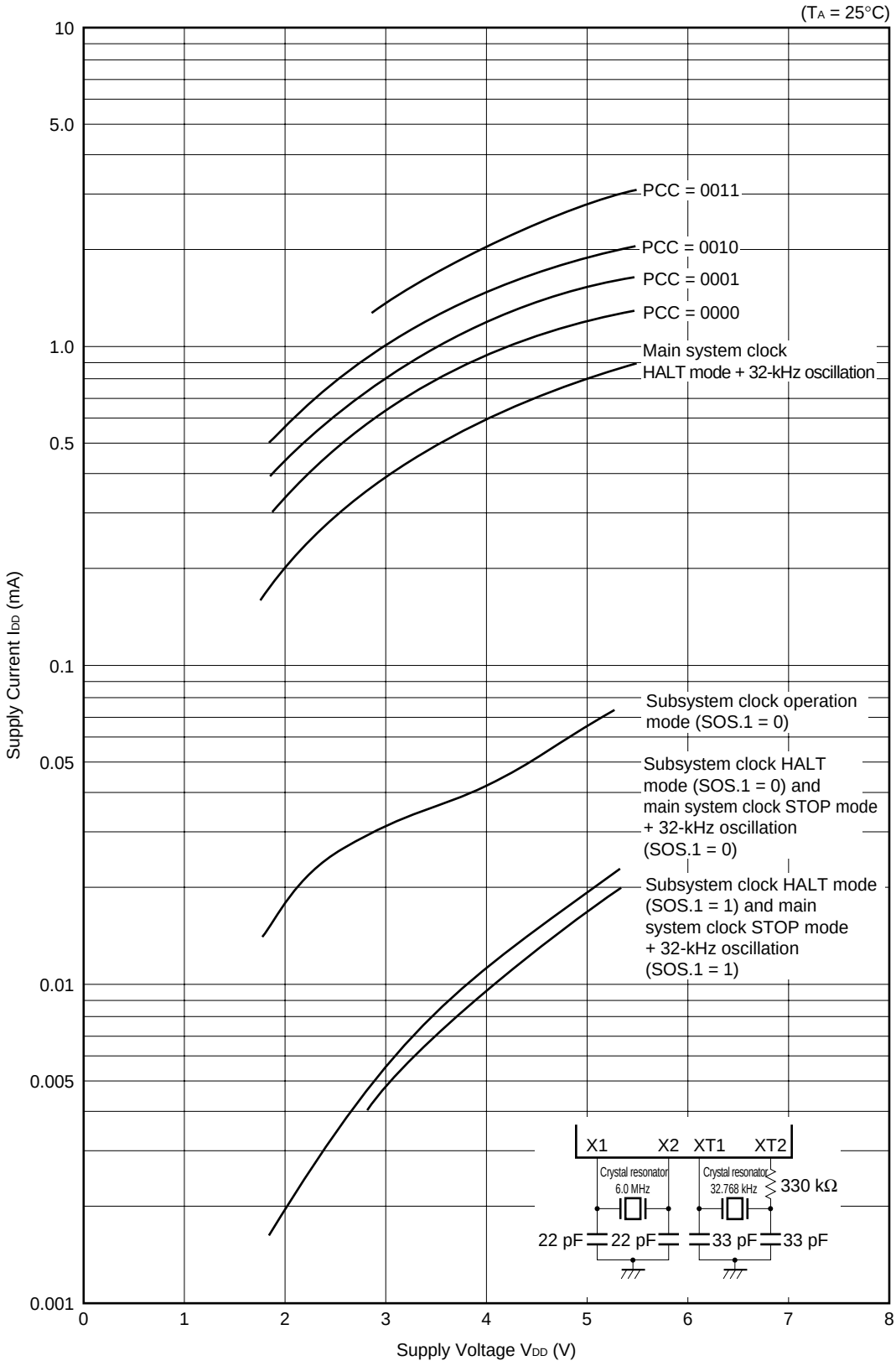


Program Memory Read Timing

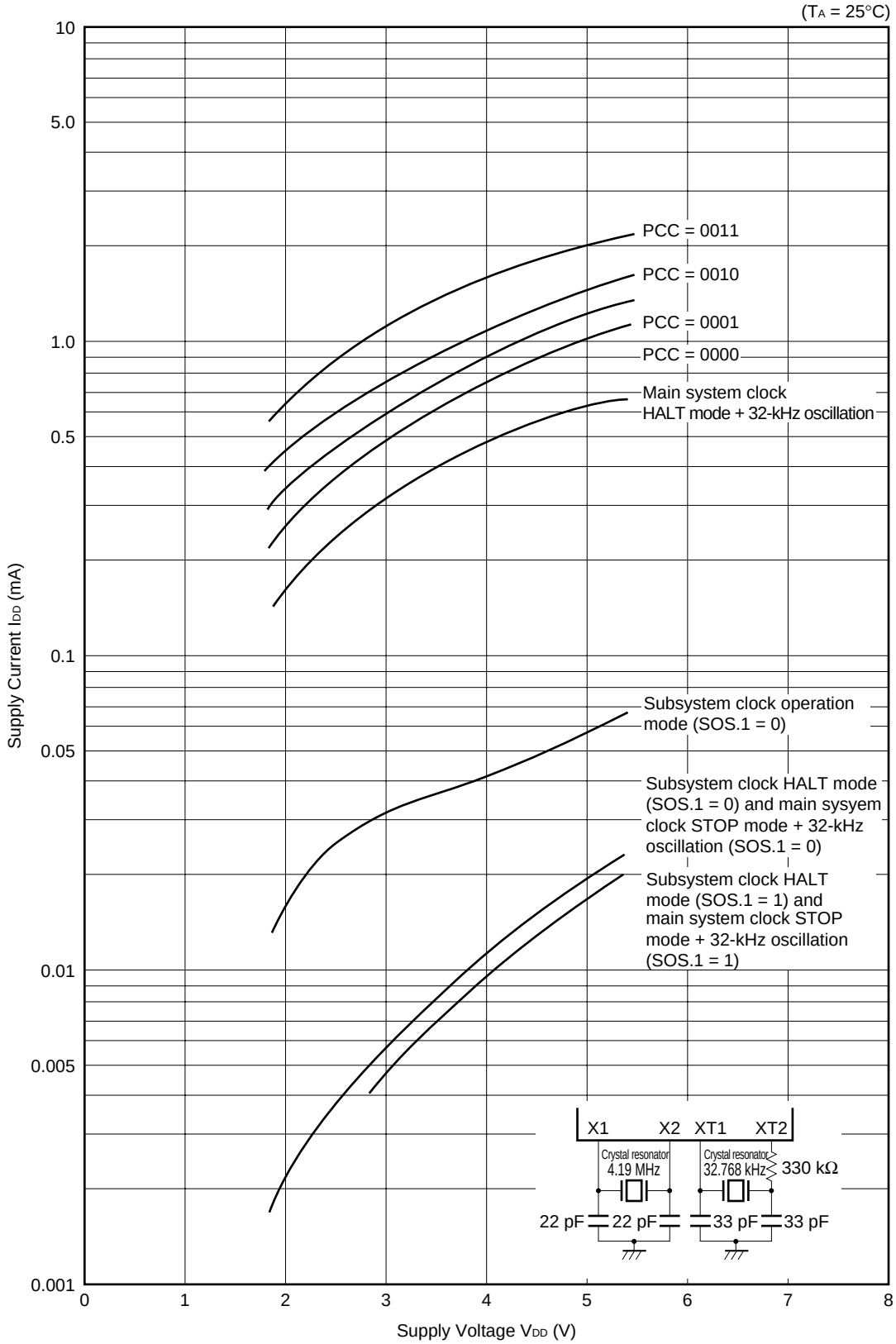


10. CHARACTERISTICS CURVES (REFERENCE VALUES)

I_{DD} vs V_{DD} (Main System Clock: 6.0-MHz Crystal Resonator)

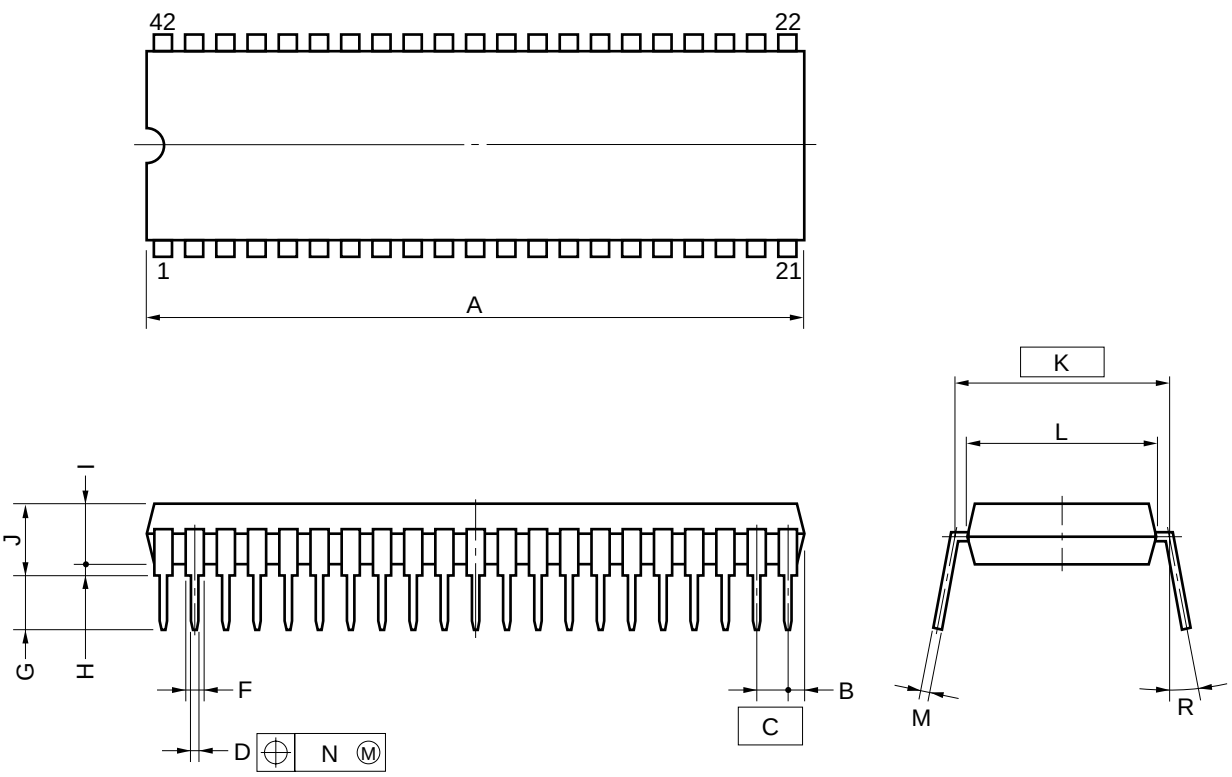


I_{DD} vs V_{DD} (Main System Clock: 4.19-MHz Crystal Resonator)



11. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

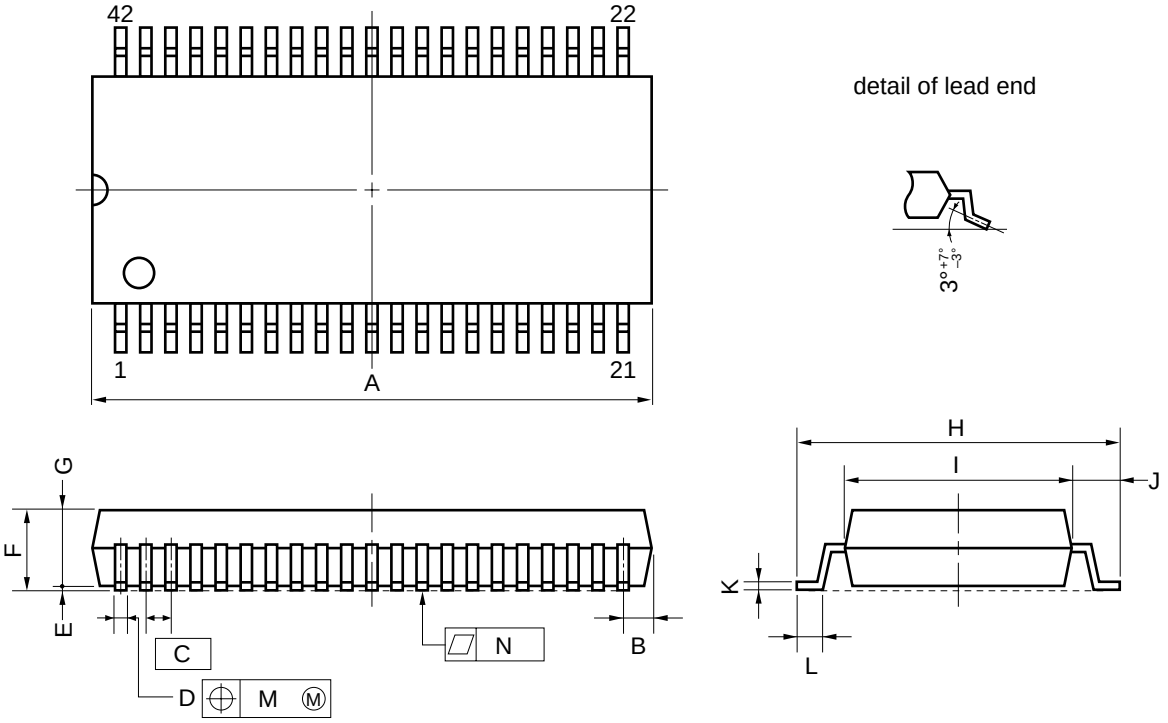
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

42 PIN PLASTIC SHRINK SOP (375 mil)



S42GT-80-375B-1

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.16 MAX.	0.715 MAX.
B	1.13 MAX.	0.044 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	$0.35^{+0.10}_{-0.05}$	$0.014^{+0.004}_{-0.003}$
E	0.125±0.075	0.005±0.003
F	2.9 MAX.	0.115 MAX.
G	2.5±0.2	$0.098^{+0.009}_{-0.008}$
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.15±0.2	$0.281^{+0.009}_{-0.008}$
J	1.6±0.2	0.063±0.008
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.10	0.004
N	0.10	0.004

★ 12. RECOMMENDED SOLDERING CONDITIONS

The μPD75P0076 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC Sales representative.

Table 12-1. Surface Mounting Type Soldering Conditions

μPD75P0076GT: 42-pin plastic shrink SOP (375 mil, 0.8 mm pitch)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds or less (at 210°C or higher), Number of reflow processes: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds or less (at 200°C or higher), Number of reflow processes: Twice or less	VP15-00-2
Wave soldering	Solder temperature: 260°C or below, Time: 10 seconds or less, Number of flow process: 1, Preheating temperature: 120°C or below (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or below, Time : 3 seconds or less (per device side)	—

Caution Use of more than one soldering method should be avoided (except for partial heating).

Table 12-2. Insertion Type Soldering Conditions

μPD75P0076CU: 42-pin plastic shrink DIP (600 mil, 1.778 mm pitch)

Soldering Method	Soldering Conditions
Wave soldering (pins only)	Solder bath temperature: 260 °C or less, Time: 10 seconds or less
Partial heating	Pin temperature: 300 °C or below, Time: 3 seconds or less (per device side)

Caution Ensure that the application of wave soldering is limited to the pins and no solder touches the main unit directly.

APPENDIX A DIFFERENCES AMONG μPD75068, 750068 AND 75P0076

Parameter		μPD75068	μPD750068	μPD75P0076
Program memory		Mask ROM 0000H to 1F7FH (8064 x 8 bits)	Mask ROM 0000H to 1FFFH (8192 x 8 bits)	One-time PROM 0000H to 3FFFH (16384 x 8 bits)
Data memory		000H to 1FFH (512 x 4 bits)		
CPU		75X Standard CPU	75XL CPU	
General-purpose register		4 bits x 8 or 8 bits x 4	(4 bits x 8 or 8 bits x 4) x 4 banks	
Instruction execution time	When main system clock is selected	0.95, 1.91, 15.3 μs (during 4.19-MHz operation)	• 0.67, 1.33, 2.67, 10.7 μs (during 6.0-MHz operation) • 0.95, 1.91, 3.81, 15.3 μs (during 4.19-MHz operation)	
	When subsystem clock is selected	122 μs (during 32.768-kHz operation)		
I/O port	CMOS input	12 (Connections of on-chip pull-up resistor specified by software: 7)		
	CMOS input/output	12 (Connections of on-chip pull-up resistor specified by software)		
★	N-ch open-drain input/output	8 (on-chip pull-up resistor specified by mask option) Withstand voltage is 10 V	8 (on-chip pull-up resistor specified by mask option) Withstand voltage is 13 V	8 (no mask option) Withstand voltage is 13 V
	Total	32		
Timer		3 channels • 8-bit timer/event counter • 8-bit basic interval timer • Watch timer	4 channels • 8-bit timer/event counter 0 (watch timer output added) • 8-bit timer/event counter 1 (can be used as a 16-bit timer/event counter) • 8-bit basic interval timer/watchdog timer • Watch timer	
A/D converter		• 8-bit resolution x 8 channels (successive approximation) • Can operate at the voltage from V_{DD} = 2.7 V	• 8-bit resolution x 8 channels (successive approximation) • Can operate at the voltage from V_{DD} = 1.8 V	
★ ★	Clock output (PCL)	Φ, 524, 262, 65.5 kHz (Main system clock: during 4.19-MHz operation)	• Φ, 1.05 MHz, 262 kHz, 65.5 kHz (Main system clock: during 4.19-MHz operation) • Φ, 1.5 MHz, 375 kHz, 93.8 kHz (Main system clock: during 6.0-MHz operation)	
Buzzer output (BUZ)		2, 4, 32 kHz (Main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation)	• 2, 4, 32 kHz (Main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation) • 2.93, 5.86, 46.9 kHz (Main system clock: during 6.0-MHz operation)	
Serial interface		3 modes supported • 3-wire serial I/O mode ...MSB/LSB first selectable • 2-wire serial I/O mode • SBI mode	2 modes supported • 3-wire serial I/O mode...MSB/LSB first selectable • 2-wire serial I/O mode	
Vectored interrupt		3 external, 3 internal	3 external, 4 internal	
Test inputs		1 external, 1 internal		
Power supply voltage		V_{DD} = 2.7 to 6.0 V	V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85 °C		
Package		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 x 10 mm)	• 42-pin plastic shrink DIP (600 mil, 1.778-mm pitch) • 42-pin plastic shrink SOP (375 mil, 0.8-mm pitch)	

Note Under development

APPENDIX B DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD75P0076. In the 75XL series, the common relocatable assembler of the series is used together with device files according to the product.

RA75X relocatable assembler	Host machine			Order code (Part No.)
		OS	Supply Medium	
★	PC-9800 Series	MS-DOS™ (Ver.3.30 to Ver.6.2[Note])	3.5" 2HD	μS5A13RA75X
			5" 2HD	μS5A10RA75X
	IBM PC/AT™ or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13RA75X
			5" 2HC	μS7B10RA75X

Device file	Host machine			Order code (Part No.)
		OS	Supply Medium	
★	PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note])	3.5" 2HD	μS5A13DF750068
			5" 2HD	μS5A10DF750068
	IBM PC/AT or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13DF750068
			5" 2HC	μS7B10DF750068

Note Ver. 5.00 or later include a task swapping function, but this software is not able to use that function.

Remark Operation of the assembler and device file is guaranteed only when using the host machine and OS described above.

PROM Write Tools

Hardware	PG-1500	This is a PROM programmer which enables you to program a single-chip microcontroller with on-chip PROM by stand-alone or host machine operation by connecting an attached board and a programmer adapter (sold separately). In addition, typical PROMs in capacities ranging from 256 K to 4 M bits can be programmed.		
	PA-75P0076CU	This is a PROM programmer adapter dedicated for the μPD75P0076CU and 75P0076GT. It can be used when connected to a PG-1500.		
Software	PG-1500 controller	PG-1500 and a host machine are connected by serial and parallel interfaces and PG-1500 is controlled on the host machine.		
		Host machine		Order code (Part No.)
		OS	Supply medium	
★		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note])	3.5" 2HD	μS5A13PG1500
				5" 2HD	μS5A10PG1500
		IBM PC/AT or compatible	Refer to **OS for IBM PCs**	3.5" 2HD	μS7B13PG1500
				5" 2HC	μS7B10PG1500

Note Ver. 5.00 or later include a task swapping function, but this software is not able to use that function.

Remark Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

Debugging Tools

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the μPD75P0076.

Various system configurations using these in-circuit emulators are listed below.

Hardware	IE-75000-R[Note 1]	The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems that use 75X or 75XL Series products. For development of the μPD750068 subseries, the IE-75000-R is used with a separately sold emulation board (IE-75300-R-EM) and emulation probe. These products can be applied for highly efficient debugging when connected to a host machine and PROM programmer. The IE-75000-R can include a connected emulation board (IE-75000-R-EM).			
	IE-75001-R	The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems that use 75X or 75XL Series products. The IE-75001-R is used with a separately sold emulation board (IE-75300-R-EM) and emulation probe. These products can be applied for highly efficient debugging when connected to a host machine and PROM programmer.			
	IE-75300-R-EM	This is an emulation board for evaluating application systems that use the μPD750068 subseries. It is used in combination with the IE-75000-R or IE-75001-R in-circuit emulator.			
	EP-750068CU-R	This is an emulation probe for the μPD75P0076CU. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.			
	EP-750068GT-R EV-9500GT-42	This is an emulation probe for the μPD75P0076GT. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM. It includes a flexible board (EV-9500GT-42) to facilitate connections with target systems.			
Software	IE control program	This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232-C or Centronics interface.			
		Host machine			Order code (Part No.)
			OS	Supply Medium	
		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note 2])	3.5" 2HD	μS5A13IE75X
★				5" 2HD	μS5A10IE75X
		IBM PC/AT or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13IE75X
				5" 2HC	μS7B10IE75X

Notes 1. This is a service part provided for maintenance purpose only.

2. Ver. 5.00 or later include a task swapping function, but this software is not able to use that function.

Remarks 1. Operation of the IE control program is guaranteed only when using the host machine and OS described above.

2. The generic name for the μPD750064, 750066, 750068, and 75P0076 is the μPD750068 subseries.

OS for IBM PCs

The following operating systems for the IBM PC are supported.

OS	Version
★ PC DOS™	Ver.5.02 to Ver.6.3 J6.1/V[Note] to J6.3/V[Note]
★ MS-DOS	Ver.5.0 to Ver.6.22 5.0/V[Note] to 6.2/V[Note]
IBM DOS™	J5.02/V[Note]

Note Only the English mode is supported.

Caution Ver 5.0 and above include a task swapping function, but this software is not able to use that function.

★ APPENDIX C RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to device

Document Name	Document No.	
	English	Japanese
μPD750064, 750066, 750068, 750064(A), 750066(A), 750068(A) Data Sheet	U10165E[Note]	U10165J
μPD75P0076 Data Sheet	This document	U10232J
μPD750068 User's Manual	U10670E	U10670J
μPD750068 Instruction Table	—	IEM-5606
75XL Series Selection Guide	U10453E	U10453J

Note Preliminary product information

Documents related to development tool

Document Name			Document No.	
			English	Japanese
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1416	EEU-846
	IE-75300-R-EM User's Manual		U11345E	U11354J
	EP-750068GT-R User's Manual		U10950E	U10950J
	PG-1500 User's Manual		EEU-1335	EEU-651
Software	RA75X Assembler Package User's Manual	Operation	EEU-1346	EEU-731
		Language	EEU-1363	EEU-730
	PG-1500 Controller User's Manual	PC-9800 Series (MS-DOS) base	EEU-1291	EEU-704
		IBM PC Series (PC DOS) base	U10540E	EEU-5008

Other related documents

Document Name	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
NEC Semiconductor Device Quality Grades	C11531E	C11531J
NEC Semiconductor Device Reliability and Quality Control	C10983E	C10983J
Electrostatic Discharge (ESD) Test	—	MEM-539
Semiconductor Device Quality Assurance Guide	MEI-1202	MEI-603
Microcontroller-related Product Guide —Third Party Products—	—	U11416J

Caution The contents of the documents listed above are subject to change without prior notice to users. Make sure to use the latest edition when starting design.

[MEMO]

NOTES FOR CMOS DEVICES

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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