CS8361

5V Dual Micropower Low Dropout Regulator with $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$

Description

The CS8361 is a precision micropower dual voltage regulator with $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$.

The 5V standby output is accurate within ±2% while supplying loads of 100mA and has a typical dropout voltage of 400mV. Quiescent current is low, typically 140µA with a 300µA load. The active $\overline{\text{RESET}}$ output monitors the 5V standby output and holds the $\overline{\text{RESET}}$ line low during power-up and regulator dropout conditions. The $\overline{\text{RESET}}$ circuit includes hysteresis and is guaranteed to operate correctly with 1V on the standby output.

The second output tracks the 5V standby output through an external adjust lead, and can supply loads of 250mA with a typical dropout voltage of 400mV. The logic level $\overline{\text{ENABLE}}$ lead is used to control this tracking regulator output.

Both outputs are protected against overvoltage, short circuit, reverse battery and overtemperature conditions. The robustness and low quiescent current of the CS8361 makes it not only well suited for automotive microprocessor applications, but for any battery powered microprocessor applications.

Features

- **2 Regulated Outputs**
  Standby Output 5V ±2%; 100mA
  Tracking Output 5V; 250mA

- **Low Dropout Voltage (0.4V at rated current)**

- **RESET Option**

- **ENABLE Option**

- **Low Quiescent Current**

- **Protection Features**
  Independent Thermal Shutdown
  Short Circuit
  60V Load Dump
  Reverse Battery

Package Options

16 Lead PDIP & SOIC Wide
(internally fused leads)

V_{IN} 1		V_{STBY}
NC		NC
V_{TRK}		NC
Gnd		Gnd
Gnd		Gnd
Adj		NC
NC		NC
$\overline{\text{ENABLE}}$		$\overline{\text{RESET}}$

7L TO-220   **7L D²PAK**

1. V_{STBY}
2. V_{IN}
3. V_{TRK}
4. Gnd
5. Adj
6. $\overline{\text{ENABLE}}$
7. $\overline{\text{RESET}}$
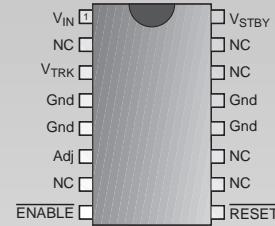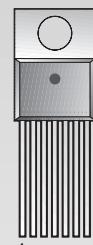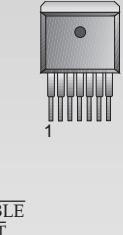
Also available in 20 Lead SOIC Wide. Consult factory for 20 Lead PSOP .

Block Diagram

V_{IN} — Overvoltage Shutdown — OVSD — Current Limit — Bandgap — BG — BG — TSD — OVSD — V_{STBY} 5V,100mA,2% — RESET — V_{TRK} 250mA — Thermal Shutdown — TSD — Current Limit — Adj — $V_{STANDBY}$ — TSD — OVSD — $\overline{\text{ENABLE}}$ — BG — Gnd — RESET — $\overline{\text{RESET}}$

* Consult factory for positive ENABLE option.

Absolute Maximum Ratings

Supply Voltage, V_{IN} ....-16V to 26V

Positive Transient Input Voltage, tr > 1ms..60V

Negative Transient Input Voltage, T < 100ms, 1% Duty Cycle..-50V

Input Voltage Range ($\overline{ENABLE}$, $\overline{RESET}$) ....-0.3V to 10V

Junction Temperature..-40°C to +150°C

Storage Temperature Range ....-55°C to +150°C

ESD Susceptibility (Human Body Model)..2kV

Lead Temperature Soldering
    Wave Solder (through hole styles only) ....10 sec. max, 260°C peak
    Reflow (SMD styles only) ....60 sec. max above 183°C, 230°C peak

Electrical Characteristics: $6V \leq V_{IN} \leq 26V$, $I_{OUT1} = I_{OUT2} = 100\mu A$, $-40°C \leq T_A \leq +125°C$, $-40°C \leq T_J \leq +150°C$, unless otherwise specified.					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **Tracking Output (V_{TRK})**					
$V_{STBY} - V_{TRK}$, V_{TRK} Tracking Error	$6V \leq V_{IN} \leq 26V$ $100\mu A \leq I_{TRK} \leq 250mA$ (note 1)	-25		+25	mV
Adjust Pin Current, I_{Adj}	Loop in Regulation		1.5	5	μA
Line Regulation	$6V \leq V_{IN} \leq 26V$ (note 1)		5	50	mV
Load Regulation	$100\mu A \leq I_{TRK} \leq 250mA$ (note 1)		5	50	mV
Dropout Voltage ($V_{IN} - V_{TRK}$)	$I_{TRK} = 100\mu A$ $I_{TRK} = 250mA$		100 400	150 700	mV mV
Current Limit	$V_{IN} = 12V$, $V_{TRK} = 4.5$	275	500		mA
Quiescent Current	$V_{IN} = 12V$, $I_{TRK} = 250mA$ No Load on V_{STBY}		25	50	mA
Reverse Current	$V_{TRK} = 5V$, $V_{IN} = 0V$		200	1500	μA
Ripple Rejection	$f = 120Hz$, $I_{TRK} = 250mA$ $7V \leq V_{IN} \leq 17V$	60	70		dB
■ **Standby Output (V_{STBY})**					
Output Voltage, V_{STBY}	$6V \leq V_{IN} \leq 26V$ $100\mu A \leq I_{STBY} \leq 100mA$	4.90	5.00	5.10	V
Line Regulation	$6V \leq V_{IN} \leq 26V$		5	50	mV
Load Regulation	$100\mu A \leq I_{STBY} \leq 100mA$		5	50	mV
Dropout Voltage ($V_{IN} - V_{STBY}$)	$I_{STBY} = 100\mu A$ $I_{STBY} = 100mA$		100 400	150 600	mV mV
Current Limit	$V_{IN} = 12V$, $V_{STBY} = 4.5V$	125	200		mA
Short Circuit Current	$V_{IN} = 12V$, $V_{STBY} = 0V$	10	100		mA
Quiescent Current	$V_{IN} = 12V$, $I_{STBY} = 100mA$ $I_{TRK} = 0mA$		10	20	mA
	$V_{IN} = 12V$, $I_{STBY} = 300\mu A$ $I_{TRK} = 0mA$		140	200	μA
Reverse Current	$V_{STBY} = 5V$, $V_{IN} = 0V$		100	200	μA
Ripple Rejection	$f = 120Hz$, $I_{STBY} = 100mA$ $7V \leq V_{IN} \leq 17V$	60	70		dB

Note 1: V_{TRK} connected to Adj lead. V_{TRK} can be set to higher values by using an external resistor divider.

Electrical Characteristics: 6V ≤ V$_{IN}$ ≤ 26V, I$_{OUT1}$ = I$_{OUT2}$ = 100μA, -40°C ≤ T$_A$ ≤+125°C, -40°C ≤T$_J$ ≤ +150°C, unless otherwise specified.					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ **RESET ENABLE Functions**					
$\overline{\text{ENABLE}}$ Input Threshold		0.8	1.2	2.0	V
$\overline{\text{ENABLE}}$ Input Bias Current	V$_{ENABLE}$ = 0V to 10V	-10	0	10	μA
$\overline{\text{RESET}}$ Threshold High (V$_{RH}$)	V$_{STBY}$ Increasing	4.59	4.87	V$_{STBY}$-0.02	V
$\overline{\text{RESET}}$ Hysteresis		60	120	180	mV
$\overline{\text{RESET}}$ Threshold Low (V$_{RL}$)	V$_{STBY}$ Decreasing	4.53	4.75	V$_{STBY}$-0.08	V
$\overline{\text{RESET}}$ Leakage				25	μA
Output Voltage					
Low (V$_{RLO}$); R$_{RST}$ = 10kΩ	1V ≤ VS$_{TBY}$ ≤ V$_{RL}$		0.1	0.4	V
Low (V$_{RPEAK}$)	V$_{STBY}$, Power Up, Power Down		0.6	1.0	V
■ **Protection Circuitry (Both Outputs)**					
Independent Thermal Shutdown	V$_{STBY}$	150	180		°C
	V$_{TRK}$	150	165		°C
Overvoltage Shutdown		30	34	38	V

Package Lead Description					
PACKAGE LEAD #				LEAD SYMBOL	FUNCTION
7L TO-220	**7L D²PAK**	**16L PDIP & SO Wide** *(Internally Fused Leads)*	**20L SO Wide** *(Internally Fused Leads)*		
1	1	16	20	V$_{STBY}$	Standby output voltage delivering 100mA.
2	2	1	1	V$_{IN}$	Input voltage.
3	3	3	2	V$_{TRK}$	Tracking output voltage controlled by $\overline{\text{ENABLE}}$ delivering 250mA.
4	4	4,5,12,13	4,5,6,7 14,15,16,17	Gnd	Reference ground connection.
5	5	6	8	Adj	Resistor divider from V$_{TRK}$ to Adj. Sets the output voltage on V$_{TRK}$. If tied to V$_{TRK}$, V$_{TRK}$ will track V$_{STBY}$.
6	6	8	10	$\overline{\text{ENABLE}}$	Provides on/off control of the tracking output, active LOW.
7	7	9	11	$\overline{\text{RESET}}$	CMOS compatible output lead that goes low whenever V$_{STBY}$ falls out of regulation.
		2,7,10, 11,14,15	3,9,12,13, 18,19	NC	No Connection.

Circuit Description

ENABLE Function

The $\overline{\text{ENABLE}}$ function switches the output transistor for V_{TRK} on and off. When the $\overline{\text{ENABLE}}$ lead voltage exceeds 1.4V(typ), V_{TRK} turns off. This input has several hundred millivolts of hysteresis to prevent spurious output activity during power-up or power-down.

RESET Function

The $\overline{\text{RESET}}$ is an open collector NPN transistor, controlled by a low voltage detection circuit sensing the V_{STBY} (5V) output voltage. This circuit guarantees the $\overline{\text{RESET}}$ output stays below 1V (0.1V typ) when V_{STBY} is as low as 1V to ensure reliable operation of microprocessor-based systems.

V_TRK Output Voltage

This output uses the same type of output device as V_{STBY}, but is rated for 250mA. The output is configured as a tracking regulator of the standby output. By using the standby output as a voltage reference, giving the user an external programming lead (Adj lead), output voltages from 5V to 20V are easily realized. The programming is done with a simple resistor divider (Figure 2), and following the formula:

$$V_{TRK} = V_{STBY} \times (1 + R1/R2) + I_{Adj} \times R1$$

If another 5V output is needed, simply connect the Adj lead to the V_{TRK} output lead.

Application Notes

External Capacitors

Output capacitors for the CS8361 are required for stability. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to -40°C, capacitors rated at that temperature must be used.

More information on capacitor selection for Smart Regulators™ is available in the Smart Regulator application note, "Compensation for Linear Regulators."

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 1) is:

PD(max) = {V_{IN}(max)–V_{OUT1}(min)}I_{OUT1}(max)+
{V_{IN}(max)–V_{OUT2}(min)}I_{OUT2}(max)+V_{IN}(max)IQ   (1)

Where

V_{IN}(max) is the maximum input voltage,

V_{OUT1}(min) is the minimum output voltage from V_{OUT1},

V_{OUT2}(min) is the minimum output voltage from V_{OUT2},

I_{OUT1}(max) is the maximum output current, for the application

I_{OUT2}(max) is the maximum output current, for the application

I_Q is the quiescent current the regulator consumes at I_{OUT}(max).

Once the value of PD(max) is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.
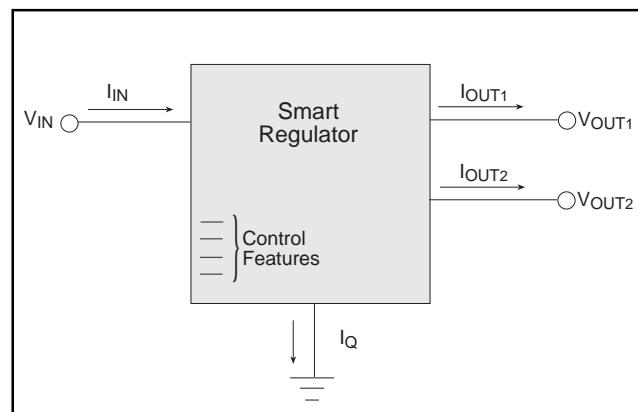

Figure 1: Dual output regulator with key performance parameters labeled.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \qquad (3)$$

where:
$R_{\Theta JC}$ = the junction–to–case thermal resistance,
$R_{\Theta CS}$ = the case–to–heat sink thermal resistance, and
$R_{\Theta SA}$ = the heat sink–to–ambient thermal resistance.

$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

Test & Application Circuits
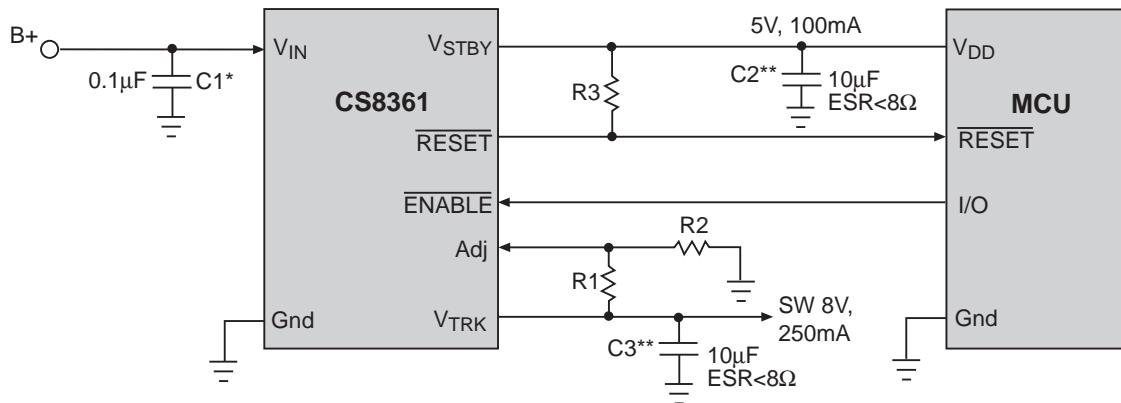
$V_{TRK} \sim V_{STBY} (1 + R1/R2)$
For $V_{TRK} \sim 8V$, R1/R2 ~ 0.6

 * C1 is required if regulator is located far from power supply filter.
** C2 and C3 are required for stability.

Figure 2: 5V, 8V Regulator
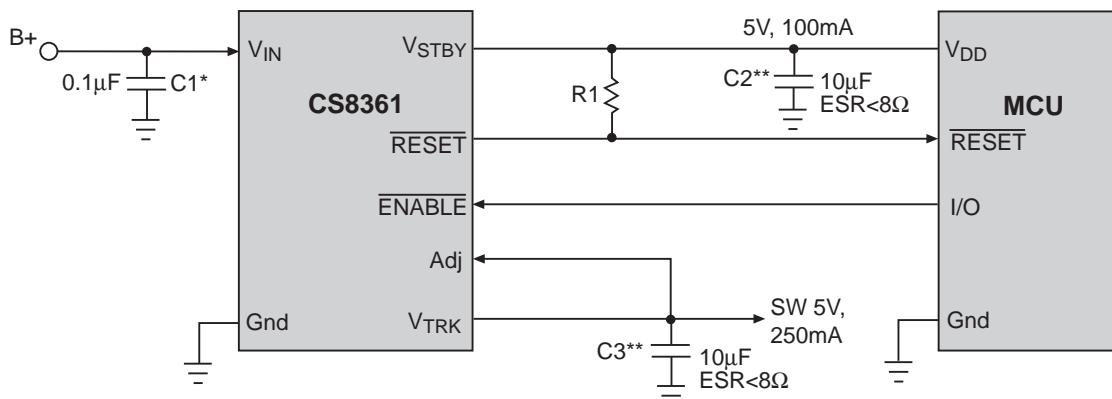
 * C1 is required if regulator is located far from power supply filter.
** C2 and C3 are required for stability.

Figure 3: Dual 5V Regulator

Package Specification

PACKAGE DIMENSIONS IN mm(INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
16L PDIP	19.69	18.67	.775	.735
16L SO Wide*	10.50	10.10	.413	.398
20L SO Wide*	13.00	12.60	.512	.496

7 Lead D²PAK (DPS)* Short-Leaded

1.68 (.066) / 1.40 (.055)
10.31 (.406) / 10.05 (.396)
1.40 (.055) / 1.14 (.045)
8.53 (.336) / 8.28 (.326)
14.71 (.579) / 13.69 (.539)
2.79 (.110) / 2.54 (.100)
1.98 (.078) / 1.47 (.058)
0.91 (.036) / 0.66 (.026)
1.27 (.050) REF
.254 (.010) REF
TERMINAL 8
6.50 (.256) REF
7.75 (.305) REF
4.57 (.180) / 4.31 (.170)
0.10 (.004) / 0.00 (.000)
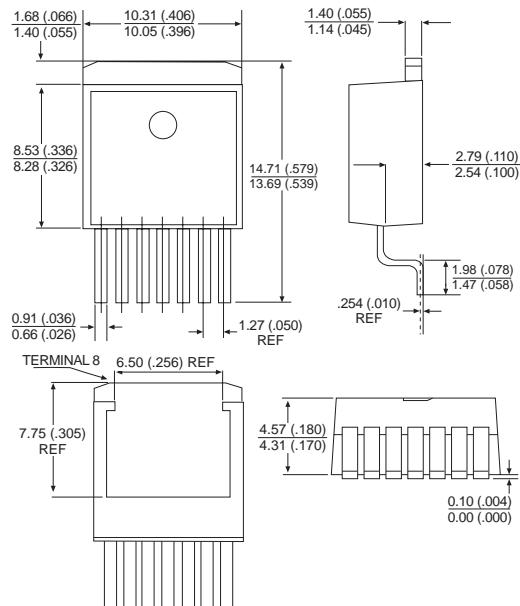
*CHERRY SEMICONDUCTOR SHORT-LEADED FOOTPRINT

Surface Mount Wide Body (DW); 300 mil wide

7.60 (.299) / 7.40 (.291)
10.65 (.419) / 10.00 (.394)
0.51 (.020) / 0.33 (.013)
1.27 (.050) BSC
2.49 (.098) / 2.24 (.088)
2.65 (.104) / 2.35 (.093)
1.27 (.050) / 0.40 (.016)
0.32 (.013) / 0.23 (.009)
0.30 (.012) / 0.10 (.004)
D

REF: JEDEC MS-013
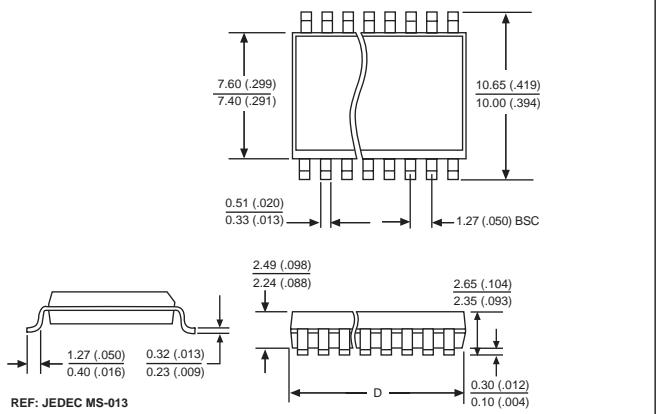
Ordering Information

Part Number	Description
CS8361YDPS7	7L D²PAK short-leaded
CS8361YDPSR7	7L D²PAK short-leaded, *(tape & reel)*
CS8361YT7	7L TO-220 (Straight)
CS8361YDWF16	16L SO Wide*
CS8361YDWFR16	16L SO Wide*, *(tape & reel)*
CS8361YN16	16L PDIP
CS8361YDW20	20L SO Wide*
CS8361YDWR20	20L SO Wide*, *(tape & reel)*

PACKAGE THERMAL DATA

Thermal Data	typ	$R_{\Theta JA}$	$R_{\Theta JC}$	˚C/W
7L D²PAK		10-50**	3.5	
7L TO-220		50	3.5	
16L PDIP		80	42	
16L SO Wide*		75	18	
20L SO Wide*		55	9	

** *Depending on thermal properties of substrate.* $R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$

7 Lead TO-220 (T) Straight

10.54 (.415) / 9.78 (.385)
2.87 (.113) / 2.62 (.103)
6.55 (.258) / 5.94 (.234)
3.96 (.156) / 3.71 (.146)
14.22 (.560) / 13.72 (.540)
0.94 (.037) / 0.58 (.023)
1.40 (.055) / 1.14 (.045)
0.64 (.025) / 0.38 (.015)
7.75 (.305) / 7.49 (.295)
4.83 (.190) / 4.06 (.160)
1.40 (.055) / 1.14 (.045)
14.99 (.590) / 14.22 (.560)
0.56 (.022) / 0.36 (.014)
2.92 (.115) / 2.29 (.090)
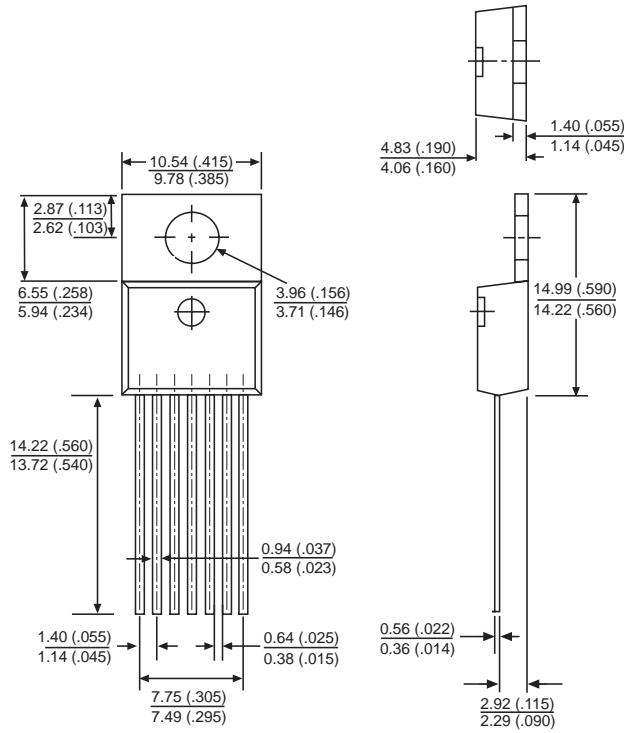
Plastic DIP (N); 300 mil wide

7.11 (.280) / 6.10 (.240)
1.77 (.070) / 1.14 (.045)
2.54 (.100) BSC
8.26 (.325) / 7.62 (.300)
3.68 (.145) / 2.92 (.115)
.356 (.014) / .203 (.008)
0.39 (.015) MIN.
.558 (.022) / .356 (.014)
D
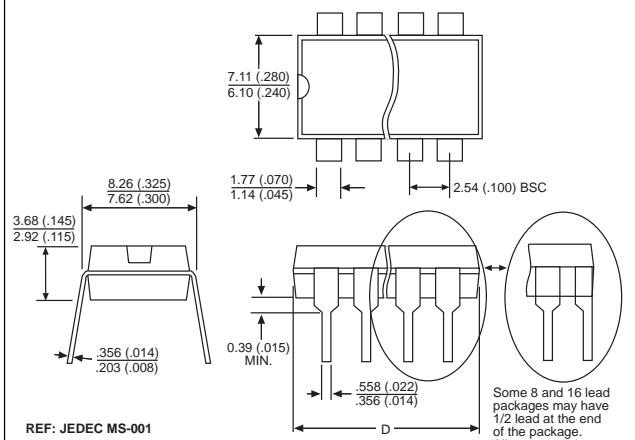
Some 8 and 16 lead packages may have 1/2 lead at the end of the package. All specs are the same.

REF: JEDEC MS-001

* Internally Fused Leads

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