SGS-THOMSON MICROELECTRONICS

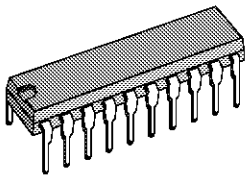
L6213

SOLENOID DRIVER + SWITCH MODE POWER SUPPLY

ADVANCE DATA

- OPERATING SUPPLY VOLTAGE UP TO 46V
- 1A POWER SUPPLY (5V)
- 5A SOLENOID DRIVER
- PRECISE ON CHIP REFERENCE VOLTAGE
- DISCONTINUOUS MODE - FREQUENCY VARIABLE
- VERY HIGH EFFICIENCY
- 1Ω OUTPUT DMOS (SMPS)
- INTERNAL CURRENT LIMIT (SMPS SECTION)
- EXTERNALLY PROGRAMMABLE SOLENOID CURRENT RISING SLOPE
- EXTERNALLY PROGRAMMABLE FIXED HYSTERESIS CONTROL
- OPTIMIZED DMOS $R_{DS\ ON}$ FOR HIGH SIDE CHOPPING

MULTIPOWER BCD TECHNOLOGY



Powerdip 16+2+2

DESCRIPTION

The L6213 is an IC containing a S.M.P.S. delivering 1A at a voltage of 5V and a section designed to drive a solenoid with a current up to 5A.

The device is realized in BCD mixed technology, which combines isolated DMOS power transistor with CMOS and Bipolar circuits on the same chip.

The SMPS section can deliver 1A DC with an output voltage of 5V, including current limiting, reset and power fail for microprocessor and thermal protection.

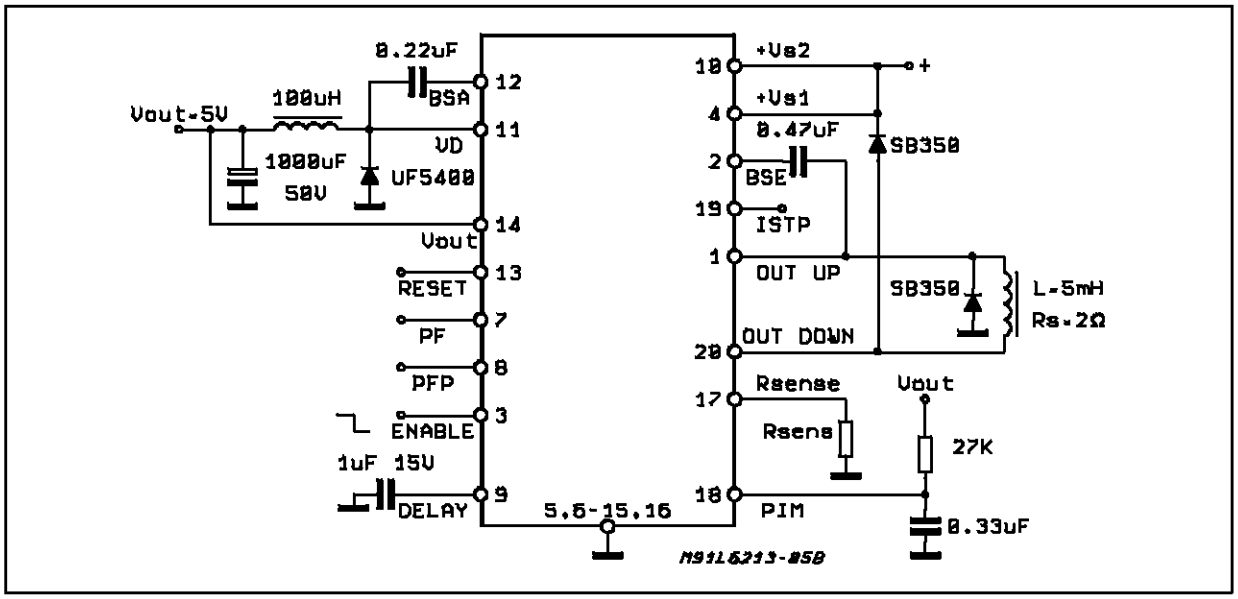
The solenoid driver section is designed for high current applications like hammer driver in electronic typewriter.

The solenoid output section contains a high side and a low side DMOS, which $R_{DS\ ON}$ are optimized for high side chopping. The current rising slope is externally programmable through an external capacitor.

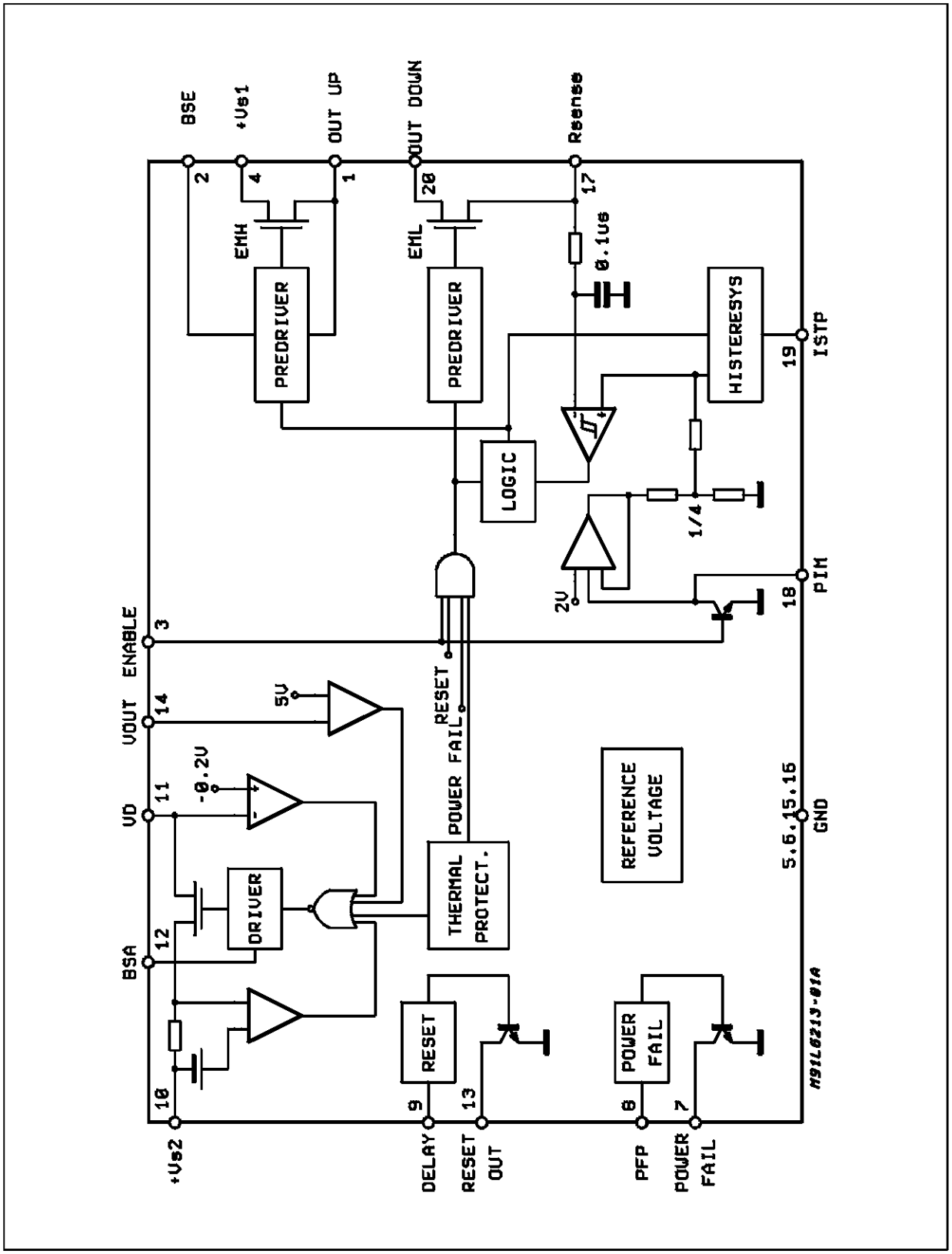
The level of hysteresis of the current can be changed through an external resistor.

The device is supplied in Powerdip 16+2+2, and use the four center pins to conduct heat to the printed circuit.

APPLICATION CIRCUIT



BLOCK DIAGRAM



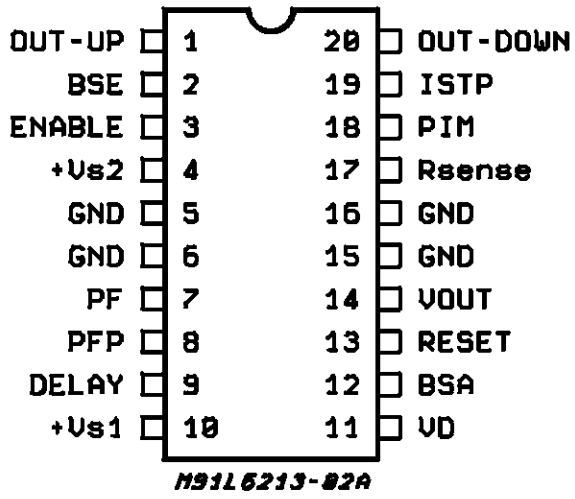
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	52	V
V_D; V_{OUT-UP}	Output Negative Voltage DC	-1.3	V
V_D	Output Negative Voltage peak at t = 0.1µs f = 100KHz	-5V	V
$V_{OUT-DOWN}$	Output Positive Voltage DC	V_S + 1.3	V
	Output Positive Voltage peak at t = 0.1µs f = 25KHz	V_S + 5	V
V_{OUT-UP}	Output Negative Voltage peak at t = 0.1µs f = 25KHz	-5	V
PFP	Input Voltage	25	V
V_O, Enable PIM	Input Voltage	7	V
Reset, PF	Output Voltage	20	V
CD, ISTP	Input Voltage	5.5	V
Out-Up Out-Down	Output Current DC = 10% T_{ON} = 3.5ms	5.5	A
T_{stg}	Storage Temperature	-50 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	14	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	60	°C/W

PIN CONNECTION (Top view)



PIN DESCRIPTION

Nr.	Name	Description
1	Out-Up	Solenoid section upper DMOS output.
2	BSE	Solenoid section upper DMOS bootstrap. A capacitor connected between pin 2 and pin 1 ensures the efficient driving of the solenoid section upper DMOS.
3	ENABLE	Solenoid control input - TTL compatible.
4	$+V_{S1}$	Unregulated voltage input - Solenoid section.
5, 6	GND	Ground.
7	PF	Power fail output, the saturation of PF is guaranteed if VPS exceed 3V. PF is at logic 1 a time T_1 after RESET reached the high level. PF came back to logic 0 when VPS goes down under 18V. (see fig. 1)
8	PFP	Power fail programming. A resistor divider connected to VPS changes the Power fail threshold levels.
9	CD	Capacitor delay. A capacitor connected to this pin determines the Reset signal delay time t_d.
10	V_{S2}	Unregulated voltage input - SMPS sections.
11	VD	Regulator output and diode voltage control.
12	BSA	SMPS section DMOS bootstrap. A capacitor connected between pin 12 and pin 11 ensures efficient driving of SMPS DMOS.
13	RESET	Reset output. The saturation of Reset is guaranteed if VPS exceeds 3V. The Reset output reaches the logic level 1 a time delay (set by capacitor CD) after VPS has reached a rising threshold voltage. Reset reaches 0 level when VPS goes down below folling threshold.
14	V_{out}	Feed back input of the regulation loop.
15, 16	GND	Ground.
17	R_{sense}	Connection for solenoid sensing resistor.
18	PIM	Programming of solenoid current rising edge. An RC network connected to this pin determines the slope of the solenoid current rising edge.
19	ISTP	Programming of solenoid current histeresys.
20	Out-Down	Solenoid section lower DMOS output.

ELECTRICAL CHARACTERISTICS (Refer to the application circuit, T_J =25°C, I_{out} Power Supply = 50mA, VPS from 12V to 46V; unless otherwise specified.

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
STEP-DOWN SECTION							
10, 4	V_i	Supply Voltage		14		46	V
14	V_o	Output Voltage	I_O = 0.05 to 1A	4.85		5.2	V
	$R_{DS\,on}$	On State Drain Resistance	T_J = 25°C; VPS = 15 to 46V		0.56	0.7	Ω
10	$t_{h\,on}$	Turn-on Threshold	VPS Rising Fig. 1	10		12	V
10	$t_{h\,off}$	Turn-off Threshold	VPS Falling Fig. 1	10		12	V
10	I_B	Input Bias Current				15	mA
11	I_{lim}	Static Current Limiting		2.2		3.4	A
2, 10	I_i	Total Input Current	ENABLE = 1, VPS = 46V, I_{load} = 0			13	mA
2, 10	I_i	Total Input Current	ENABLE = 1, VPS = 15V, I_{load} = 0			18	mA
11	t_{dp}	Protection Current Maximum Delay Time				1	µs
	t_{off}	Minimum Power off State	VPS = 46V I_O = 50mA	4.2		7.8	µs

ELECTRICAL CHARACTERISTICS (continued)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
POWER FAIL							
10	V_{thR}	Rising Threshold Voltage	PFP open Fig. 1	19.5	20	23	V
10	V_{thF}	Falling Threshold Voltage	PFP open Fig. 1	16.6	18.1	19.5	V
10	ΔV_{th}	Threshold Hysteresis	PFP open Fig. 1	0.5			V
8	I_{PFI}	Divided Internal Current				130	µA
8	$V_{th\text{-}PFP}$	Rising Threshold Voltage	VPS = 24V	1.1	1.21	1.29	V
8	$V_{th\text{-}PFP}$	Falling Threshold Voltage	VPS = 24V	0.98	1.06	1.13	V
8	$\Delta V_{th\ -PFP}$	Threshold Hysteresis	VPS = 24V	30			mV
7	V_{sat}	Output PF Saturation	PF current = 2.5mA VPS = 3 to 46V			0.4	V
7	I_{leak}	Output Leakage Current	VPS = 46V VPF = 20V			50	µA
7	t1	Delay to Reset	RESET High to PF high Delay Time (fig. 1)	0		1	µs
7	t2	Noise Immunity	When VPS drops to 8V for a time from 0 to t2, PF must be at 1 logic level (fig. 2)	0		1	µs
7	t3	Noise Immunity	When VPS drops to 17V for a time greater than t3, PF must be at 0 logic level (fig. 2)	4			µs
RESET							
9	I_d	Delay Source Current	V_D = 0 to 4.1V	70		140	µA
9	I_d	Delay Sink Current	VD = 4.3 to 2V	10			mA
13	V_{sat}	Output RESET Saturation	RESET Current = 2.5mA VPS = 3 to 46V			0.4	V
13	I_{leak}	Output Leakage Current	VPS = 46V RD = 4 to 5V V_{RESET} = 20V			50	µA
13	t4	Noise Immunity	When VPS drops to 10V for a time greater than t4 RESET must be at 0 logic level (fig. 1)	4			µs
SOLENOID CONTROL SECTION							
18	Vsat	Saturation Voltage	ENABLE = 1 I PIM = 5mA			0.2	V
18	I_{leak}	Leakage Current	PIM = 0.2 to 2.5V ENABLE = 0			±100	µA
18	V_{clamp}	Clamp Voltage		1.9	2	2.1	V
17		Minimum Offset Threshold	PIM = GND V_{sens} = 10mV ENABLE = 0	lower MOS must be in conduction			
17		MAximum Offset Voltage	PIM = GND V_{sens} = 50mV ENABLE = 0	lower MOS must be open			
17	V_{sense}	Static Voltage Limiting Threshold	V_{sens} going from 0 to 0.6V PIM = 3V, the EMH DMOS goes to high resistance state when V_{sens} is within: (see Block Diagram)	0.475	0.5	0.525	V
17		Maximum Delay Time				1	µs
	t_p	Protection Time		2		4	µs
	EMH R_{on}	On State Drain to Source Resistance	T_j = 25°C, VPS 15 to 46V		0.35	0.45	Ω
	EML R_{on}	On State Drain to Source Resistance	Tj = 25°C, VPS 15 to 46V		0.28	0.4	Ω
17	V_{sense}	Vsense Hysteresis	IST = Open IST = 0.75V IST = 3V	35 15 80	50 25 100	65 35 120	mV mV mV

Figure 1: Power Fail and Reset Static Operation. (PFP open)

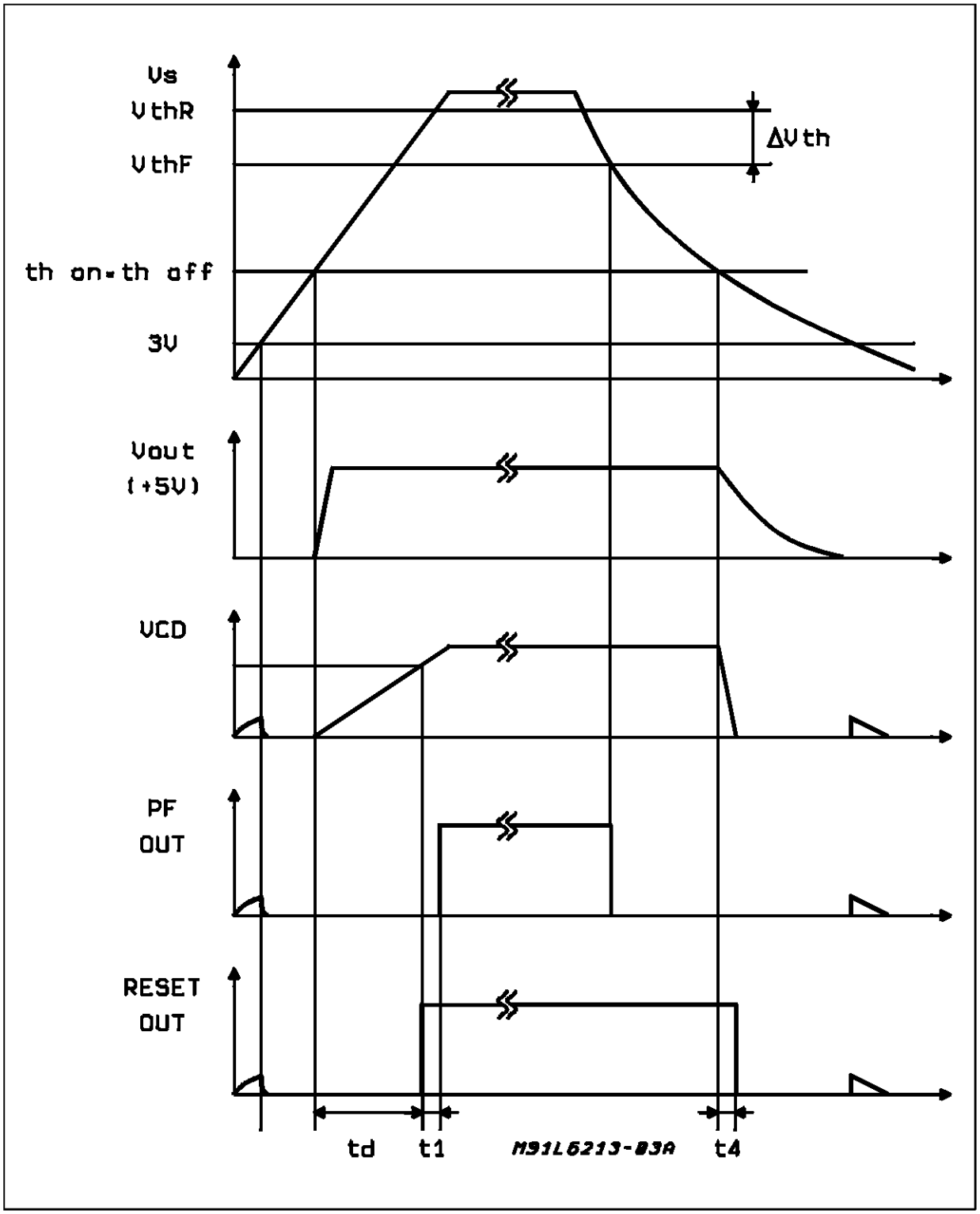
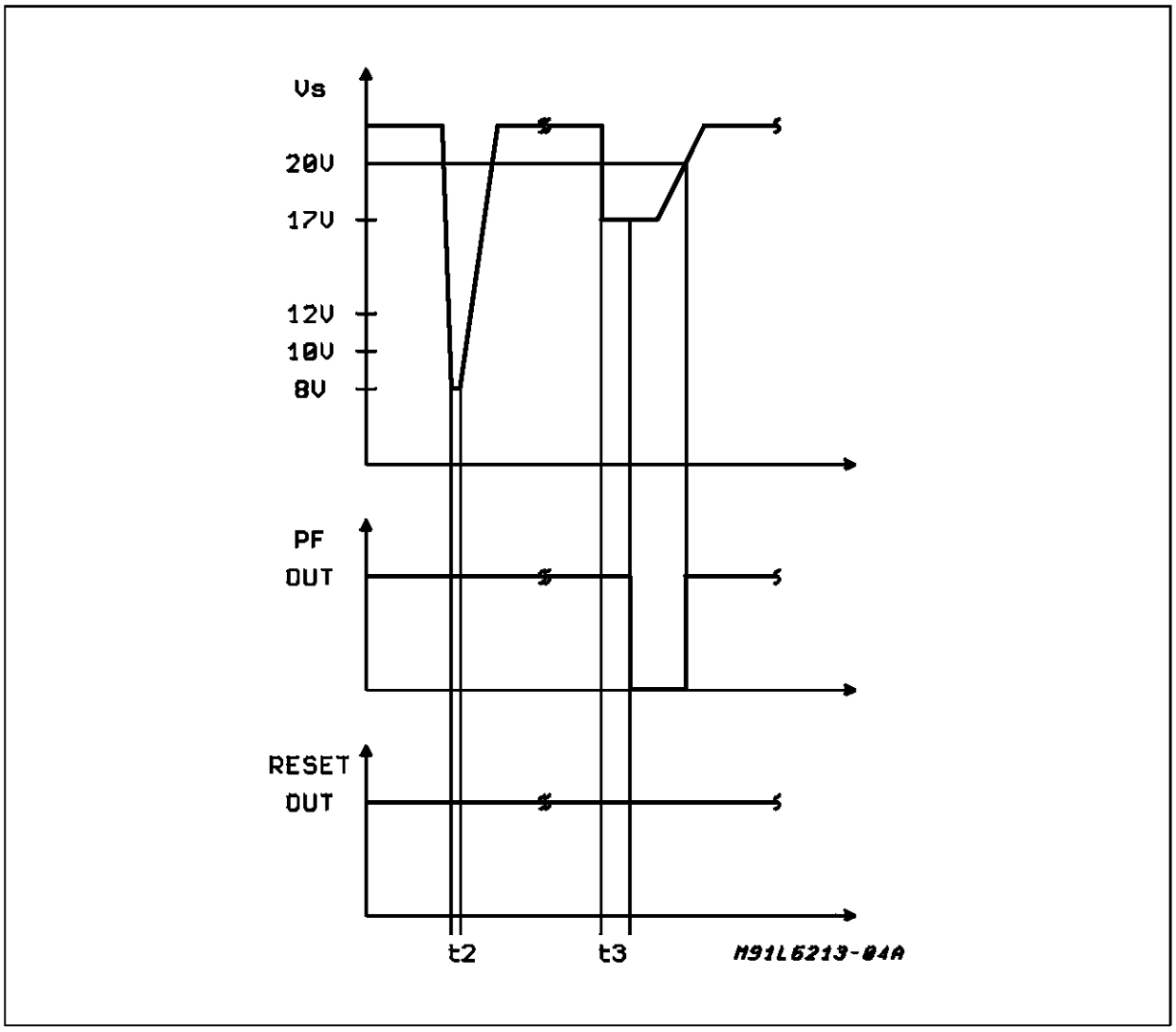


Figure 2: Power Fail and Reset Noise Immunity and Dynamic Operation.



POWERDIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		22.86			0.900	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050