Technical Summary

X.25 Protocol Controller (XPC)

The MC68605 X.25 Protocol Controller (XPC) is an intelligent HCMOS communications protocol controller that implements the 1984 International Telegraph and Telephone Consultative Committee (CCITT) X.25 Recommendation, data link access procedure (LAPB). It supports full duplex point-to-point serial communication at up to 10 megabits per second (MBPS) and relieves the host processor of managing the communications link by providing sequencing using HDLC framing, error control, retransmission based upon a cyclic redundancy check (CRC), and flow control using the receive not ready supervisory frame. The XPC directly supports the physical level interfaces (Recommendation X.21 physical level, X.21 *bis*, and V-series) and also provides an efficient interface to the packet level for information and control exchange. Key features of the XPC include:

- Fully Implements X.25 Recommendation LAPB Procedure by Independently Generating Link Level Commands and Responses
- Option to Implement X.75 Recommendation
- Optional Transparent Operation (Monitor Mode) where XPC Provides HDLC/SDLC Framing Functions for User Generated Frames
- Performs DMA Transfer of Information Frames To and From Memory Using Two On-Chip 22-Byte FIFOs
- Primary Communication Through Shared Memory Structures with a Powerful Command Set to Off-Load Data Link Management
- Flexible Rx/Tx Linked Memory Structures Minimize Host Intervention and Simplify Memory Management
- Basic (Modulo 8) and Extended (Modulo 128) Operation
- Automatic Comparison of the Programmable Local and Remote Addresses
- Detection of Programmable Timeout and Retries Limit Conditions
- 16- or 32-Bit CRC Generation and Checking
- Standard Modem Interface
- NRZ or NRZI Encoding/Decoding
- Vectored Interrupts and Status Reporting
- Built-In Diagnostics Provide Local Loopback and External Loopback Testing
- Up to 10 Mbps Synchronous Serial Data Rate
- 12.5 and 10 MHz System Clock Versions
- 8- and 16-Bit Data Bus Support
- 32-Bit Address Bus with Virtual Address Capability
- M68000 Family Asynchronous Bus Structure
- Programmable Byte Ordering of Data for Alternate Memory Organization Schemes