# MK2771-16
# VCXO and Set-Top Clock Source

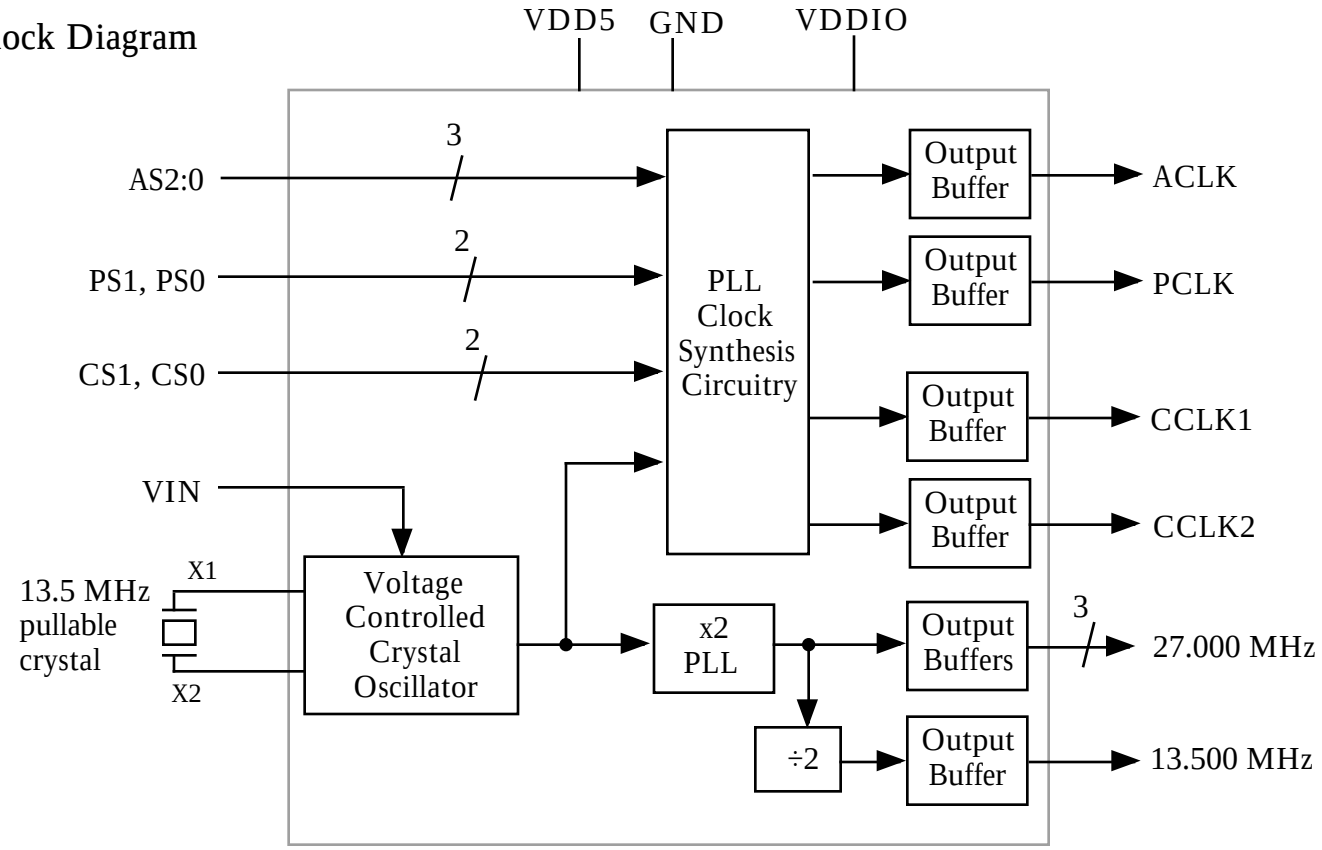
## Description

The MK2771-16 is a low cost, low jitter, high performance VCXO and clock synthesizer designed for set-top boxes. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3V input voltage to cause the output clocks to vary by ±100 ppm. Using ICS/MicroClock's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 13.5 MHz crystal input to produce multiple output clocks including a selectable processor clock, a selectable audio clock, two communications clocks, a 13.5 MHz clock, and three 27 MHz clocks. All clocks are frequency locked to the 27.00MHz output (and to each other) with zero ppm error, so any output can be used as the VCXO output.

## Features

- Packaged in 28 pin SSOP (QSOP)
- On-chip patented VCXO with pull range of 200ppm (minimum)
- VCXO tuning voltage of 0 to 3V
- Processor frequency include 16.66, 20, 25, 32, 40, and 50 MHz
- Audio clocks support 32 kHz, 44.1 kHz, 48 kHz and 96 kHz sampling rates
- Zero ppm synthesis error in all clocks (all exactly track 27MHz VCXO)
- Uses an inexpensive 13.5 MHz crystal
- Full CMOS output swings with 25mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 5V operating voltage with 3.3V capable I/O

## Block Diagram





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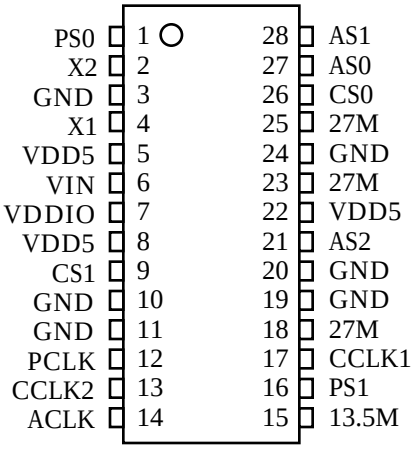
## Pin Assignment




VDD5=5V±10%
VDDIO=3.3V±10%
VIN=0 to 3.0V (3.3V OK)

### Audio Clock (MHz)

| AS2 | AS1 | AS0 | ACLK |
|---|---|---|---|
| 0 | 0 | 0 | 8.192 |
| 0 | 0 | 1 | 11.2896 |
| 0 | 1 | 0 | 12.288 |
| 0 | 1 | 1 | 5.6448 |
| 1 | 0 | 0 | 18.432 |
| 1 | 0 | 1 | 16.9344 |
| 1 | 1 | 0 | 49.152 |
| 1 | 1 | 1 | 24.576 |

0 = connect directly to GND
M = leave unconnected (floating)
1 = connect directly to VDDIO

### Communications Clocks (MHz)

| CS1 | CS0 | CCLK1 | CCLK2 |
|---|---|---|---|
| 0 | 0 | Low | 33.333 |
| 0 | 1 | Low | 24.576 |
| 1 | 0 | 11.0592 | 18.432 |
| 1 | 1 | 11.0592 | 3.6864 |

### Processor Clock (MHz)

| PS1 | PS0 | PCLK |
|---|---|---|
| 0 | 0 | 50 |
| 0 | 1 | 16.667 |
| M | 0 | 25 |
| M | 1 | 32 |
| 1 | 0 | 40 |
| 1 | 1 | 20 |

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | PS0 | I | Processor Clock Select 0. Selects PCLK frequency. See table above. Internal pull-up. |
| 2 | X2 | XO | Crystal connection. Connect to a pullable 13.5 MHz crystal. |
| 3, 10, 11 | GND | P | Connect to ground. |
| 4 | X1 | XI | Crystal connection. Connect to a pullable 13.5 MHz crystal. |
| 5, 8, 22 | VDD5 | P | Connect to +5V. |
| 6 | VIN | I | Voltage Input to VCXO. Zero to 3V signal which controls the frequency of the VCXO. |
| 7 | VDDIO | P | Connect to +3.3V or +5V. Amplitude of inputs and outputs will match this. |
| 9 | CS1 | I | Communications clock select pin 1 . Selects CCLK 1 and 2 per table above. Internal pull-up. |
| 12 | PCLK | O | Processor Clock output. Determined by status of PS1, PS0. |
| 13 | CCLK2 | O | Communications Clock output 2 determined by status of CS1,CS0 per table above. |
| 14 | ACLK | O | Audio Clock Output. Determined by status of AS2:0 per table above. |
| 15 | 13.5M | O | 13.50 MHz VCXO clock output. |
| 16 | PS1 | TI | Processor Clock Select 1. Selects PCLK frequency. See table above. Self-biased to M. |
| 17 | CCLK1 | O | Communications Clock output 1 determined by status of CS1, CS0 per table above. |
| 18, 23, 25 | 27M | O | 27.00 MHz VCXO clock output. |
| 19, 20, 24 | GND | P | Connect to ground. |
| 21 | AS2 | I | Audio Clock Select 2. Selects ACLK on pin 14 per table above. Internal pull-up. |
| 26 | CS0 | I | Communications clocks select pin 0. Selects CCLK1 and 2 per table above. Internal pull-up. |
| 27 | AS0 | I | Audio Clock Select 0. Selects ACLK on pin 14. See table above. Internal pull-up. |
| 28 | AS1 | I | Audio Clock Select 1. Selects ACLK on pin 14. See table above. Internal pull-up. |

Key: I = Input; TI = Tri-level input; O = output; P = power supply connection; XI, XO = crystal connections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## Electrical Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| **ABSOLUTE MAXIMUM RATINGS (note 1)** | | | | | |
| Supply voltage, VDD | Referenced to GND | | | 7 | V |
| Inputs and Clock Outputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Ambient Operating Temperature | | 0 | | 70 | °C |
| Soldering Temperature | Max of 10 seconds | | | 260 | °C |
| Storage temperature | | -65 | | 150 | °C |
| **DC CHARACTERISTICS (VDD = 5.0V unless noted)** | | | | | |
| Operating Voltage, VDD | | 4.75 | | 5.25 | V |
| Operating Voltage, VDDIO | for all inputs/outputs | 3.00 | | 5.25 | V |
| Input High Voltage, VIH, X1 pin only | | 3.5 | 2.5 | | V |
| Input Low Voltage, VIL, X1 pin only | | | 2.5 | 1.5 | V |
| Input High Voltage, VIH (except PS1) | | 2 | | | V |
| Input Low Voltage, VIL (except PS1) | | | | 0.8 | V |
| Input High Voltage, VIH, PS1 only | | VDD-0.5 | | | V |
| Input Low Voltage, VIL, PS1 only | | | | 0.5 | V |
| Output High Voltage, VOH | IOH=-25mA | 2.4 | | | V |
| Output Low Voltage, VOL | IOL=25mA | | | 0.4 | V |
| Output High Voltage, VOH, CMOS level | IOH=-8mA | VDD-0.4 | | | V |
| Operating Supply Current, IDD5 | No Load, note 2 | | 42 | | mA |
| Operating Supply Current, IDDIO | No Load, VDDIO=3.3V | | 19 | | mA |
| Short Circuit Current | Each output | | ±100 | | mA |
| Input Capacitance | | | 7 | | pF |
| Frequency synthesis error | All clocks | | | 0 | ppm |
| VIN, VCXO control voltage | | 0 | | 3 | V |
| **AC CHARACTERISTICS (VDD = 5.0V unless noted)** | | | | | |
| Input Frequency | | | 13.500000 | | MHz |
| Output Clock Rise Time | 0.8 to 2.0V | | | 1.5 | ns |
| Output Clock Fall Time | 2.0 to 0.8V | | | 1.5 | ns |
| Output Clock Duty Cycle | At 1.4V | 40 | | 60 | % |
| Maximum Absolute Jitter, short term | | | 300 | | ps |
| 27 MHz output pullability, note 3 | 0V ≤ VIN ≤ 3V | ±100 | ±140 | | ppm |

Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With all clocks at highest MHz.
3. With a pullable crystal that conforms to ICS' specifications:

| | |
|---|---|
| Correlation (load) capacitance | 14 pF |
| C0/C1 | 240 maximum |
| ESR | 25 Ω maximum |
| Initial Accuracy | ±20 ppm |
| Aging and Temp stability | ±50 ppm |
| Operating Temperature | 0 to 70°C |


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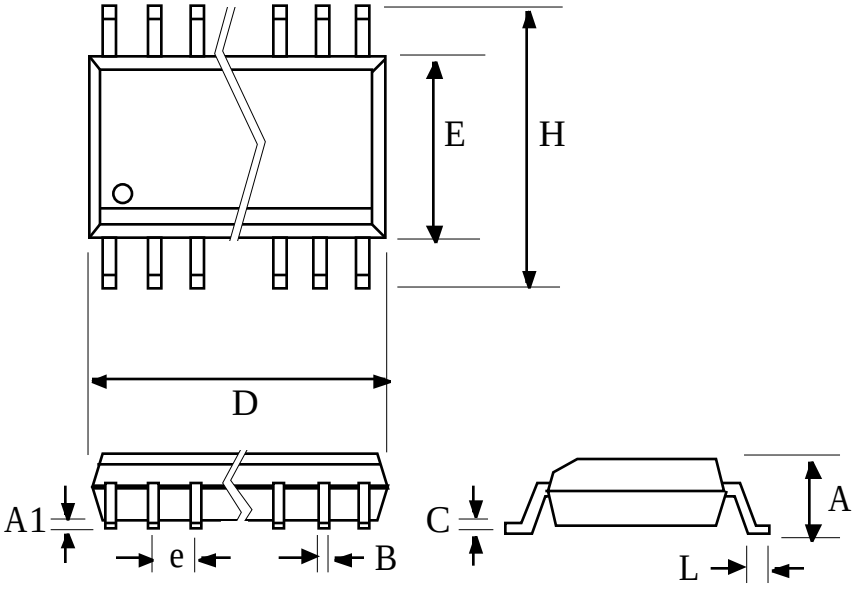
## External Components

The MK2771-16 requires a minimum number of external components for proper operation. Use a low inductance ground plane, connect all GNDs to this. Connect 0.01µF decoupling caps on pins 5, 7, 8 and 22 directly to the ground plane, as close to the MK2771-16 as possible. A series termination resistor of 33Ω may be used for each clock output.The 13.500 MHz crystal must be connected as close to the chip as possible. The crystal should be a parallel mode, pullable, with load capacitance of 14pF. Consult ICS/MicroClock full specifications. Please obey Application Note MAN05 for pullable crystal layout info except for the following: the MK2771-16 introduces a GND pin (pin #3) between the pullable crystal pins. This ground should be brought in straight from the right side underneath the device.

## Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)




28 pin SSOP

| | Inches | | Millimeters | |
|---|---|---|---|---|
| Symbol | Min | Max | Min | Max |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.102 | 0.254 |
| B | 0.008 | 0.012 | 0.203 | 0.305 |
| C | 0.007 | 0.010 | 0.191 | 0.254 |
| D | 0.386 | 0.394 | 9.804 | 10.008 |
| E | 0.150 | 0.157 | 3.810 | 3.988 |
| e | .025 BSC | | 0.635 BSC | |
| H | 0.228 | 0.244 | 5.791 | 6.198 |
| L | 0.016 | 0.050 | 0.406 | 1.270 |

## Ordering Information

| Part/Order Number | Marking | Shipping packaging | Package | Temperature |
|---|---|---|---|---|
| MK2771-16R | MK2771-16R | tubes | 28 pin SSOP (QSOP) | 0-70 °C |
| MK2771-16RTR | MK2771-16R | tape and reel | 28 pin SSOP (QSOP) | 0-70 °C |