## DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC


## HEF4006B <br> MSI

18-stage static shift register
Product specification
File under Integrated Circuits, IC04

PHILIPS

## DESCRIPTION

The HEF4006B is an 18-stage shift register arranged as two 4-stage and two 5-stage shift registers with a common clock input ( $\overline{\mathrm{CP}}$ ). The two 4-stage shift registers each have a data input $\left(\mathrm{D}_{\mathrm{A}}, \mathrm{D}_{\mathrm{B}}\right)$ and a data output $\left(\mathrm{O}_{3 \mathrm{~A}}, \mathrm{O}_{3 \mathrm{~B}}\right)$; the two


Fig. 1 Functional diagram.

## FUNCTION TABLE

| $\mathbf{D}_{\mathbf{n}}$ | $\overline{\mathbf{C P}}$ | $\mathbf{O}_{\mathbf{n}}{ }^{(5)}$ |
| :---: | :---: | :---: |
| $\mathrm{D}_{1}$ | $\square$ | $\mathrm{D}_{1}$ |
| X |  | no change |

## Notes

1. $\mathrm{X}=$ state is immaterial
2. $\int=$ positive-going transition
3. $\downarrow$ = negative-going transition
4. $\mathrm{D}_{1}=$ either HIGH or LOW
5. The moment $D_{1}$ appears at $O$ depends on the register length.

5-stage shift registers each have a data input ( $\mathrm{D}_{\mathrm{C}}, \mathrm{D}_{\mathrm{D}}$ ) and data outputs from the fourth and fifth stages $\left(\mathrm{O}_{3 \mathrm{C}}, \mathrm{O}_{4 \mathrm{C}}\right.$, $\mathrm{O}_{3 \mathrm{D}}, \mathrm{O}_{4 \mathrm{D}}$ ).

The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data are shifted into the first register position of each register from the data inputs ( $D_{A}$ to $D_{D}$ ) and all the data in each register are shifted one position to the right on the HIGH to LOW transition of $\overline{\mathrm{CP}}$.


Fig. 2 Pinning diagram.

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HEF4006BP(N): 14-lead DIL; plastic (SOT27-1)
HEF4006BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
HEF4006BT(D): 14-lead SO; plastic
(SOT108-1)
( ): Package Designator North America
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PINNING

| $\frac{D_{A} \text { to } D_{D}}{C P}$ | data inputs <br> clock input <br> (HIGH to LOW; edge-triggered) |
| :--- | :--- |
| $O_{3 A}$ to $O_{3 D} ; O_{4 C} ; O_{4 D}$ | data outputs |

FAMILY DATA, IDD LIMITS category MSI
See Family Specifications


Fig. 3 Logic diagram.

## 18-stage static shift register

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## AC CHARACTERISTICS

$\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$; input transition times $\leq 20 \mathrm{~ns}$

|  | $\begin{gathered} \mathbf{V}_{\mathrm{DD}} \\ \mathbf{V} \end{gathered}$ | SYMBOL | MIN | TYP | MAX |  | TYPICAL EXTRAPOLATION FORMULA |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Propagation delays $\overline{\mathrm{CP}} \rightarrow \mathrm{O}_{\mathrm{n}}$ <br> HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {PHL }}$ |  | $\begin{aligned} & 90 \\ & 40 \\ & 30 \end{aligned}$ | $\begin{array}{r} 180 \\ 80 \\ 60 \end{array}$ | ns <br> ns ns | $\begin{aligned} & 63 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) C_{\mathrm{L}} \\ & 29 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 22 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| LOW to HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $t_{\text {PLH }}$ |  | $\begin{aligned} & 90 \\ & 40 \\ & 35 \end{aligned}$ | $\begin{array}{r} \hline 180 \\ 85 \\ 70 \\ \hline \end{array}$ | ns <br> ns <br> ns | $\begin{aligned} & 63 \mathrm{~ns}+(0,55 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 29 \mathrm{~ns}+(0,23 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ & 27 \mathrm{~ns}+(0,16 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| Output transition times HIGH to LOW | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{t}_{\text {THL }}$ |  | $\begin{aligned} & 60 \\ & 30 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{array}{r} 120 \\ 60 \\ 40 \end{array}$ | ns <br> ns <br> ns | $\begin{aligned} 10 \mathrm{~ns} & +(1,0 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 9 \mathrm{~ns} & +(0,42 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 6 \mathrm{~ns} & +(0,28 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| LOW to HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | ${ }_{\text {t }}^{\text {th }}$ H |  | $\begin{aligned} & 60 \\ & 30 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{array}{r} 120 \\ 60 \\ 40 \\ \hline \end{array}$ | ns <br> ns <br> ns | $\begin{aligned} \hline 10 \mathrm{~ns} & +(1,0 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 9 \mathrm{~ns} & +(0,42 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \\ 6 \mathrm{~ns} & +(0,28 \mathrm{~ns} / \mathrm{pF}) \mathrm{C}_{\mathrm{L}} \end{aligned}$ |
| Minimum clock pulse width; HIGH | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | twCPH | $\begin{aligned} & 60 \\ & 40 \\ & 30 \end{aligned}$ | $\begin{aligned} & 30 \\ & 20 \\ & 15 \end{aligned}$ |  | ns <br> ns <br> ns | see also waveforms Fig. 4 |
| Set-up time $\mathrm{D}_{\mathrm{n}} \rightarrow \overline{\mathrm{CP}}$ | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $t_{\text {su }}$ | $\begin{array}{r} 20 \\ 10 \\ 5 \\ \hline \end{array}$ | $\begin{array}{r} 10 \\ 5 \\ 0 \end{array}$ |  | ns <br> ns ns |  |
| Hold time $\mathrm{D}_{\mathrm{n}} \rightarrow \overline{\mathrm{CP}}$ | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $t_{\text {hold }}$ | $\begin{aligned} & 5 \\ & 5 \\ & 5 \end{aligned}$ | $\begin{array}{r} \hline-5 \\ 0 \\ 0 \\ \hline \end{array}$ |  | ns <br> ns ns |  |
| Maximum clock pulse frequency | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\mathrm{f}_{\text {max }}$ | $\begin{array}{r} 9 \\ 15 \\ 18 \end{array}$ | $\begin{aligned} & 18 \\ & 30 \\ & 36 \end{aligned}$ |  | MHz <br> MHz <br> MHz |  |


|  | $\mathbf{V}_{\mathbf{D D}}$ | TYPICAL FORMULA FOR $\mathbf{P}(\mu \mathbf{W})$ |  |
| :--- | :---: | :---: | :--- |
| Dynamic power | 5 | $600 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | where |
| dissipation per | 10 | $3200 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{\mathrm{o}} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | $\mathrm{f}_{\mathrm{i}}=$ input freq. $(\mathrm{MHz})$ |
| package $(\mathrm{P})$ | 15 | $11600 \mathrm{f}_{\mathrm{i}}+\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right) \times \mathrm{V}_{\mathrm{DD}}{ }^{2}$ | $\mathrm{f}_{\mathrm{o}}=$ output freq. $(\mathrm{MHz})$ |
|  |  | $\mathrm{C}_{\mathrm{L}}=$ load capacitance $(\mathrm{pF})$ |  |
|  |  | $\sum\left(\mathrm{f}_{0} C_{\mathrm{L}}\right)=$ sum of outputs |  |
|  |  | $\mathrm{V}_{\mathrm{DD}}=$ supply voltage $(\mathrm{V})$ |  |



Fig. 4 Waveforms showing minimum clock pulse width, and set-up and hold-times for $D_{n}$ to $\overline{C P}$. Set-up and hold times are shown as positive values but may be specified as negative values.

